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FNA21012A

1200 V Motion SPM® 2 Series

Features

- UL Certified No. E209204 (UL1557)
- 1200 V - 10 A 3-Phase IGBT Inverter, Including Control ICs for Gate Drive and Protections
- Low-Loss, Short-Circuit-Rated IGBTs
- Very Low Thermal Resistance Using Al₂O₃ DBC Substrate
- Built-In Bootstrap Diodes and Dedicated Vs Pins Simplify PCB Layout
- Separate Open-Emitter Pins from Low-Side IGBTs for Three-Phase Current Sensing
- Single-Grounded Power Supply Supported
- Built-In NTC Thermistor for Temperature Monitoring and Management
- Adjustable Over-Current Protection via Integrated Sense-IGBTs
- Isolation Rating of 2500 Vrms / 1 min.

Applications

- Motion Control - Industrial Motor (AC 400 V Class)

Related Resources

- [AN-9075 - Users Guide for 1200V SPM® 2 Series](#)
- [AN-9076 - Mounting Guide for New SPM® 2 Package](#)
- [AN-9079 - Thermal Performance of 1200V Motion SPM® 2 Series by Mounting Torque](#)

General Description

The FNA21012A is a Motion SPM® 2 module providing a fully-featured, high-performance inverter output stage for AC induction, BLDC, and PMSM motors. These modules integrate optimized gate drive of the built-in IGBTs to minimize EMI and losses, while also providing multiple on-module protection features: under-voltage lockouts, over-current shutdown, temperature sensing, and fault reporting. The built-in, high-speed HVIC requires only a single supply voltage and translates the incoming logic-level gate inputs to high-voltage, high-current drive signals to properly drive the module's internal IGBTs. Separate negative IGBT terminals are available for each phase to support the widest variety of control algorithms.

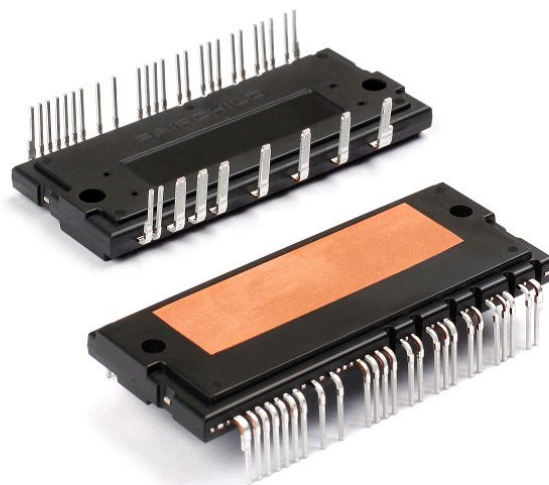


Figure 1. Package Overview

Package Marking and Ordering Information

| Device | Device Marking | Package | Packing Type | Quantity |
|-----------|----------------|-----------|--------------|----------|
| FNA21012A | FNA21012A | SPMCA-A34 | Rail | 6 |

Intergrated Power Functions

- 1200 V - 10 A IGBT inverter for three-phase DC / AC power conversion (refer to Figure 3)

Intergrated Drive, Protection, and System Control Functions

- For inverter high-side IGBTs: gate-drive circuit, high-voltage isolated high-speed level-shifting control circuit, Under-Voltage Lock-Out Protection (UVLO), Available bootstrap circuit example is given in Figures 5 and 15.
- For inverter low-side IGBTs: gate-drive circuit, Short-Circuit Protection (SCP) control circuit, Under-Voltage Lock-Out Protection (UVLO)
- Fault signaling: corresponding to UV (low-side supply) and SC faults
- Input interface: active-HIGH interface, works with 3.3 / 5 V logic, Schmitt-trigger input

Pin Configuration

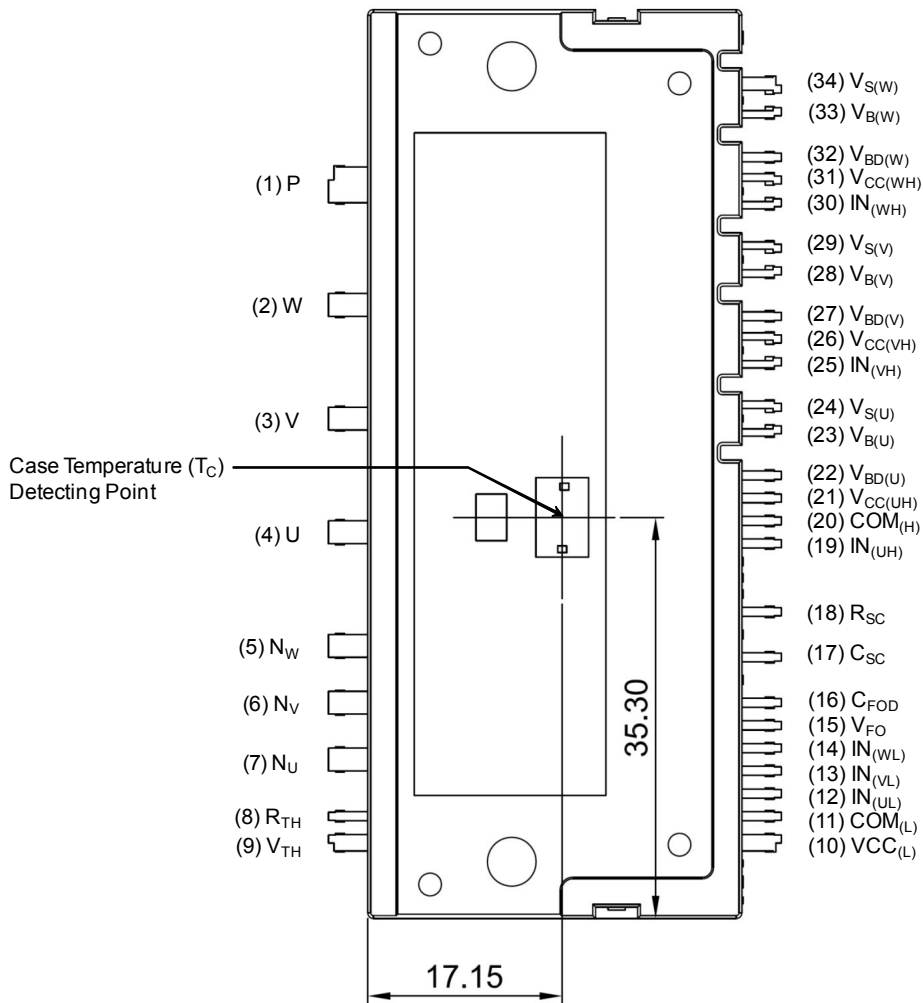


Figure 2. Top View

Pin Descriptions

| Pin Number | Pin Name | Pin Description |
|------------|---------------------|---|
| 1 | P | Positive DC-Link Input |
| 2 | W | Output for W Phase |
| 3 | V | Output for V Phase |
| 4 | U | Output for U Phase |
| 5 | N _W | Negative DC-Link Input for W Phase |
| 6 | N _V | Negative DC-Link Input for V Phase |
| 7 | N _U | Negative DC-Link Input for U Phase |
| 8 | R _{TH} | Series Resistor for Thermistor (Temperature Detection) |
| 9 | V _{TH} | Thermistor Bias Voltage |
| 10 | V _{CC(L)} | Low-Side Bias Voltage for IC and IGBTs Driving |
| 11 | COM _(L) | Low-Side Common Supply Ground |
| 12 | IN _(UL) | Signal Input for Low-Side U Phase |
| 13 | IN _(VL) | Signal Input for Low-Side V Phase |
| 14 | IN _(WL) | Signal Input for Low-Side W Phase |
| 15 | V _{FO} | Fault Output |
| 16 | C _{FOD} | Capacitor for Fault Output Duration Selection |
| 17 | C _{SC} | Capacitor (Low-Pass Filter) for Short-Circuit Current Detection Input |
| 18 | R _{SC} | Resistor for Short-Circuit Current Detection |
| 19 | IN _(UH) | Signal Input for High-Side U Phase |
| 20 | COM _(H) | High-Side Common Supply Ground |
| 21 | V _{CC(UH)} | High-Side Bias Voltage for U Phase IC |
| 22 | V _{BD(U)} | Anode of Bootstrap Diode for U Phase High-Side Bootstrap Circuit |
| 23 | V _{B(U)} | High-Side Bias Voltage for U Phase IGBT Driving |
| 24 | V _{S(U)} | High-Side Bias Voltage Ground for U Phase IGBT Driving |
| 25 | IN _(VH) | Signal Input for High-Side V Phase |
| 26 | V _{CC(VH)} | High-Side Bias Voltage for V Phase IC |
| 27 | V _{BD(V)} | Anode of Bootstrap Diode for V Phase High-Side Bootstrap Circuit |
| 28 | V _{B(V)} | High-Side Bias Voltage for V Phase IGBT Driving |
| 29 | V _{S(V)} | High-Side Bias Voltage Ground for V Phase IGBT Driving |
| 30 | IN _(WH) | Signal Input for High-Side W Phase |
| 31 | V _{CC(WH)} | High-Side Bias Voltage for W Phase IC |
| 32 | V _{BD(W)} | Anode of Bootstrap Diode for W Phase High-Side Bootstrap Circuit |
| 33 | V _{B(W)} | High-Side Bias Voltage for W Phase IGBT Driving |
| 34 | V _{S(W)} | High-Side Bias Voltage Ground for W Phase IGBT Driving |

Internal Equivalent Circuit and Input/Output Pins

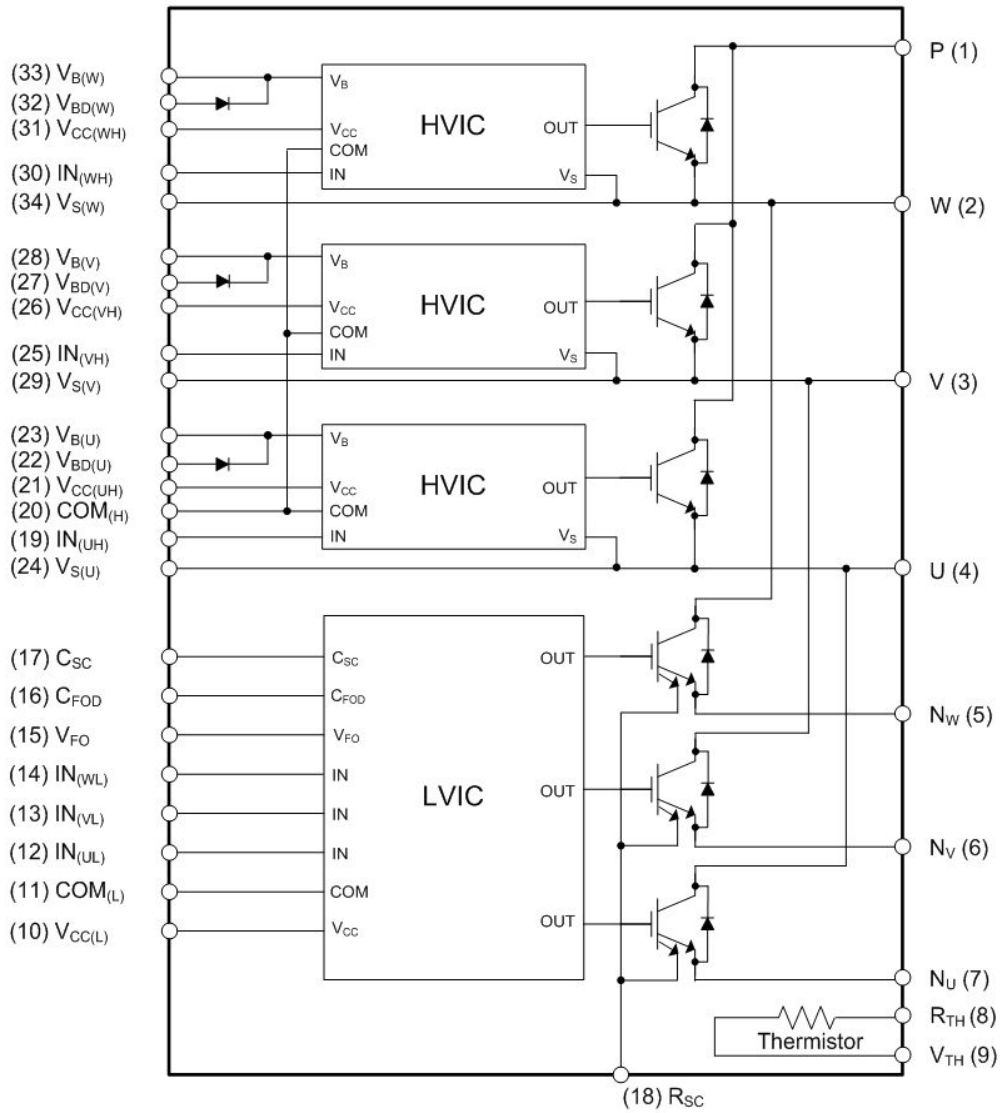


Figure 3. Internal Block Diagram

Notes:

1. Inverter high-side is composed of three normal-IGBTs, freewheeling diodes, and one control IC for each IGBT.
2. Inverter low-side is composed of three sense-IGBTs, freewheeling diodes, and one control IC for each IGBT. It has gate drive and protection functions.
3. Inverter power side is composed of four inverter DC-link input terminals and three inverter output terminals.

Absolute Maximum Ratings ($T_J = 25^\circ\text{C}$, unless otherwise specified.)**Inverter Part**

| Symbol | Parameter | Conditions | Rating | Unit |
|------------------------|------------------------------------|---|-----------|------------------|
| V_{PN} | Supply Voltage | Applied between P - N_U , N_V , N_W | 900 | V |
| $V_{PN(\text{Surge})}$ | Supply Voltage (Surge) | Applied between P - N_U , N_V , N_W | 1000 | V |
| V_{CES} | Collector - Emitter Voltage | | 1200 | V |
| $\pm I_C$ | Each IGBT Collector Current | $T_C = 25^\circ\text{C}$, $T_J \leq 150^\circ\text{C}$ (Note 4) | 10 | A |
| $\pm I_{CP}$ | Each IGBT Collector Current (Peak) | $T_C = 25^\circ\text{C}$, $T_J \leq 150^\circ\text{C}$, Under 1 ms Pulse Width (Note 4) | 20 | A |
| P_C | Collector Dissipation | $T_C = 25^\circ\text{C}$ per One Chip (Note 4) | 93 | W |
| T_J | Operating Junction Temperature | | -40 ~ 150 | $^\circ\text{C}$ |

Control Part

| Symbol | Parameter | Conditions | Rating | Unit |
|----------|--------------------------------|---|---------------------|------|
| V_{CC} | Control Supply Voltage | Applied between $V_{CC(H)}$, $V_{CC(L)}$ - COM | 20 | V |
| V_{BS} | High-Side Control Bias Voltage | Applied between $V_{B(U)} - V_{S(U)}$, $V_{B(V)} - V_{S(V)}$, $V_{B(W)} - V_{S(W)}$ | 20 | V |
| V_{IN} | Input Signal Voltage | Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$, $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$ - COM | -0.3 ~ $V_{CC}+0.3$ | V |
| V_{FO} | Fault Output Supply Voltage | Applied between V_{FO} - COM | -0.3 ~ $V_{CC}+0.3$ | V |
| I_{FO} | Fault Output Current | Sink Current at V_{FO} pin | 2 | mA |
| V_{SC} | Current Sensing Input Voltage | Applied between C_{SC} - COM | -0.3 ~ $V_{CC}+0.3$ | V |

Bootstrap Diode Part

| Symbol | Parameter | Conditions | Rating | Unit |
|-----------|------------------------------------|---|-----------|------------------|
| V_{RRM} | Maximum Repetitive Reverse Voltage | | 1200 | V |
| I_F | Forward Current | $T_C = 25^\circ\text{C}$, $T_J \leq 150^\circ\text{C}$ (Note 4) | 1.0 | A |
| I_{FP} | Forward Current (Peak) | $T_C = 25^\circ\text{C}$, $T_J \leq 150^\circ\text{C}$, Under 1 ms Pulse Width (Note 4) | 2.0 | A |
| T_J | Operating Junction Temperature | | -40 ~ 150 | $^\circ\text{C}$ |

Total System

| Symbol | Parameter | Conditions | Rating | Unit |
|-----------------------|--|--|-----------|------------------|
| $V_{PN(\text{PROT})}$ | Self-Protection Supply Voltage Limit (Short-Circuit Protection Capability) | $V_{CC} = V_{BS} = 13.5 \sim 16.5 \text{ V}$, $T_J = 150^\circ\text{C}$, Non-Repetitive, < 2 μs | 800 | V |
| T_C | Module Case Operation Temperature | See Figure 2 | -40 ~ 125 | $^\circ\text{C}$ |
| T_{STG} | Storage Temperature | | -40 ~ 125 | $^\circ\text{C}$ |
| V_{ISO} | Isolation Voltage | 60 Hz, Sinusoidal, AC 1 Minute, Connection Pins to Heat Sink Plate | 2500 | V_{rms} |

Thermal Resistance

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|----------------|--|---------------------------------------|------|------|------|-----------------------------|
| $R_{th(j-c)Q}$ | Junction-to-Case Thermal Resistance (Note 5) | Inverter IGBT Part (per 1 / 6 Module) | - | - | 1.33 | $^\circ\text{C} / \text{W}$ |
| $R_{th(j-c)F}$ | | Inverter FWD Part (per 1 / 6 Module) | - | - | 2.30 | $^\circ\text{C} / \text{W}$ |

Notes:

- These values had been made an acquisition by the calculation considered to design factor.
- For the measurement point of case temperature (T_C), please refer to Figure 2.

Electrical Characteristics ($T_J = 25^\circ\text{C}$, unless otherwise specified.)

Inverter Part

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---------------|--|--|------|------|------|---------------|
| $V_{CE(SAT)}$ | Collector - Emitter Saturation Voltage | $V_{CC} = V_{BS} = 15\text{ V}$ $V_{IN} = 5\text{ V}$ | - | 2.20 | 2.80 | V |
| V_F | FWDI Forward Voltage | $V_{IN} = 0\text{ V}$ $I_F = 10\text{ A}, T_J = 25^\circ\text{C}$ | - | 2.20 | 2.80 | V |
| HS | t_{ON} $t_{C(ON)}$ t_{OFF} $t_{C(OFF)}$ t_{rr} | Switching Times $V_{PN} = 600\text{ V}, V_{CC} = 15\text{ V}, I_C = 10\text{ A}$ $T_J = 25^\circ\text{C}$ $V_{IN} = 0\text{ V} \leftrightarrow 5\text{ V}$, Inductive Load See Figure 5 (Note 6) | 0.45 | 0.85 | 1.35 | μs |
| | | | - | 0.25 | 0.55 | μs |
| | | | - | 0.95 | 1.45 | μs |
| | | | - | 0.10 | 0.40 | μs |
| | | | - | 0.25 | - | μs |
| LS | t_{ON} $t_{C(ON)}$ t_{OFF} $t_{C(OFF)}$ t_{rr} | $V_{PN} = 600\text{ V}, V_{CC} = 15\text{ V}, I_C = 10\text{ A}$ $T_J = 25^\circ\text{C}$ $V_{IN} = 0\text{ V} \leftrightarrow 5\text{ V}$, Inductive Load See Figure 5 (Note 6) | 0.35 | 0.75 | 1.25 | μs |
| | | | - | 0.20 | 0.50 | μs |
| | | | - | 0.95 | 1.45 | μs |
| | | | - | 0.10 | 0.40 | μs |
| | | | - | 0.20 | - | μs |
| I_{CES} | Collector - Emitter Leakage Current | $V_{CE} = V_{CES}$ | - | - | 5 | mA |

Note:

6. t_{ON} and t_{OFF} include the propagation delay of the internal drive IC. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching times of IGBT under the given gate-driving condition internally. For the detailed information, please see Figure 4.

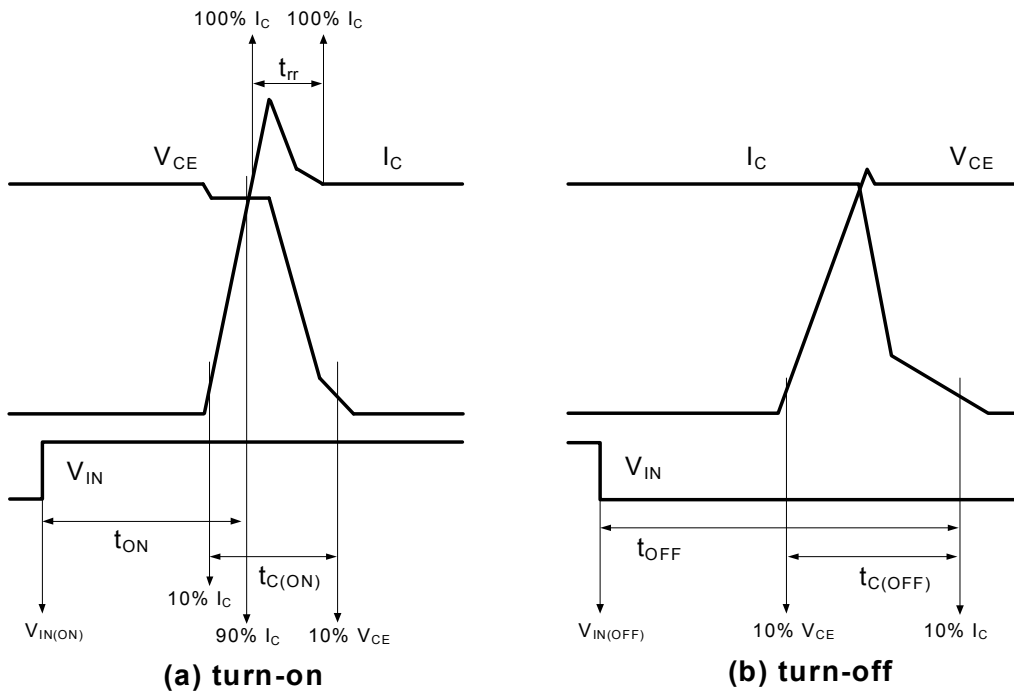


Figure 4. Switching Time Definition

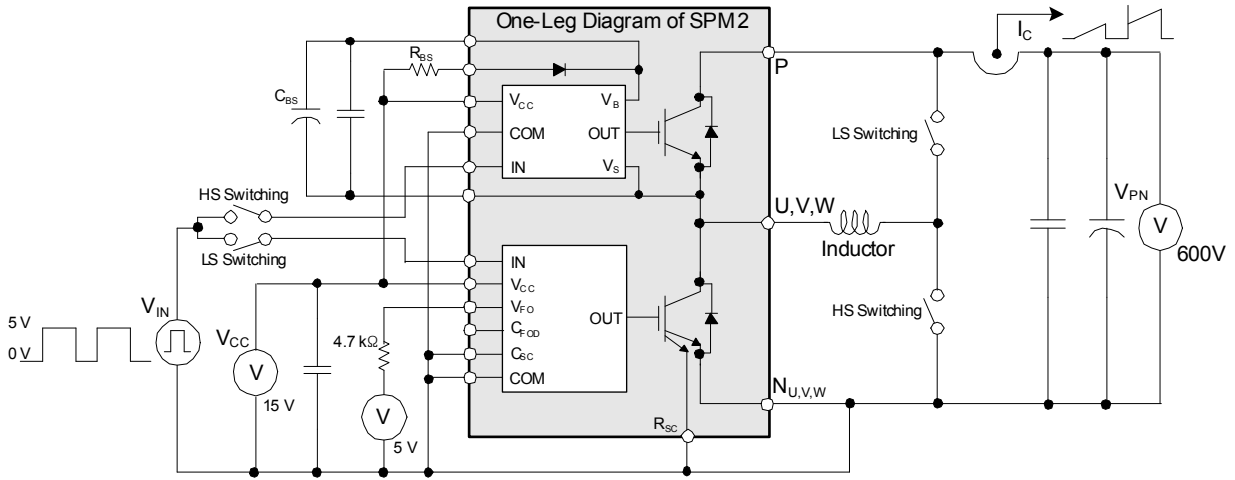


Figure 5. Example Circuit for Switching Test

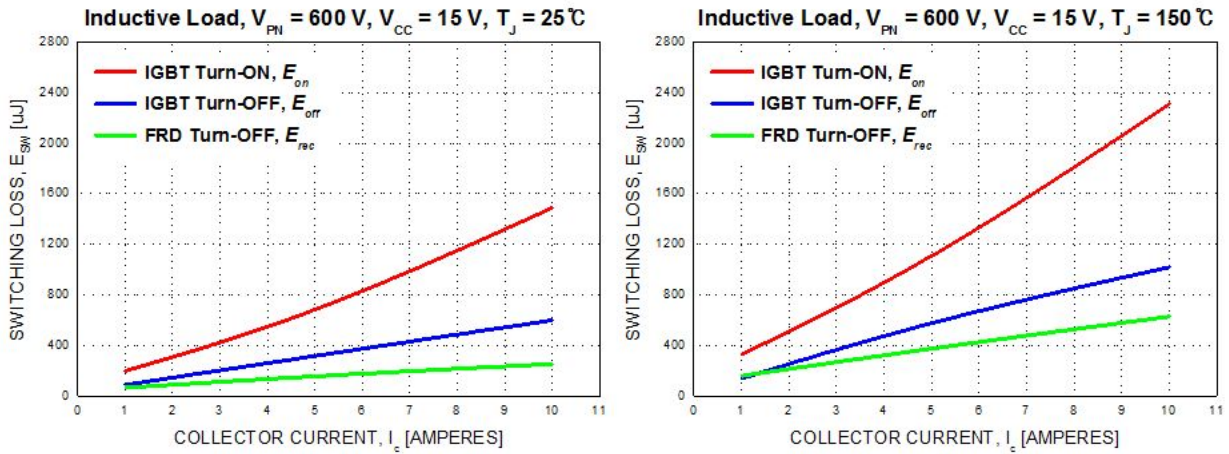


Figure 6. Switching Loss Characteristics (Typical)

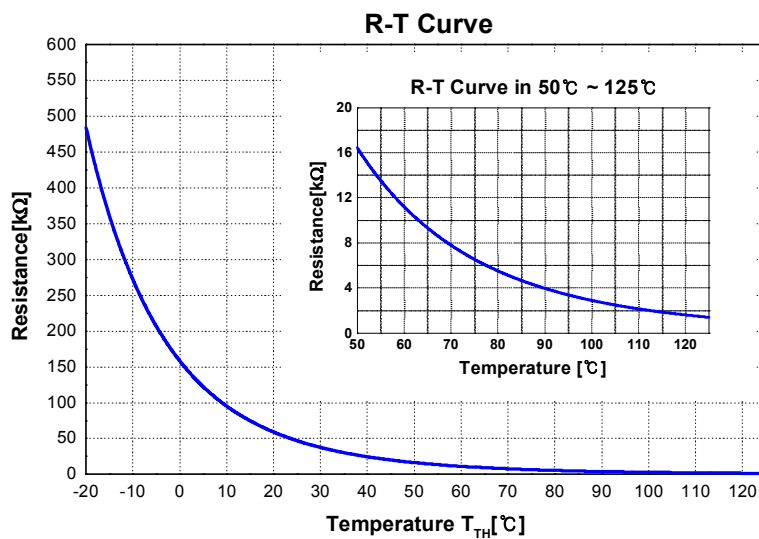


Figure 7. R-T Curve of Built-in Thermistor

Bootstrap Diode Part

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|----------|-----------------------|---|------|------|------|------|
| V_F | Forward Voltage | $I_F = 1.0 \text{ A}$, $T_J = 25^\circ\text{C}$ | - | 2.2 | - | V |
| t_{rr} | Reverse-Recovery Time | $I_F = 1.0 \text{ A}$, $dI_F / dt = 50 \text{ A} / \mu\text{s}$, $T_J = 25^\circ\text{C}$ | - | 80 | - | ns |

Control Part

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit | |
|---------------|---|--|-----------------------|------|------|------|---------------|
| I_{QCCH} | Quiescent V_{CC} Supply Current | $V_{CC(UH,VH,WH)} = 15 \text{ V}$, $I_{N(UH,VH,WH)} = 0 \text{ V}$ | | - | - | 0.15 | mA |
| I_{QCCL} | | $V_{CC(L)} = 15 \text{ V}$, $I_{N(UL,VL,WL)} = 0 \text{ V}$ | | - | - | 5.00 | mA |
| I_{PCCH} | Operating V_{CC} Supply Current | $V_{CC(UH,VH,WH)} = 15 \text{ V}$, $f_{PWM} = 20 \text{ kHz}$, Duty = 50%, Applied to one PWM Signal Input for High-Side | | - | - | 0.30 | mA |
| I_{PCCL} | | $V_{CC(L)} = 15 \text{ V}$, $f_{PWM} = 20 \text{ kHz}$, Duty = 50%, Applied to one PWM Signal Input for Low-Side | | - | - | 8.50 | mA |
| I_{QBS} | Quiescent V_{BS} Supply Current | $V_{BS} = 15 \text{ V}$, $I_{N(UH, VH, WH)} = 0 \text{ V}$ | | - | - | 0.30 | mA |
| I_{PBS} | Operating V_{BS} Supply Current | $V_{CC} = V_{BS} = 15 \text{ V}$, $f_{PWM} = 20 \text{ kHz}$, Duty = 50%, Applied to one PWM Signal Input for High-Side | | - | - | 4.50 | mA |
| V_{FOH} | Fault Output Voltage | $V_{CC} = 15 \text{ V}$, $V_{SC} = 0 \text{ V}$, V_{FO} Circuit: 4.7 k Ω to 5 V Pull-up | 4.5 | - | - | V | |
| V_{FOL} | | $V_{CC} = 15 \text{ V}$, $V_{SC} = 1 \text{ V}$, V_{FO} Circuit: 4.7 k Ω to 5 V Pull-up | - | - | 0.5 | V | |
| I_{SEN} | Sensing Current of Each Sense IGBT | $V_{CC} = 15 \text{ V}$, $V_{IN} = 5 \text{ V}$, $R_{SC} = 0 \Omega$, No Connection of Shunt Resistor at $N_{U,V,W}$ Terminal | | - | 7 | - | mA |
| $V_{SC(ref)}$ | Short Circuit Trip Level | $V_{CC} = 15 \text{ V}$ (Note 7) | | 0.43 | 0.50 | 0.57 | V |
| I_{SC} | Short Circuit Current Level for Trip | $R_{SC} = 68 \Omega (\pm 1\%)$, No Connection of Shunt Resistor at $N_{U,V,W}$ Terminal (Note 7) | - | 20 | - | A | |
| UV_{CCD} | Supply Circuit Under-Voltage Protection | Detection Level | 10.3 | - | 12.8 | V | |
| UV_{CCR} | | Reset Level | 10.8 | - | 13.3 | V | |
| UV_{BSD} | | Detection Level | 9.5 | - | 12.0 | V | |
| UV_{BSR} | | Reset Level | 10.0 | - | 12.5 | V | |
| t_{FOD} | Fault-Out Pulse Width | $C_{FOD} = \text{Open}$ | (Note 8) | 50 | - | - | μs |
| | | $C_{FOD} = 2.2 \text{ nF}$ | | 1.7 | - | - | ms |
| $V_{IN(ON)}$ | ON Threshold Voltage | Applied between $I_{N(UH, VH, WH)} - COM_{(H)}$, $I_{N(UL, VL, WL)} - COM_{(L)}$ | - | - | 2.6 | V | |
| $V_{IN(OFF)}$ | OFF Threshold Voltage | | 0.8 | - | - | V | |
| R_{TH} | Resistance of Thermistor | at $T_{TH} = 25^\circ\text{C}$ | See Figure 7 (Note 9) | - | 47 | - | k Ω |
| | | at $T_{TH} = 100^\circ\text{C}$ | | - | 2.9 | - | k Ω |

Notes:

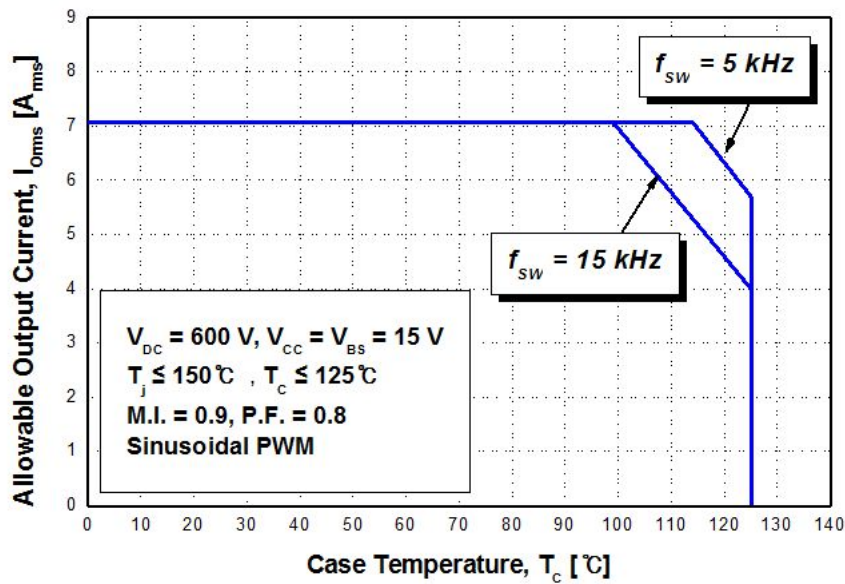
- Short-circuit current protection functions only at the low-sides because the sense current is divided from main current at low-side IGBTs. Inserting the shunt resistor for monitoring the phase current at N_U , N_V , N_W terminal, the trip level of the short-circuit current is changed.
- The fault-out pulse width t_{FOD} depends on the capacitance value of C_{FOD} according to the following approximate equation : $t_{FOD} = 0.8 \times 10^6 \times C_{FOD} \text{ [s]}$.
- T_{TH} is the temperature of thermistor itself. To know case temperature (T_C), conduct experiments considering the application.

Recommended Operating Conditions

| Symbol | Parameter | Conditions | Value | | | Unit |
|--------------------------|--|--|-------|------|------|------------------|
| | | | Min. | Typ. | Max. | |
| V_{PN} | Supply Voltage | Applied between P - N_U, N_V, N_W | 300 | 600 | 800 | V |
| V_{CC} | Control Supply Voltage | Applied between $V_{CC(UH, VH, WH)} - COM_{(H)}, V_{CC(L)} - COM_{(L)}$ | 13.5 | 15.0 | 16.5 | V |
| V_{BS} | High-Side Bias Voltage | Applied between $V_{B(U)} - V_{S(U)}, V_{B(V)} - V_{S(V)}, V_{B(W)} - V_{S(W)}$ | 13.0 | 15.0 | 18.5 | V |
| $dV_{CC}/dt, dV_{BS}/dt$ | Control Supply Variation | | -1 | - | 1 | V / μ s |
| t_{dead} | Blanking Time for Preventing Arm - Short | For Each Input Signal | 2.0 | - | - | μ s |
| f_{PWM} | PWM Input Signal | $-40^\circ\text{C} \leq T_C \leq 125^\circ\text{C}, -40^\circ\text{C} \leq T_J \leq 150^\circ\text{C}$ | - | - | 20 | kHz |
| V_{SEN} | Voltage for Current Sensing | Applied between $N_U, N_V, N_W - COM_{(H, L)}$ (Including Surge Voltage) | -5 | | 5 | V |
| $PW_{IN(ON)}$ | Minimum Input Pulse Width | $I_C \leq 20$ A, Wiring Inductance between N_U, V, W and DC Link N < 10nH (Note 10) | 1.5 | - | - | μ s |
| $PW_{IN(OFF)}$ | | | 1.5 | - | - | |
| T_J | Junction Temperature | | -40 | - | 150 | $^\circ\text{C}$ |

Note:

10. This product might not make output response if input pulse width is less than the recommended value.



Note:

11. This allowable output current value is the reference data for the safe operation of this product. This may be different from the actual application and operating condition.

Mechanical Characteristics and Ratings

| Parameter | Conditions | Min. | Typ. | Max. | Unit | |
|---------------------------|-----------------------------|--------------------------|------|------|-------|---------|
| Device Flatness | See Figure 9 | 0 | - | +200 | μm | |
| Mounting Torque | Mounting Screw: M4 | Recommended 1.0 N • m | 0.9 | 1.0 | 1.5 | N • m |
| | See Figure 10 | Recommended 10.1 kg • cm | 9.1 | 10.1 | 15.1 | kg • cm |
| Terminal Pulling Strength | Load 19.6 N | 10 | - | - | s | |
| Terminal Bending Strength | Load 9.8 N, 90 degrees Bend | 2 | - | - | times | |
| Weight | | - | 50 | - | g | |

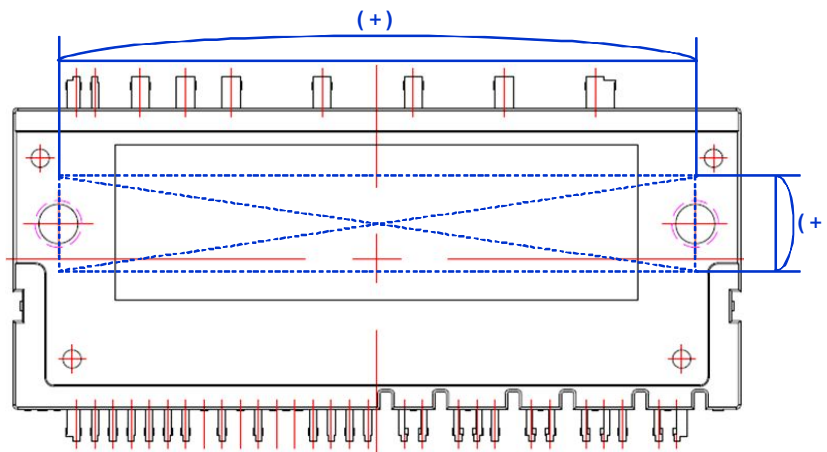


Figure 9. Flatness Measurement Position

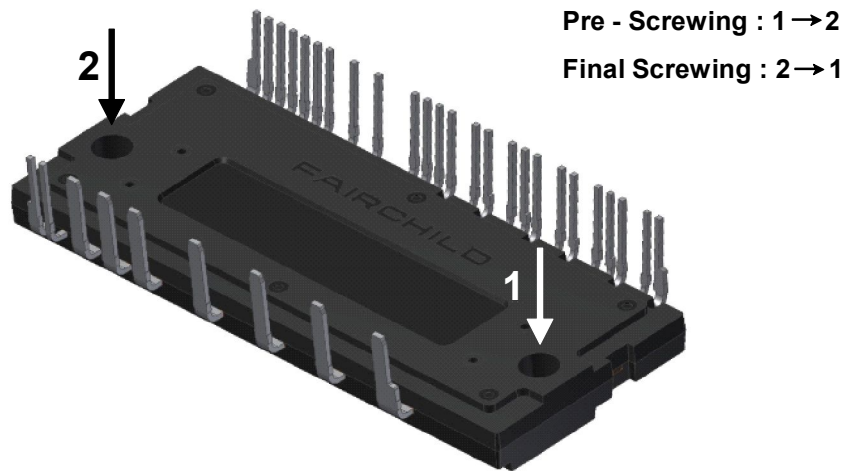


Figure 10. Mounting Screws Torque Order

Notes:

- 12. Do not over torque when mounting screws. Too much mounting torque may cause DBC cracks, as well as bolts and Al heat-sink destruction.
- 13. Avoid one-sided tightening stress. Figure 10 shows the recommended torque order for the mounting screws. Uneven mounting can cause the DBC substrate of package to be damaged. The pre-screwing torque is set to 20 ~ 30% of maximum torque rating.

Time Charts of SPMs Protective Function

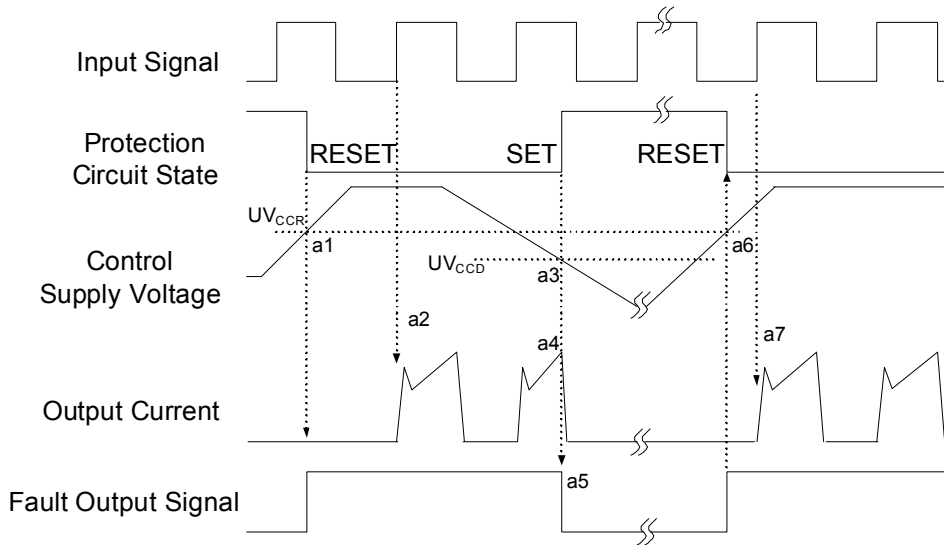


Figure 11. Under-Voltage Protection (Low-Side)

- a1 : Control supply voltage rises: after the voltage rises UV_{CCR} , the circuits start to operate when the next input is applied.
- a2 : Normal operation: IGBT ON and carrying current.
- a3 : Under-voltage detection (UV_{CCD}).
- a4 : IGBT OFF in spite of control input condition.
- a5 : Fault output operation starts with a fixed pulse width according to the condition of the external capacitor C_{FOD} .
- a6 : Under-voltage reset (UV_{CCR}).
- a7 : Normal operation: IGBT ON and carrying current by triggering next signal from LOW to HIGH.

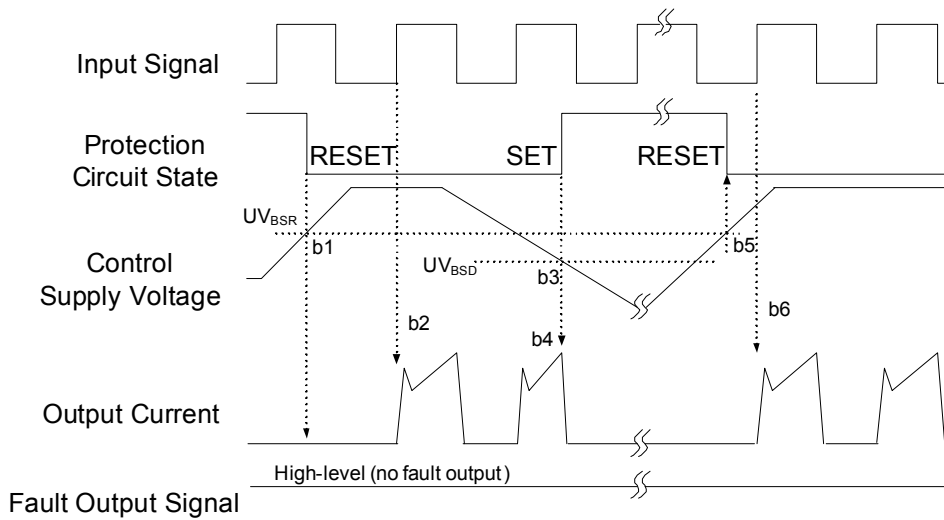


Figure 12. Under-Voltage Protection (High-Side)

- b1 : Control supply voltage rises: after the voltage reaches UV_{BSR} , the circuits start to operate when the next input is applied.
- b2 : Normal operation: IGBT ON and carrying current.
- b3 : Under-voltage detection (UV_{BSD}).
- b4 : IGBT OFF in spite of control input condition, but there is no fault output signal.
- b5 : Under-voltage reset (UV_{BSR}).
- b6 : Normal operation: IGBT ON and carrying current by triggering next signal from LOW to HIGH.

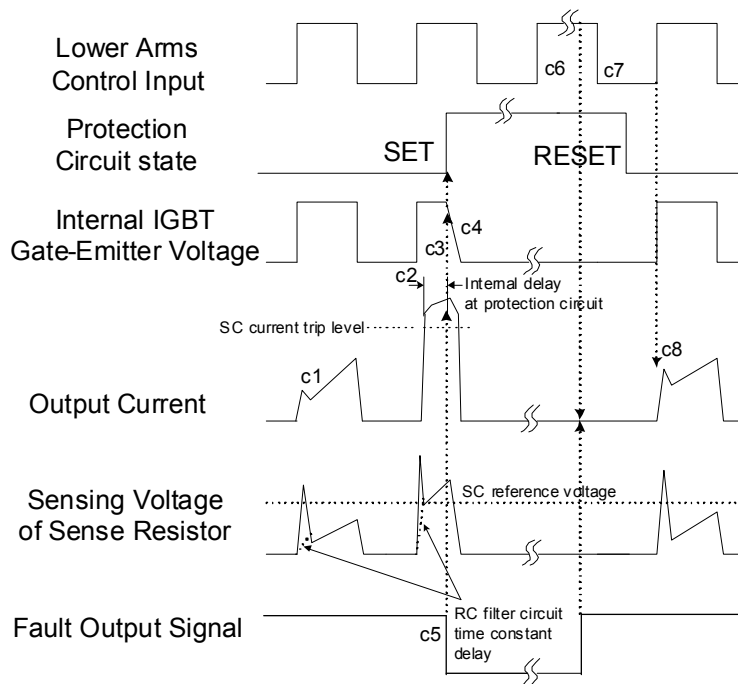


Figure 13. Short-Circuit Current Protection (Low-Side Operation only)

(with the external sense resistance and RC filter connection)

- c1 : Normal operation: IGBT ON and carrying current.
- c2 : Short-circuit current detection (SC trigger).
- c3 : All low-side IGBTs gate are hard interrupted.
- c4 : All low-side IGBTs turn OFF.
- c5 : Fault output operation starts with a fixed pulse width according to the condition of the external capacitor C_{FOD} .
- c6 : Input HIGH: IGBT ON state, but during the active period of fault output, the IGBT doesn't turn ON.
- c7 : Fault output operation finishes, but IGBT doesn't turn on until triggering the next signal from LOW to HIGH.
- c8 : Normal operation: IGBT ON and carrying current.

Input/Output Interface Circuit

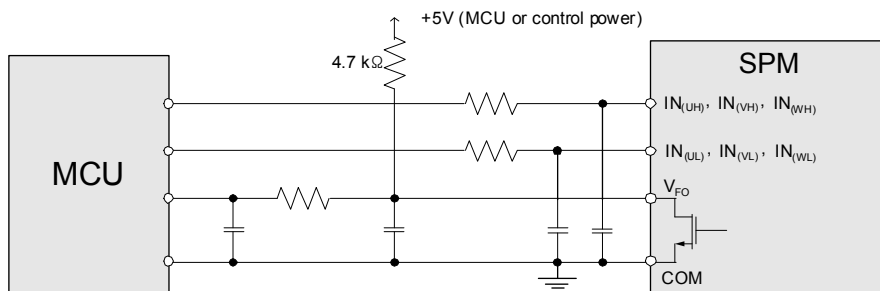


Figure 14. Recommended MCU I/O Interface Circuit

Note:

14. RC coupling at each input (parts shown dotted) might change depending on the PWM control scheme used in the application and the wiring impedance of the application's printed circuit board. The input signal section of the Motion SPM 2 product integrates 5 kΩ (typ.) pull-down resistor. Therefore, when using an external filtering resistor, please pay attention to the signal voltage drop at input terminal.

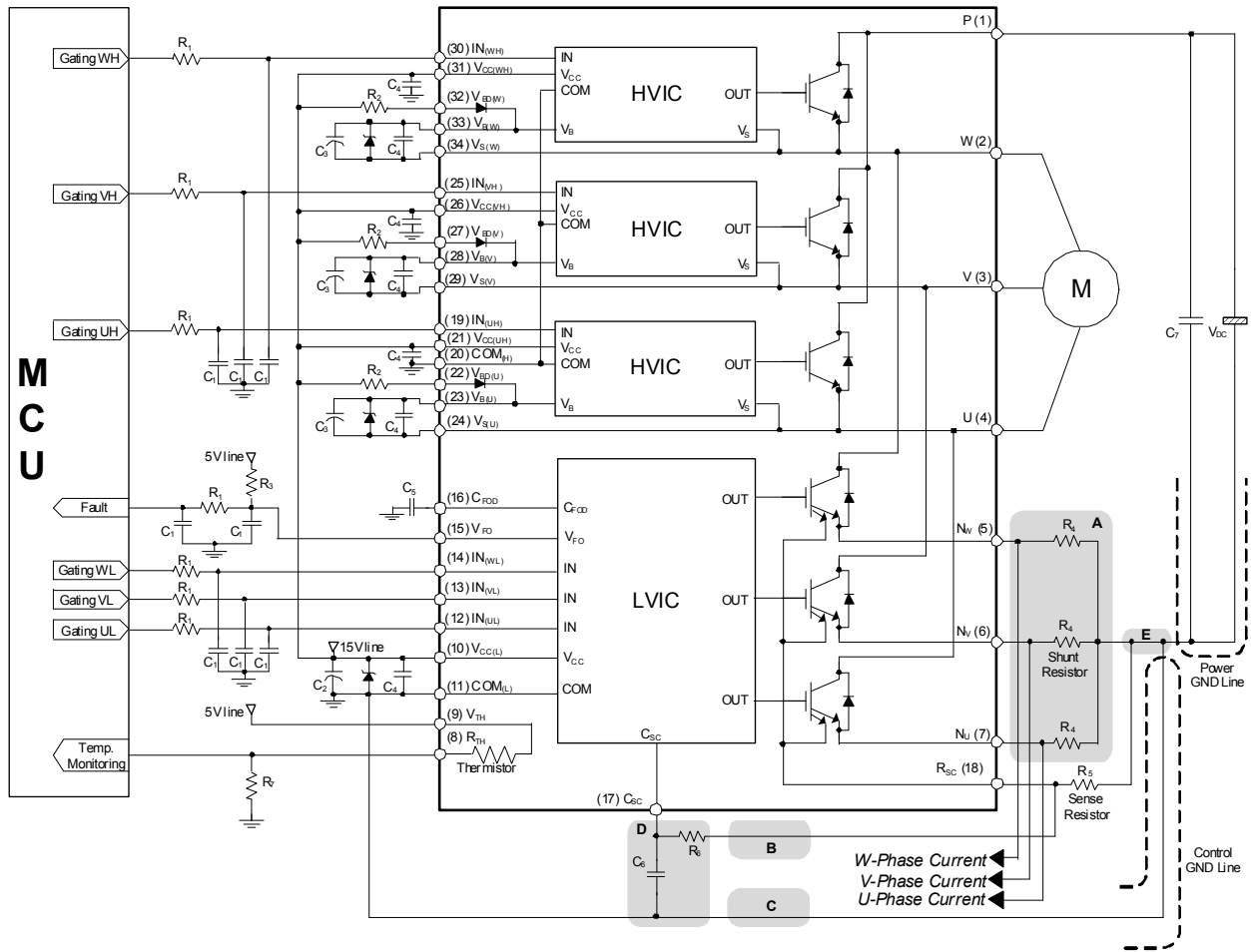
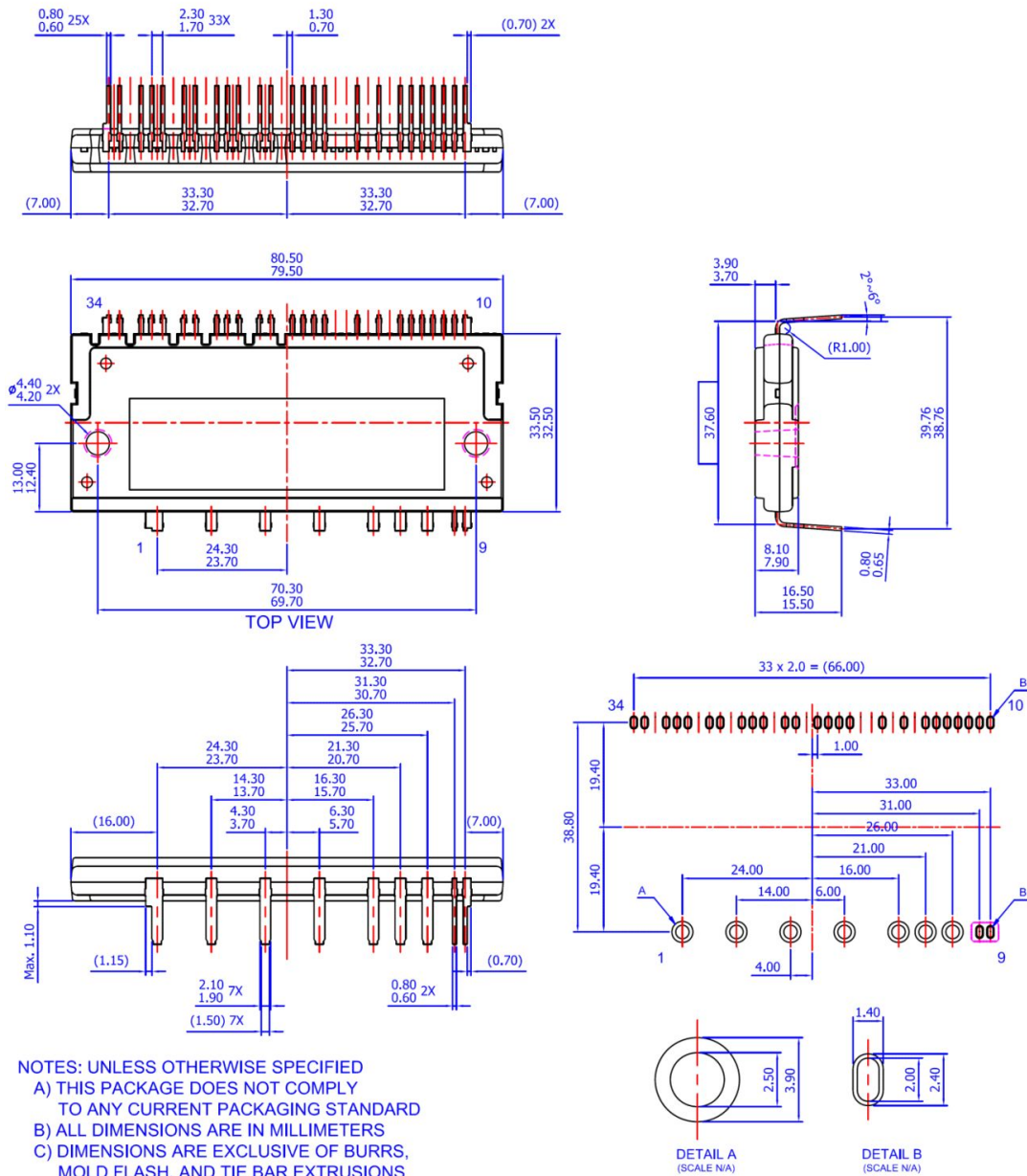


Figure 15. Typical Application Circuit

Notes:

15. To avoid malfunction, the wiring of each input should be as short as possible (less than 2 - 3 cm).
16. V_{FO} output is an open-drain type. This signal line should be pulled up to the positive side of the MCU or control power supply with a resistor that makes I_{FO} up to 2 mA. Please refer to Figure 14.
17. Fault out pulse width can be adjust by capacitor C₅ connected to the C_{FOD} terminal.
18. Input signal is active-HIGH type. There is a 5 kΩ resistor inside the IC to pull-down each input signal line to GND. RC coupling circuits should be adopted for the prevention of input signal oscillation. R₁C₁ time constant should be selected in the range 50 ~ 150 ns (recommended R₁ = 100 Ω, C₁ = 1 nF).
19. Each wiring pattern inductance of point A should be minimized (recommend less than 10 nH). Use the shunt resistor R₄ of surface mounted (SMD) type to reduce wiring inductance. To prevent malfunction, wiring of point E should be connected to the terminal of the shunt resistor R₄ as close as possible.
20. To insert the shunt resistor to measure each phase current at N_U, N_V, N_W terminal, it makes to change the trip level I_{SC} about the short-circuit current.
21. To prevent errors of the protection function, the wiring of points B, C, and D should be as short as possible. The wiring of B between C_{SC} filter and R_{SC} terminal should be divided at the point that is close to the terminal of sense resistor R₅.
22. For stable protection function, use the sense resistor R₅ with resistance variation within 1% and low inductance value.
23. In the short-circuit protection circuit, select the R₆C₆ time constant in the range 1.0 ~ 1.5 μs. R₆ should be selected with a minimum of 10 times larger resistance than sense resistor R₅. Do enough evaluation on the real system because short-circuit protection time may vary wiring pattern layout and value of the R₆C₆ time constant.
24. Each capacitor should be mounted as close to the pins of the Motion SPM® 2 product as possible.
25. To prevent surge destruction, the wiring between the smoothing capacitor C₇ and the P & GND pins should be as short as possible. The use of a high-frequency non-inductive capacitor of around 0.1 ~ 0.22 μF between the P & GND pins is recommended.
26. Relays are used in most systems of electrical equipments in industrial application. In these cases, there should be sufficient distance between the CPU and the relays.
27. The Zener diode or transient voltage suppressor should be adapted for the protection of ICs from the surge destruction between each pair of control supply terminals (recommended Zener diode is 22 V / 1 W, which has the lower Zener impedance characteristic than about 15 Ω).
28. C₂ of around seven times larger than bootstrap capacitor C₃ is recommended.
29. Please choose the electrolytic capacitor with good temperature characteristic in C₃. Choose 0.1 ~ 0.2 μF R-category ceramic capacitors with good temperature and frequency characteristics in C₄.

Detailed Package Outline Drawings (FNA21012A)



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

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