PIC16LF1904/1906/1907 Family Silicon Errata and Data Sheet Clarification

The PIC16LF1904/1906/1907 family devices that you have received conform functionally to the current Device Data Sheet (DS41569**A**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16LF1904/1906/1907 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A2**).

Data Sheet clarifications and corrections start on page 4, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/ debugger or PICkit™ 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16LF1904/ 1906/1907 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	DEVICE ID<13:0>		
	DEV<8:0>(1)	REV<4:0> Silicon Revision(2)	
		A1	A2
PIC16LF1904	01 1100 100	0 0001	0 0010
PIC16LF1906	01 1100 011	0 0001	0 0010
PIC16LF1907	01 1100 010	0 0001	0 0010

Note 1: The Device ID is located in the configuration memory at address 8006h.

2: Refer to the *"PIC16(L)F193X/(L)F194X/LF190X Memory Programming Specification"* (DS41397) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)	
				A1	A2
High-Frequency Internal Oscillator (HFINTOSC)	HFINTOSC Operation	1.1	HFINTOSC Max. VDD at -40°C	X	
Oscillator	HFINTOSC Ready/Stable bit	2.1	Bits remained set to '1' after initial trigger	X	X
Oscillator	Clock Switching	2.2	Clock switching fails	X	X
Oscillator	Oscillator Start-up Timer (OST) bit	2.3	OST bit remains set	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A2**).

1. Module: High-Frequency Internal Oscillator (HFINTOSC)

1.1 HFINTOSC Max. VDD at -40°C

The High-Frequency Internal Oscillator may stop working at -40°C when VDD is 3.6V.

Work around

1. Use the Internal Oscillator (INTOSC) with VDD = 3.5V or less.
2. Operate the device with VDD = 3.0V then, after the High-Frequency Oscillator (HFINTOSC) is operating at speed, increase VDD to 3.6V.

Affected Silicon Revisions

A1	A2						
X							

2. Module: Oscillator

2.1 OSCSTAT bits: HFIOFR and HFIOFS

When HFINTOSC is selected, the HFIOFR and HFIOFS bits will become set when the oscillator becomes ready and stable. Once these bits are set they become “stuck”, indicating that HFINTOSC is always ready and stable. If the HFINTOSC is disabled, the bits fail to be cleared.

Work around

None.

Affected Silicon Revisions

A1	A2						
X	X						

2.2 Clock Switching

When switching clock sources between an INTOSC clock source and an external clock source operating at a different power mode, one corrupted instruction may be executed after the switch occurs.

Work around

When clock switching from an external oscillator clock source, first switch to 16 MHz HFINTOSC. Once running at 16 MHz HFINTOSC, configure IRCF to run at desired frequency.

When clock switching from an INTOSC to an external oscillator clock source, first switch from desired INTOSC frequency to HFINTOSC High-Power mode (8 MHz or 16 MHz). Once running from HFINTOSC, switch to the external oscillator clock source.

Affected Silicon Revisions

A1	A2						
X	X						

2.3 Oscillator Start-up Timer (OST) bit

During the two-speed start-up sequence, the OST is enabled to count 1024 clock cycles. After the count is reached, the OSTS bit is set, the system clock is held low until the next falling edge of the external crystal (LP, XT or HS mode), before switching to the external clock source.

When an external oscillator is configured as the primary clock and Fail-Safe Clock mode is enabled (FCMEN = 1), any of the following conditions will result in the Oscillator Start-up Timer (OST) failing to restart:

- $\overline{\text{MCLR}}$ Reset
- Wake from Sleep
- Clock change from INTOSC to Primary Clock

This anomaly will manifest itself as a clock failure condition for external oscillators which take longer than the clock failure time-out period to start.

Work around

None.

Affected Silicon Revisions

A1	A2						
X	X						

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS41569**A**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (05/2011)

Initial release of this document.

Rev B Document (07/2011)

Added Silicon revision A2.

Rev C Document (01/2012)

Added Modules 2.1, 2.2 and 2.3.

NOTES:

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