

Low Power Consumption Class D Amplifier

9W+9W Analog Input

Class D Speaker Amplifier

BD28412MUV

General Description

BD28412MUV is a 9W+9W stereo (or 18W monaural) class D amplifier, developed for battery equipped speaker systems such as wireless speakers. This IC is incorporated with a precise oscillator to generate multiple switching frequencies that can avoid the AM radio interference. In addition, 2.1Ch audio system can be realized by master and slave operation without beat noise caused by interference between two ICs. Furthermore, this IC achieves lower power consumption that eliminates the need for an external heat sink.

Features

- Analog Differential Input
- Low Standby Current
- Output Feedback Circuitry Prevents Sound Quality Degradation Caused by Power Supply Voltage Fluctuation, Achieves Low Noise and Low Distortion, Eliminates the Need of Large Electrolytic-Capacitors for Decoupling
- Power Limit Function (Linearly-programmable)
- Selectable Switching Frequency (AM Avoidance Function)
- Synchronization Control is Supported (Selectable Master and Slave Operation)
- Parallel BTL (PBTL) is Supported
- Wide Voltage Range ($V_{CC}=4.5V$ to $13V$)
- High Efficiency and Low-heat-generation Make the System Smaller, Thinner, and More Power-saving
- Pop Noise Prevention During Power Supply ON/OFF
- High Reliability Design by Built-in Protection Circuits
 - Overheat Protection
 - Under Voltage Protection
 - Output Short Protection
 - Output DC Voltage Protection
- Small Package (VQFN032V5050) Achieves Mount Area Reduction

Applications

- Wireless Speakers, Small Active Speakers, Portable Audio Equipments, etc.

Key Specifications

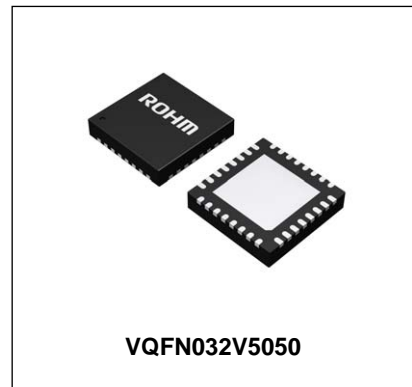
- Supply Voltage Range: 4.5V to 13V
- Speaker Output Power: 9W+9W (Typ)
($V_{CC}=12V, R_L=8\Omega, PLIMIT=0V$)
- Speaker Output Power(PBTL): 18W (Typ)
($V_{CC}=12V, R_L=4\Omega, PLIMIT=0V$)
- Total Harmonic Distortion Ratio: 0.03% (Typ) @ $P_o=1W$
($V_{CC}=11V, R_L=8\Omega, PLIMIT=0V$)
- Crosstalk: 100dB (Typ)
- PSRR: 55dB (Typ)
- Output Noise Voltage: -80dBV (Typ)
- Standby Current: 0.1 μ A (Typ)
- Operating Current: 16mA (Typ)
(No load or filter, No signal)
- Operating Temperature Range: -25°C to +85°C

Package

VQFN032V5050

W(Typ) x D(Typ) x H(Max)

5.00mm x 5.00mm x 1.00mm



Typical Application Circuit

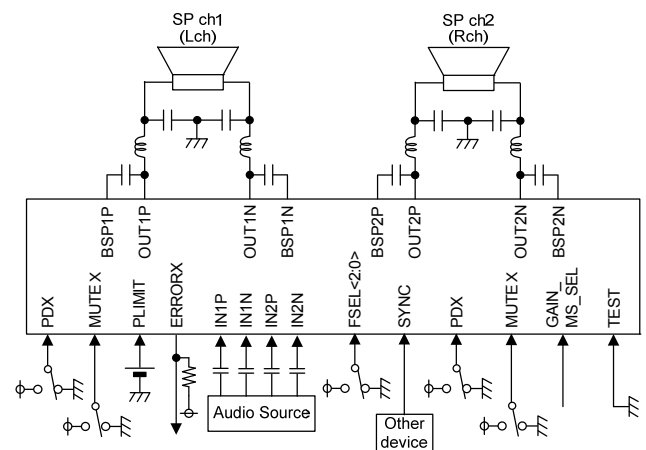


Figure 1. Typical Application Circuit

Pin Configuration

(TOP VIEW)

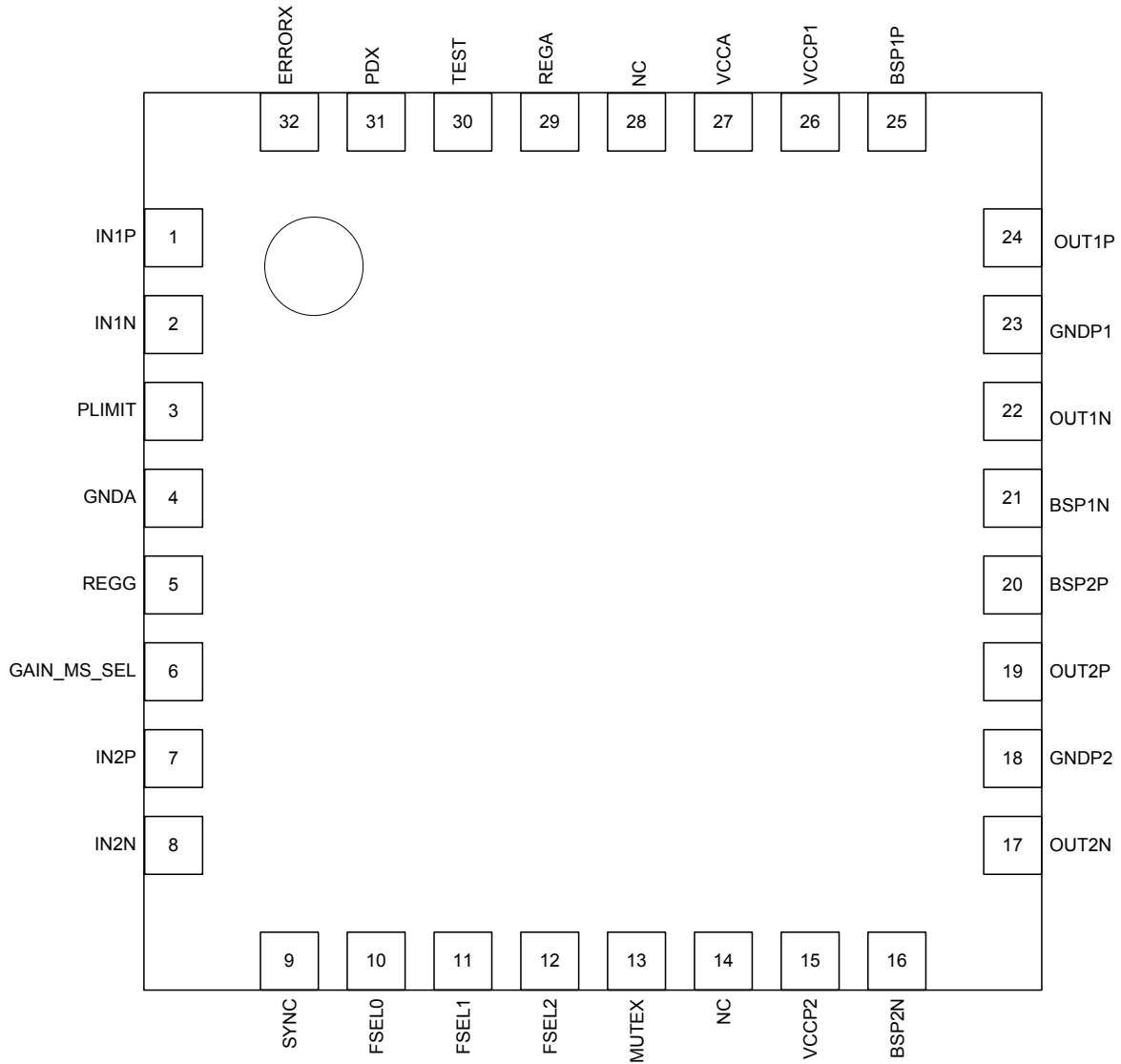


Figure 2. Pin Configuration

Pin Description

Pin No.	Pin Name	IO	Function	Internal Equivalent Circuit
1	IN1P	I	Positive input pin for Ch1	
2	IN1N	I	Negative input pin for Ch1	
3	PLIMIT	I	Power limit level setting pin	
4	GNDA	-	GND pin for Analog signal	
5	REGG	O	Internal power supply pin for Gate driver Please connect a capacitor. The REGG terminal of BD28412MUV should not be used as external supply. Therefore, do not connect anything except the capacitor for stabilization and the resistors for setting of GAIN_MS_SEL and PLIMIT.	
6	GAIN_MS_SEL	I	Gain and Master/Slave mode Setting pin	
7	IN2P	I	Positive input pin for Ch2	
8	IN2N	I	Negative input pin for Ch2	
9	SYNC	I/O	Clock input/output pin to synchronize multiple class D amplifiers	

Pin Description – continued

10	FSEL0	I	PWM frequency setting pin 0	
11	FSEL1	I	PWM frequency setting pin 1	
12	FSEL2	I	PWM frequency setting pin 2	
13	MUTEX	I	Speaker output mute control pin H: Mute OFF L: Mute ON	
14	NC	-	Non connection	
15	VCCP2	-	Power supply pin for Ch2 PWM signal Please connect a capacitor.	
16	BSP2N	O	Boot-strap pin of Ch2 negative PWM signal Please connect a capacitor.	
17	OUT2N	O	Output pin of Ch2 negative PWM signal Please connect to output LPF.	
18	GNDP2	-	GND pin for Ch2 PWM signal	
19	OUT2P	O	Output pin of Ch2 positive PWM signal Please connect to output LPF.	
20	BSP2P	O	Boot-strap pin of Ch2 positive PWM signal Please connect a capacitor.	
21	BSP1N	O	Boot-strap pin of Ch1 negative PWM signal Please connect a capacitor.	
22	OUT1N	O	Output pin of Ch1 negative PWM signal Please connect to output LPF.	
23	GNDP1	-	GND pin for Ch1 PWM signal	
24	OUT1P	O	Output pin of Ch1 positive PWM signal Please connect to output LPF.	
25	BSP1P	O	Boot-strap pin of Ch1 positive PWM signal Please connect a capacitor.	
26	VCCP1	-	Power supply pin for Ch1 PWM signal Please connect a capacitor.	
27	VCCA	-	Power supply pin for Analog signal Please connect a capacitor.	
28	NC	-	Non connection	
29	REGA	O	Internal power supply pin for Gate driver Please connect a capacitor. The REGA terminal of BD28412MUV should not be used as external supply. Therefore, do not connect anything except the capacitor for stabilization.	
30	TEST	I	Test pin Please connect to GND.	

Pin Description – continued

<p>31</p>	<p>PDX</p>	<p>I</p>	<p>Power down setting pin H: Active L: Standby</p>	
<p>32</p>	<p>ERRORX</p>	<p>O</p>	<p>Error flag pin Please connect to pull-up resistor. H: Normal L: Error detected An error flag occurs when Output Short Protection, DC Voltage Protection, or High Temperature Protection is activated. This flag shows IC condition during operation.</p>	

The numerical value of internal equivalent circuit is typical value, not guaranteed value.

Block Diagram

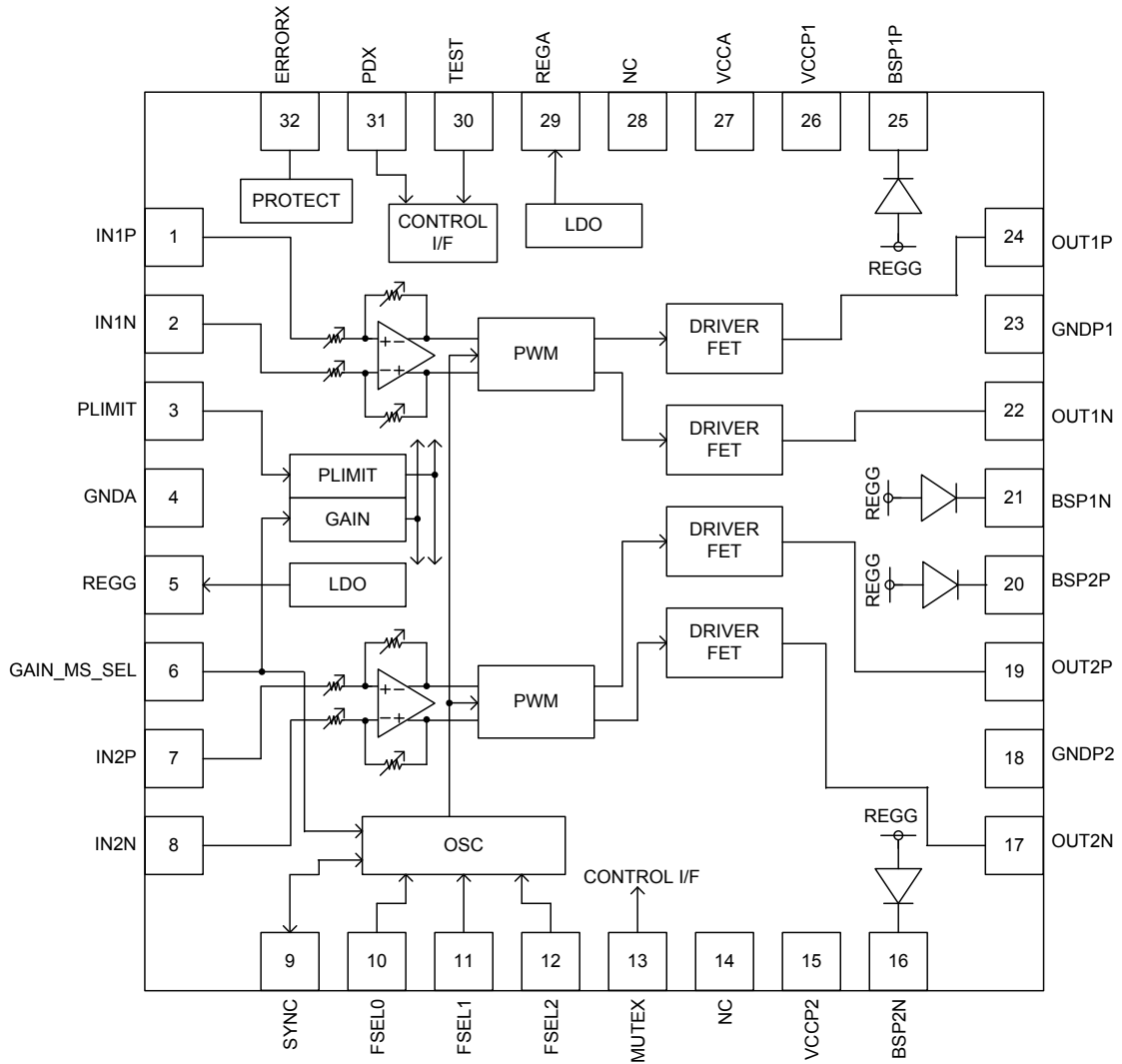


Figure 3. Block Diagram

Absolute Maximum Ratings (Tj = 25°C)

Parameter	Symbol	Rating	Unit	Conditions
Supply Voltage ^(Note 1)	V _{CCMAX}	-0.3 to +15.5	V	VCCA, VCCP1, VCCP2
Input Voltage1 ^(Note 1)	V _{IN}	-0.3 to +7	V	IN1P, IN1N, IN2P, IN2N, PLIMIT, GAIN_MS_SEL, PLIMIT, SYNC ^(Note 2) , FSEL0, FSEL1, FSEL2, PDX, MUTEX
Input Voltage2 ^(Note 1)	V _{ERR}	-0.3 to +7	V	ERRORX
Pin Voltage1 ^{(Note 1) (Note 3)}	V _{PIN1}	-0.3 to +V _{CCMAX}	V	OUT1P, OUT1N, OUT2P, OUT2N
Operating Temperature Range	Topr	-25 to +85	°C	
Storage Temperature Range	Tstg	-55 to +150	°C	
Junction Temperature Range	Tj	-40 to +150	°C	

(Note 1) The voltage that can be applied reference to GND (Pin4, 18, 23).

(Note 2) SYNC pin is I/O pin. It is specified for input mode.

(Note 3) Please use under this rating including the AC peak waveform (overshoot) for all conditions.
Only undershoot is allowed at condition of ≤15.5V by the VCC reference and ≤10nsec (cf. Figure 4)

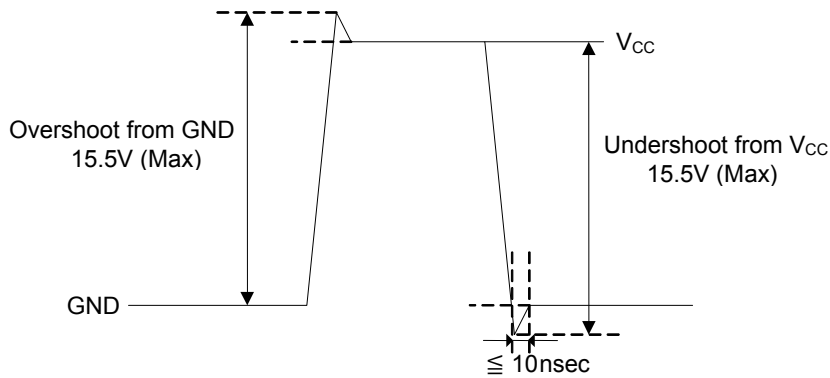


Figure 1. Overshoot and Undershoot

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Thermal Resistance ^(Note 4)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s ^(Note 6)	2s2p ^(Note 7)	
VQFN032V5050				
Junction to Ambient	θ _{JA}	138.9	39.1	°C/W
Junction to Top Characterization Parameter ^(Note 5)	Ψ _{JT}	11	5	°C/W

(Note 4) Based on JESD51-2A(Still-Air)

(Note 5) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 6) Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mm
Copper Pattern Thickness		
Footprints and Traces	70μm	

(Note 7) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size	Thermal Via ^(Note 8)	
			Pitch	Diameter
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mm	1.20mm	Φ0.30mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 μ m	74.2mm x 74.2mm	35 μ m	74.2mm x 74.2mm	70 μ m

(Note 8) This thermal via connects with the copper pattern of all layers..

Use a thermal design that allows for a sufficient margin in consideration of power dissipation under actual operating conditions. This IC exposes its frame at the backside of package. Note that this part is assumed to use after providing heat dissipation treatment to improve heat dissipation efficiency. Try to occupy as wide as possible with heat dissipation pattern not only on the board surface but also the backside.

Recommended Operating Conditions (Ta= -25°C to +85°C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Supply Voltage	V _{IN}	4.5	-	13	V	VCCA, VCCP1, VCCP2
Load Impedance (Note 9)	R _{L1}	5.4	-	-	Ω	BTL
	R _{L2}	3.2	-	-	Ω	PBTL
High Level Input Voltage	V _{IH}	2.0	-	3.3	V	FSEL0, FSEL1, FSEL2, MUTEX, PDX
Low Level Input Voltage	V _{IL}	0	-	0.8	V	FSEL0, FSEL1, FSEL2, MUTEX, PDX
Low Level Output Voltage	V _{OL}	-	-	0.8	V	ERRORX, I _{OL} =0.5mA

(Note 9) T_J<150°C

Electrical Characteristics

(Unless otherwise specified, $T_a=25^{\circ}\text{C}$, $V_{CC}=11\text{V}$, $f_{\text{PWM}}=600\text{kHz}$, $f_{\text{IN}}=1\text{kHz}$, $R_L=8\Omega$, $\text{PDX}=3.3\text{V}$, $\text{MUTEX}=3.3\text{V}$, $\text{PLIMIT}=0\text{V}$,
Gain=26dB, Output LC filter: $L=15\mu\text{H}$, $C=1\mu\text{F}$
when $V_{CC}>11\text{V}$, snubber circuit is added: $C=680\text{pF}$, $R=5.6\Omega$)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Quiescent Standby Current	I_{CC1}	-	0.1	25	μA	No load or filter, PDX=L, MUTEX=L
Quiescent Mute Current	I_{CC2}	-	10	20	mA	No load or filter, PDX=H, MUTEX=L
Quiescent Operating Current	I_{CC3}	-	16	32	mA	No load or filter, No signal, PDX=H, MUTEX=H
Regulator Output Voltage	V_{REGG}	4.45	5.55	6.05	V	PDX=H, MUTEX=H
Input Impedance 1	R_{IN1}	50	-	-	$\text{k}\Omega$	MUTEX, PDX, FSEL0, FSEL1, FSEL2, SYNC(Slave mode only),
Input Impedance 2	R_{IN2}	140	200	260	$\text{k}\Omega$	PLIMIT
Output Power ^(Note 10)	P_{O1}	-	9	-	W	$V_{\text{CC}}=12\text{V}$, THD+N=10%
Gain 1 ^(Note 10)	G_{V1}	19	20	21	dB	$P_{\text{O}}=1\text{W}$, GAIN_MS_SEL= 0V
Gain 2 ^(Note 10)	G_{V2}	25	26	27	dB	$P_{\text{O}}=1\text{W}$, GAIN_MS_SEL= $2/9 \times V_{\text{REGG}}$
Gain 3 ^(Note 10)	G_{V3}	31	32	33	dB	$P_{\text{O}}=1\text{W}$, GAIN_MS_SEL= $3/9 \times V_{\text{REGG}}$
Gain 4 ^(Note 10)	G_{V4}	35	36	37	dB	$P_{\text{O}}=1\text{W}$, GAIN_MS_SEL= $4/9 \times V_{\text{REGG}}$
Total Harmonic Distortion ^(Note 10)	THD	-	0.03	-	%	$P_{\text{O}}=1\text{W}$, BW=AES17
Crosstalk ^(Note 10)	CT	60	100	-	dB	$P_{\text{O}}=1\text{W}$, 1kHz BPF
PSRR ^(Note 10)	PSRR	-	55	-	dB	$V_{\text{RIPPLE}}=0.2 V_{\text{P-P}}$, $f=1\text{kHz}$
Output Noise Voltage ^(Note 10)	V_{NO}	-	-80	-70	dBV	$P_{\text{O}}=0\text{W}$, BW=A-Weight
PWM (Pulse Width Modulation) Frequency	f_{PWM1}	1128	1200	1272	kHz	FSEL2=H, FSEL1=H, FSEL0=H
	f_{PWM2}	940	1000	1060	kHz	FSEL2=H, FSEL1=H, FSEL0=L
	f_{PWM3}	564	600	636	kHz	FSEL2=H, FSEL1=L, FSEL0=H
	f_{PWM4}	470	500	530	kHz	FSEL2=H, FSEL1=L, FSEL0=L
	f_{PWM5}	376	400	424	kHz	FSEL2=L, FSEL1=H, FSEL0=H

(Note 10) The value is specified as typical application. Actual value depends on PCB layout and external components.

Typical Performance Curves

(Unless otherwise specified, $T_a=25^\circ\text{C}$, $V_{CC}=11\text{V}$, $f_{\text{PWM}}=600\text{kHz}$, $f_{\text{IN}}=1\text{kHz}$, $\text{PDX}=3.3\text{V}$, $\text{MUTEX}=3.3\text{V}$, $\text{PLIMIT}=0\text{V}$, $\text{Gain}=26\text{dB}$, Output LC filter: $L=15\mu\text{H}$, $C=1\mu\text{F}$ when $V_{CC}>11\text{V}$, snubber circuit is added: $C=680\text{pF}$, $R=5.6\Omega$)

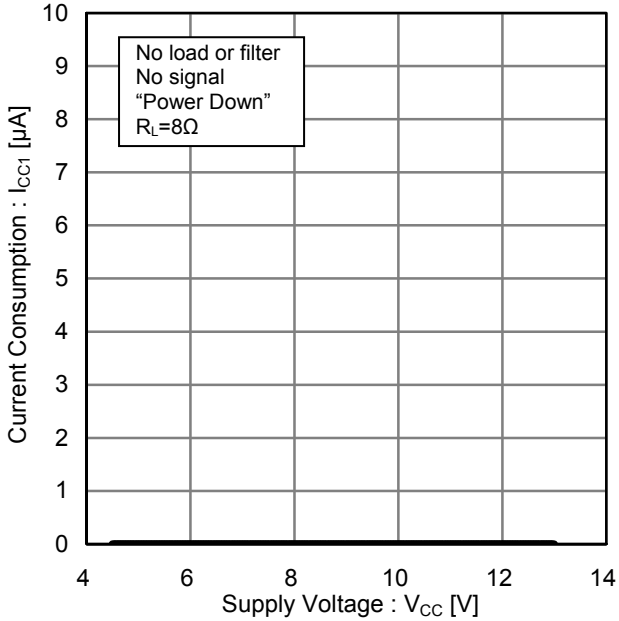


Figure 5. Current Consumption vs Supply Voltage (Power Down)

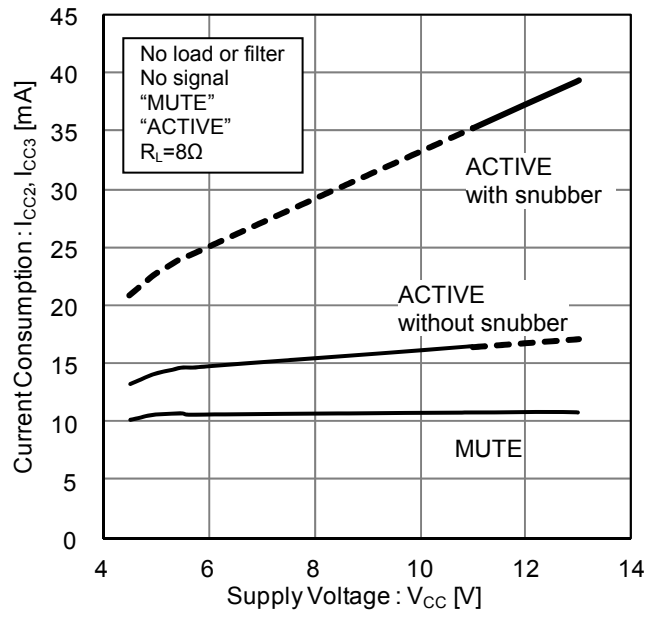


Figure 6. Current Consumption vs Supply Voltage (MUTE, ACTIVE)

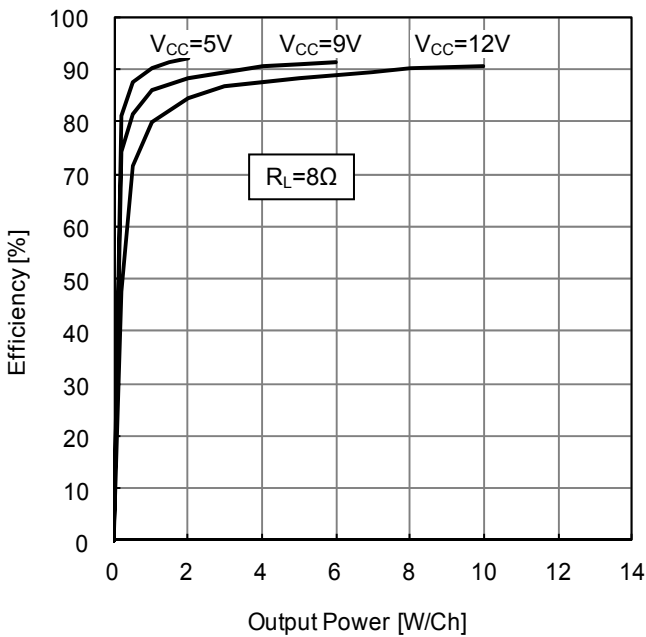


Figure 7. Efficiency vs Output Power ($R_L=8\Omega$)

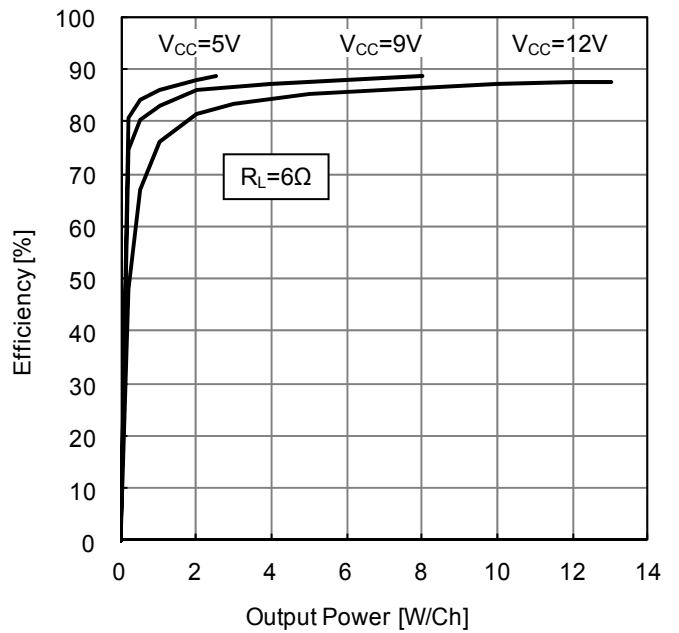


Figure 8. Efficiency vs Output Power ($R_L=6\Omega$)

Typical Performance Curves - continued

(Unless otherwise specified, $T_a=25^\circ\text{C}$, $V_{CC}=11\text{V}$, $f_{PWM}=600\text{kHz}$, $f_{IN}=1\text{kHz}$, $PDX=3.3\text{V}$, $MUTEX=3.3\text{V}$, $PLIMIT=0\text{V}$, $\text{Gain}=26\text{dB}$, Output LC filter: $L=15\mu\text{H}$, $C=1\mu\text{F}$ when $V_{CC}>11\text{V}$, snubber circuit is added: $C=680\text{pF}$, $R=5.6\Omega$)

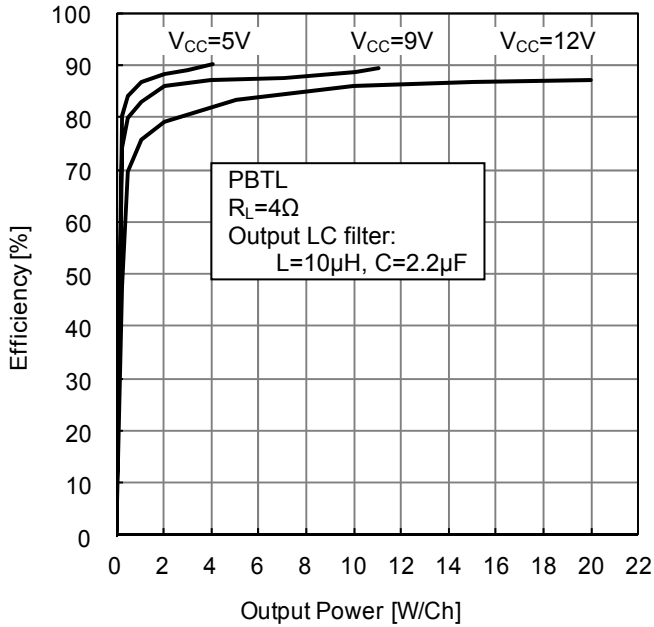


Figure 9. Efficiency vs Output Power (PBTL, $R_L=4\Omega$)

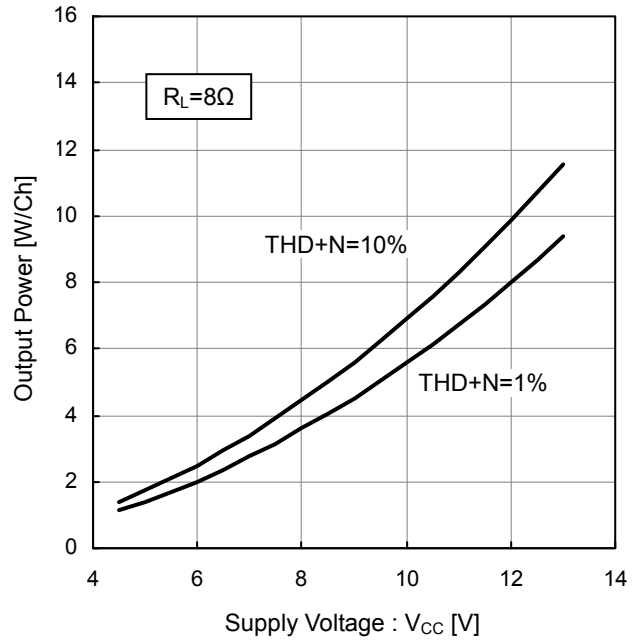


Figure 10. Output Power vs Supply Voltage ($R_L=8\Omega$)

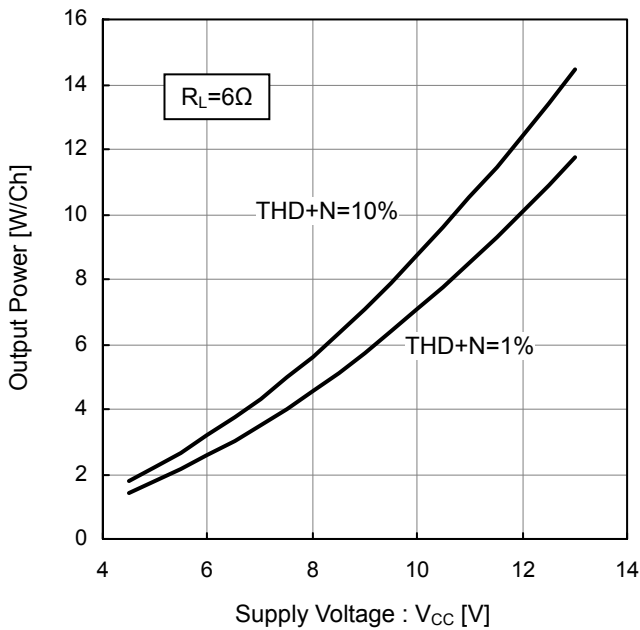


Figure 11. Output Power vs Supply Voltage ($R_L=6\Omega$)

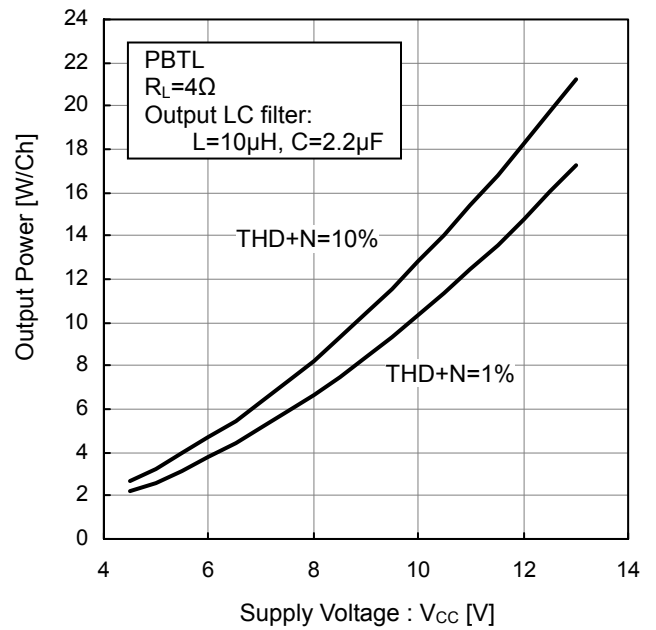


Figure 12. Output Power vs Supply Voltage (PBTL, $R_L=4\Omega$)

Typical Performance Curves - continued

(Unless otherwise specified, $T_a=25^\circ\text{C}$, $V_{CC}=11\text{V}$, $f_{PWM}=600\text{kHz}$, $f_{IN}=1\text{kHz}$, $PDX=3.3\text{V}$, $MUTEX=3.3\text{V}$, $PLIMIT=0\text{V}$, $\text{Gain}=26\text{dB}$, Output LC filter: $L=15\mu\text{H}$, $C=1\mu\text{F}$ when $V_{CC}>11\text{V}$, snubber circuit is added: $C=680\text{pF}$, $R=5.6\Omega$)

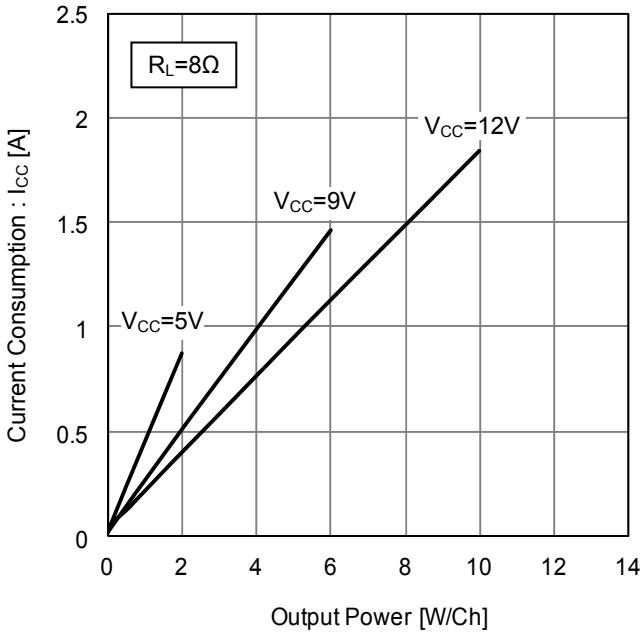


Figure 13. Current Consumption vs Output Power (RL=8Ω)

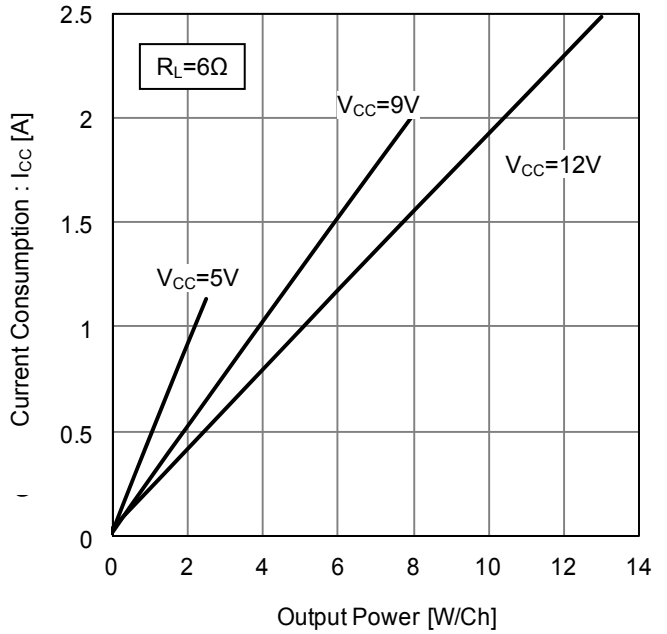


Figure 14. Current Consumption vs Output Power (RL=6Ω)

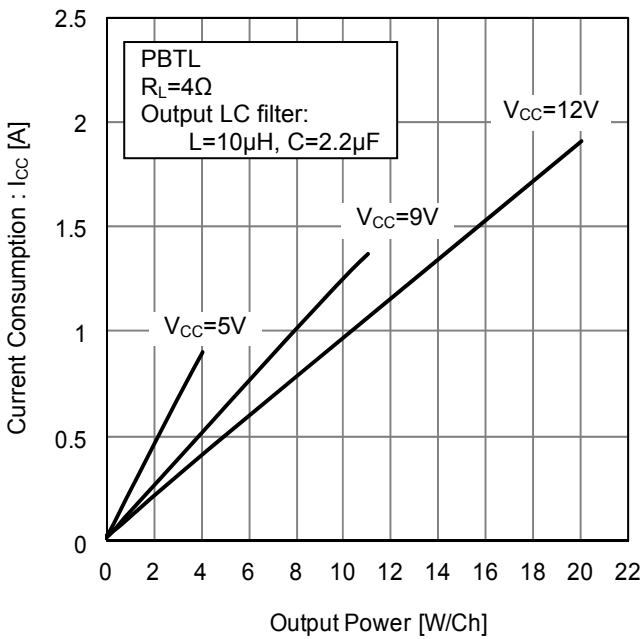


Figure 15. Current Consumption vs Output Power (PBTL, RL=4Ω)

Typical Performance Curves - continued

(Unless otherwise specified, $T_a=25^\circ\text{C}$, $V_{CC}=11\text{V}$, $f_{PWM}=600\text{kHz}$, $f_{IN}=1\text{kHz}$, $P_{DX}=3.3\text{V}$, $MUTEX=3.3\text{V}$, $PLIMIT=0\text{V}$, $\text{Gain}=26\text{dB}$, Output LC filter: $L=15\mu\text{H}$, $C=1\mu\text{F}$ when $V_{CC}>11\text{V}$, snubber circuit is added: $C=680\text{pF}$, $R=5.6\Omega$)

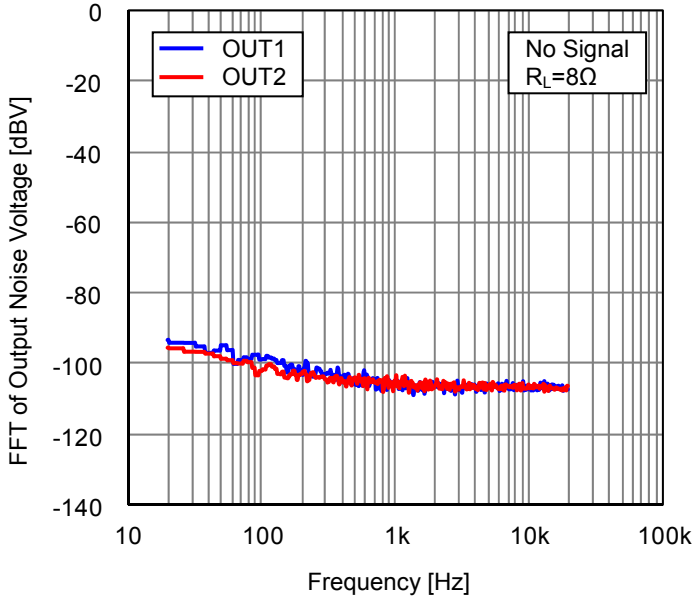


Figure16. FFT of Output Noise Voltage vs Frequency ($R_L=8\Omega$)

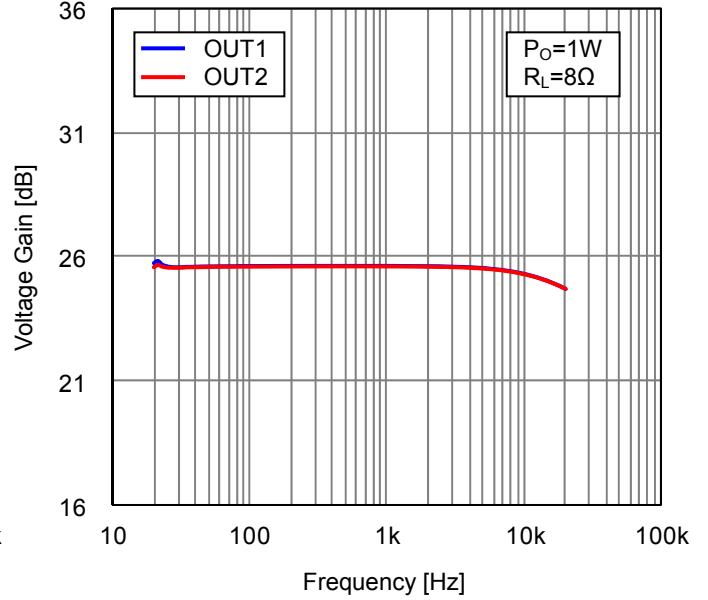


Figure17. Voltage Gain vs Frequency ($R_L=8\Omega$)

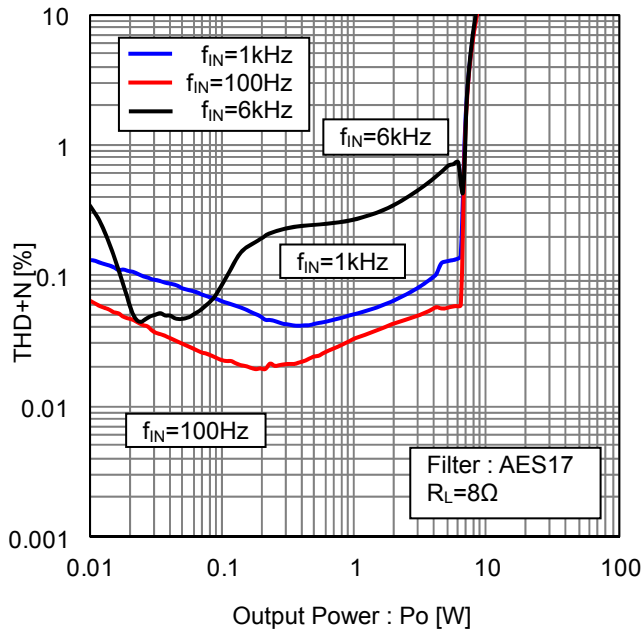


Figure18. THD+N vs Output Power ($R_L=8\Omega$)

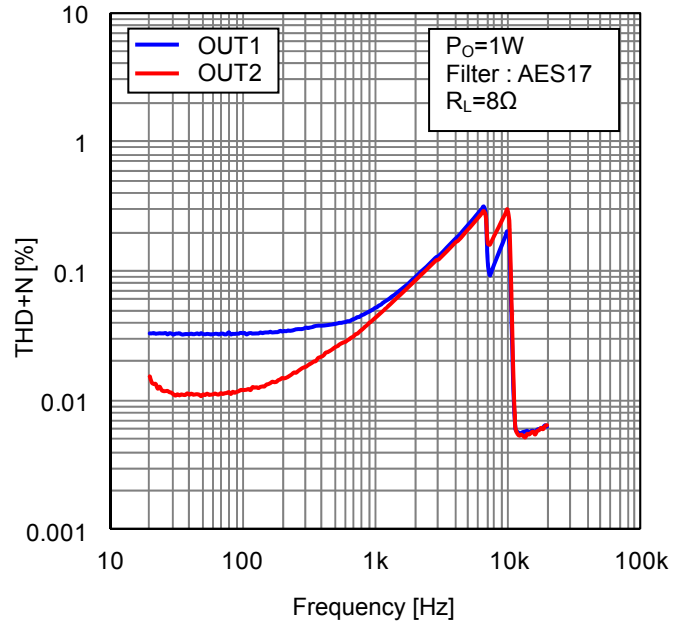


Figure19. THD+N vs Frequency ($R_L=8\Omega$)

Typical Performance Curves - continued

(Unless otherwise specified, $T_a=25^\circ\text{C}$, $V_{CC}=11\text{V}$, $f_{PWM}=600\text{kHz}$, $f_{IN}=1\text{kHz}$, $PDX=3.3\text{V}$, $MUTEX=3.3\text{V}$, $PLIMIT=0\text{V}$, Gain=26dB, Output LC filter: $L=15\mu\text{H}$, $C=1\mu\text{F}$ when $V_{CC}>11\text{V}$, snubber circuit is added: $C=680\text{pF}$, $R=5.6\Omega$)

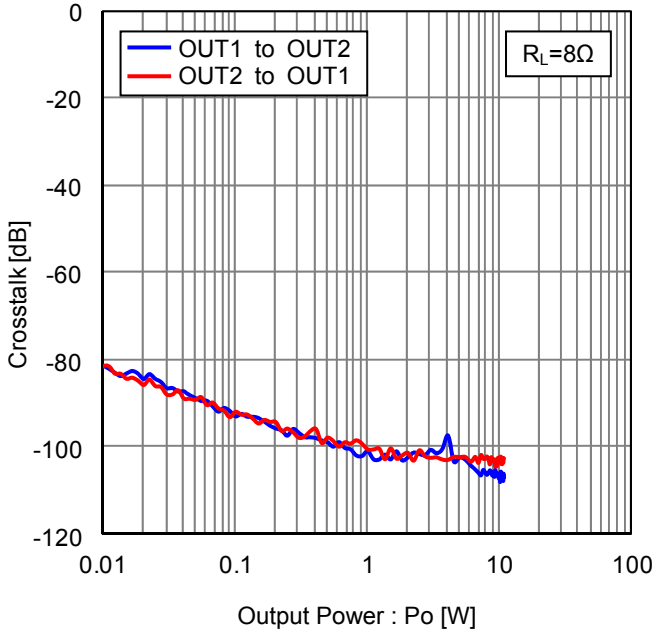


Figure 20. Crosstalk vs Output Power ($R_L=8\Omega$)

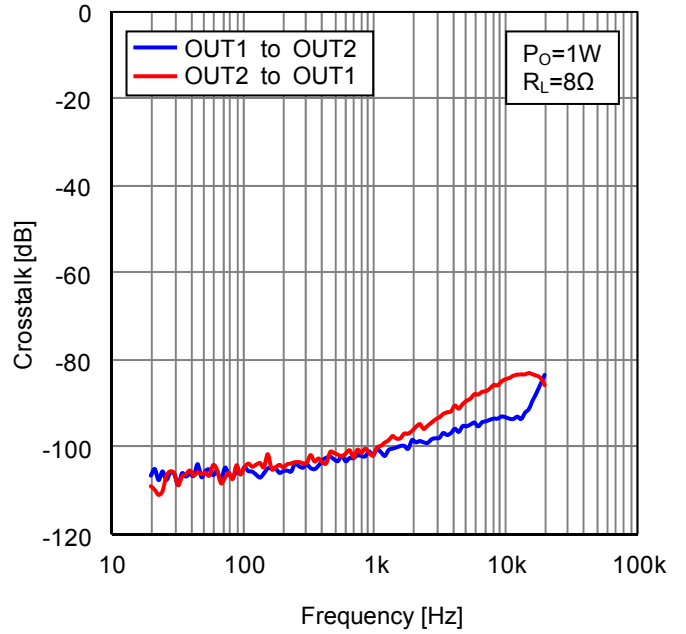


Figure 21. Crosstalk vs Frequency ($R_L=8\Omega$)

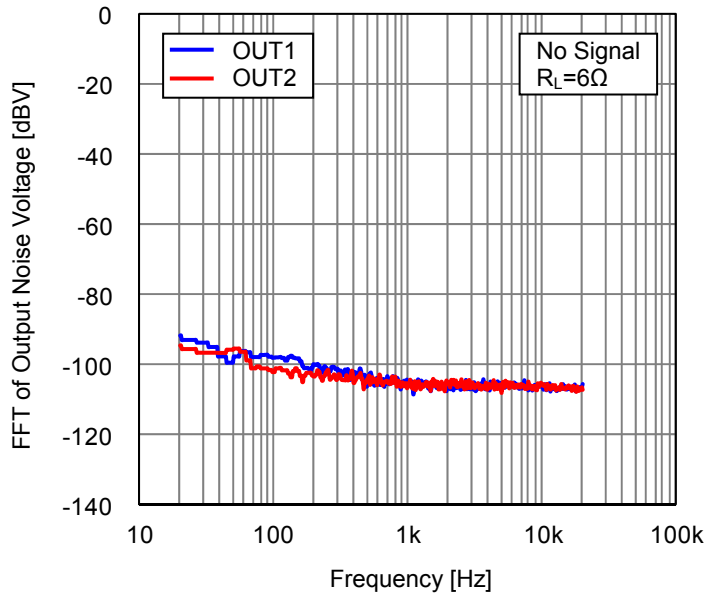


Figure 22. FFT of Output Noise Voltage vs Frequency ($R_L=6\Omega$)

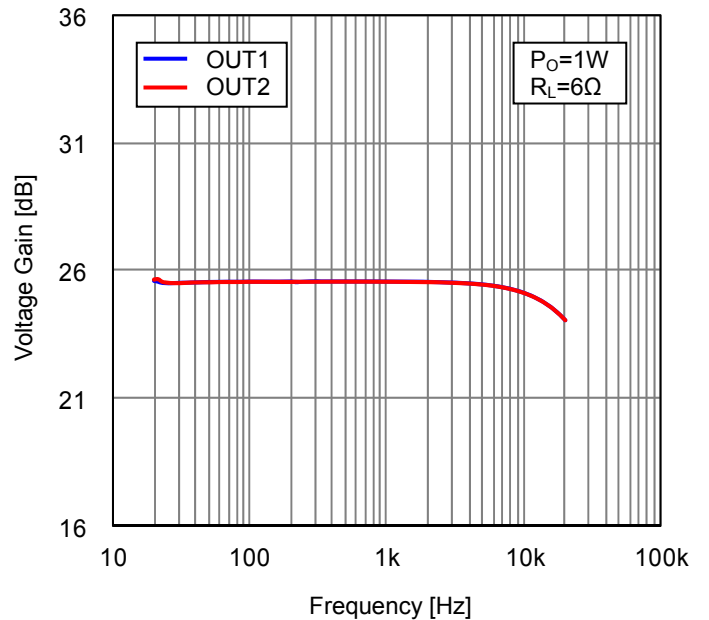


Figure 23. Voltage Gain vs Frequency ($R_L=6\Omega$)

Typical Performance Curves - continued

(Unless otherwise specified, $T_a=25^\circ\text{C}$, $V_{CC}=11\text{V}$, $f_{PWM}=600\text{kHz}$, $f_{IN}=1\text{kHz}$, $PDX=3.3\text{V}$, $MUTEX=3.3\text{V}$, $PLIMIT=0\text{V}$, $\text{Gain}=26\text{dB}$, Output LC filter: $L=15\mu\text{H}$, $C=1\mu\text{F}$ when $V_{CC}>11\text{V}$, snubber circuit is added: $C=680\text{pF}$, $R=5.6\Omega$)

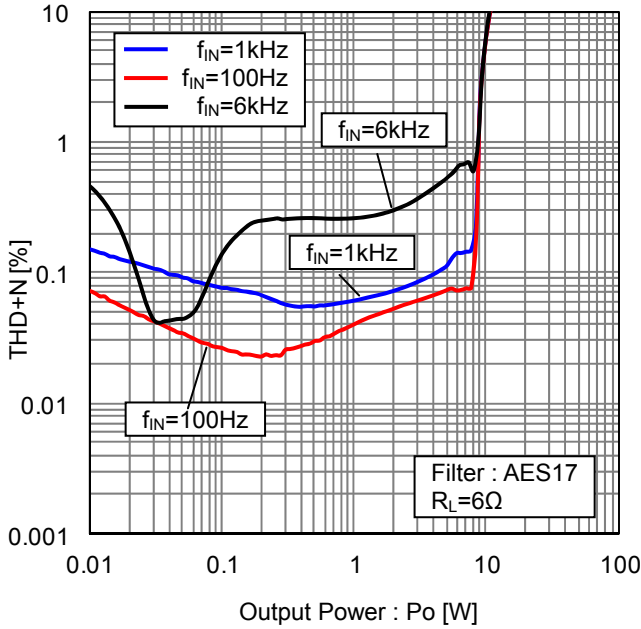


Figure 24. THD+N vs Output Power ($R_L=6\Omega$)

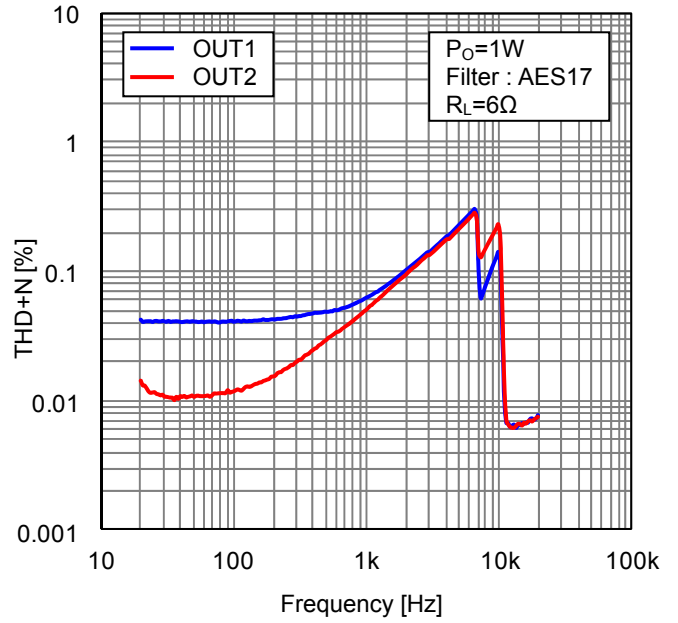


Figure 25. THD+N vs Frequency ($R_L=6\Omega$)

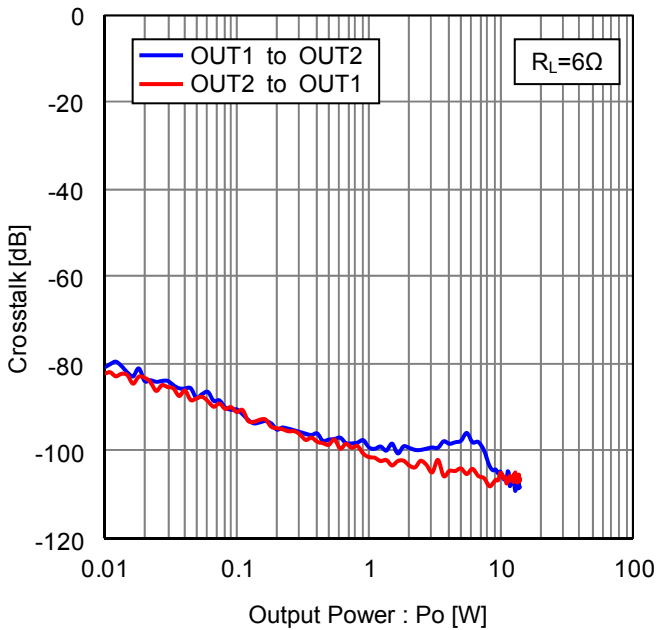


Figure 26. Crosstalk vs Output Power ($R_L=6\Omega$)

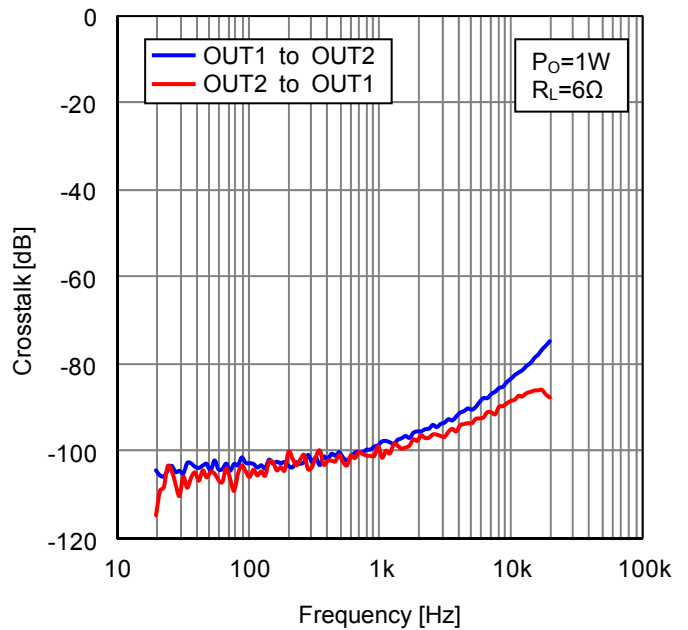


Figure 27. Crosstalk vs Frequency ($R_L=6\Omega$)

Typical Performance Curves - continued

(Unless otherwise specified, $T_a=25^\circ\text{C}$, $V_{CC}=11\text{V}$, $f_{PWM}=600\text{kHz}$, $f_{IN}=1\text{kHz}$, $P_{DX}=3.3\text{V}$, $MUTEX=3.3\text{V}$, $PLIMIT=0\text{V}$, $\text{Gain}=26\text{dB}$, Output LC filter: $L=10\mu\text{H}$, $C=2.2\mu\text{F}$ when $V_{CC}>11\text{V}$, snubber circuit is added: $C=680\text{pF}$, $R=5.6\Omega$)

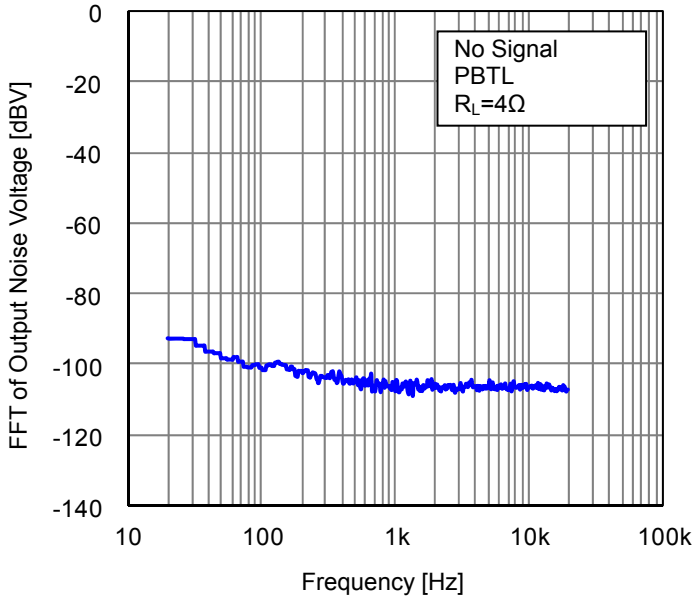


Figure 28. FFT of Output Noise Voltage vs Frequency (PBTL, $R_L=4\Omega$)

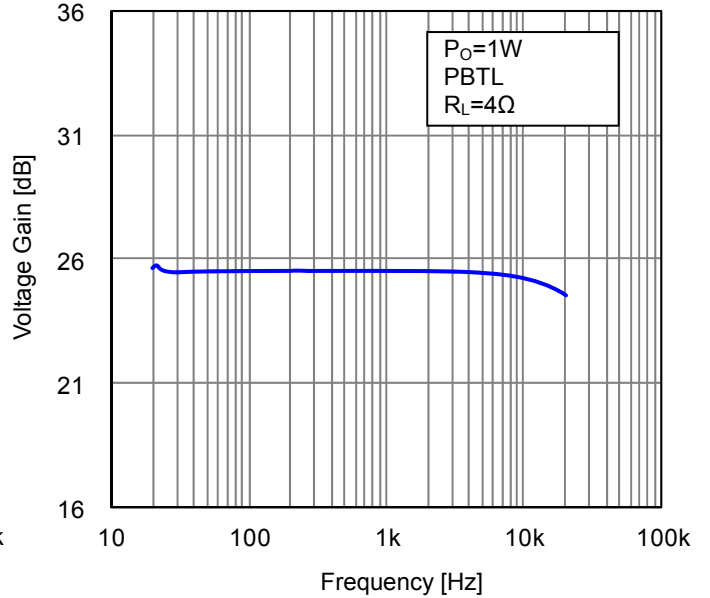


Figure 29. Voltage Gain vs Frequency (PBTL, $R_L=4\Omega$)

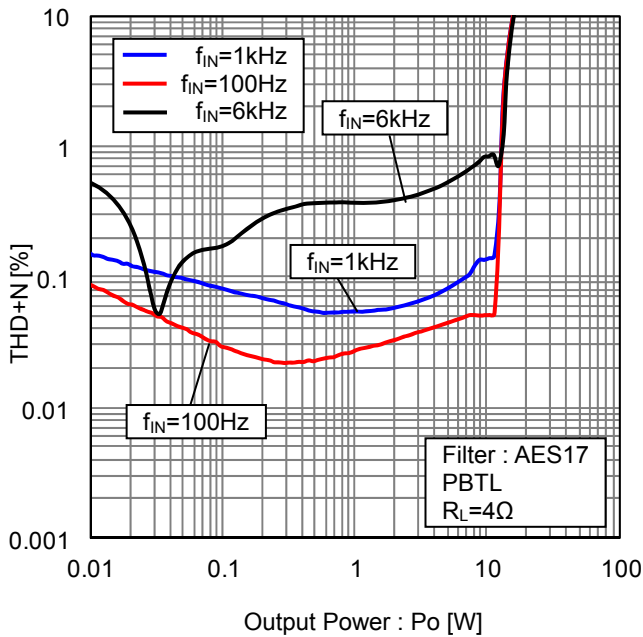


Figure 30. THD+N vs Output Power (PBTL, $R_L=4\Omega$)

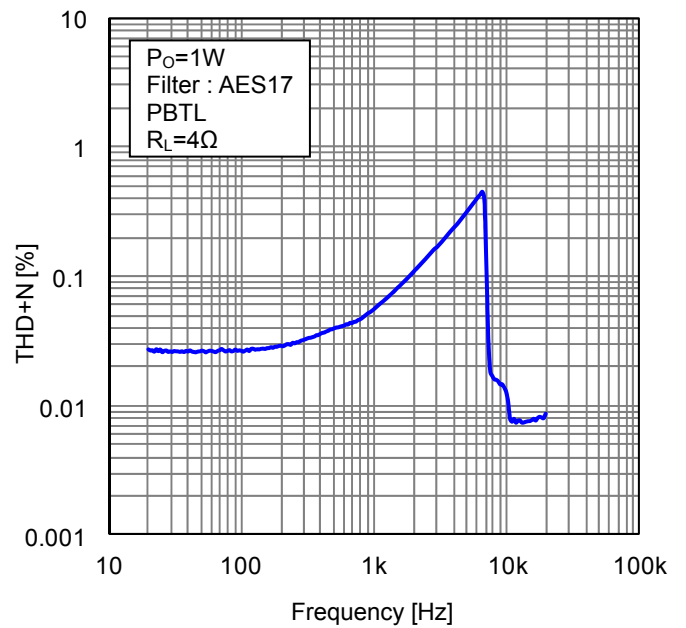


Figure 31. THD+N vs Frequency (PBTL, $R_L=4\Omega$)

Typical Performance Curves - continued

(Unless otherwise specified, $T_a=25^\circ\text{C}$, $V_{CC}=11\text{V}$, $f_{IN}=1\text{kHz}$, $PDX=3.3\text{V}$, $MUTEX=3.3\text{V}$, $PLIMIT=0\text{V}$, $\text{Gain}=26\text{dB}$, Output LC filter: $L=15\mu\text{H}$, $C=1\mu\text{F}$ when $V_{CC}>11\text{V}$, snubber circuit is added: $C=680\text{pF}$, $R=5.6\Omega$)

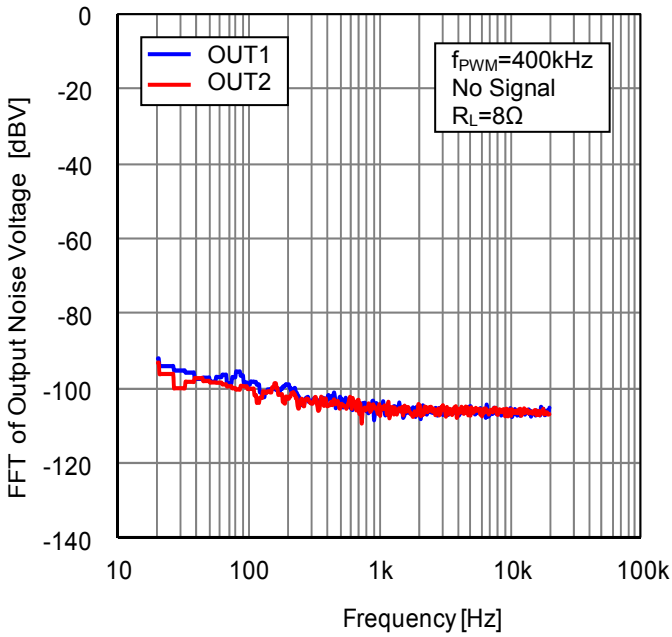


Figure 32. FFT of Output Noise Voltage vs Frequency ($f_{PWM}=400\text{kHz}$, $R_L=8\Omega$)

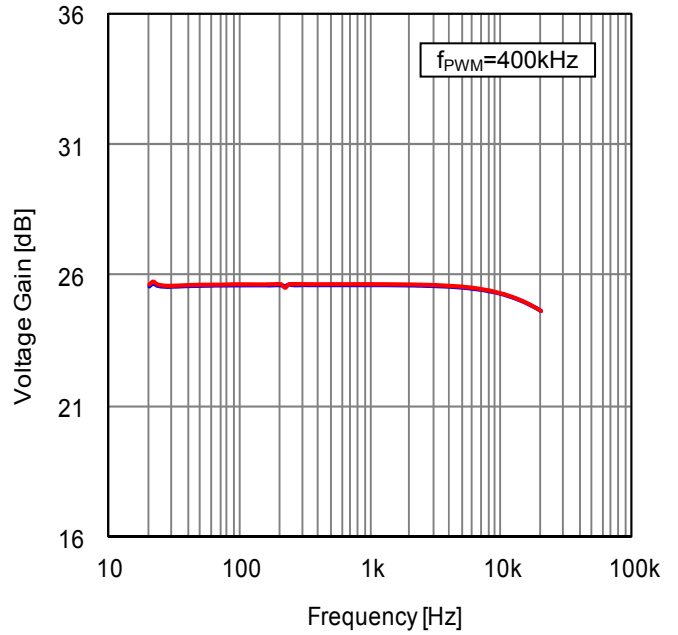


Figure 33. Voltage Gain vs Frequency ($f_{PWM}=400\text{kHz}$, $R_L=8\Omega$)

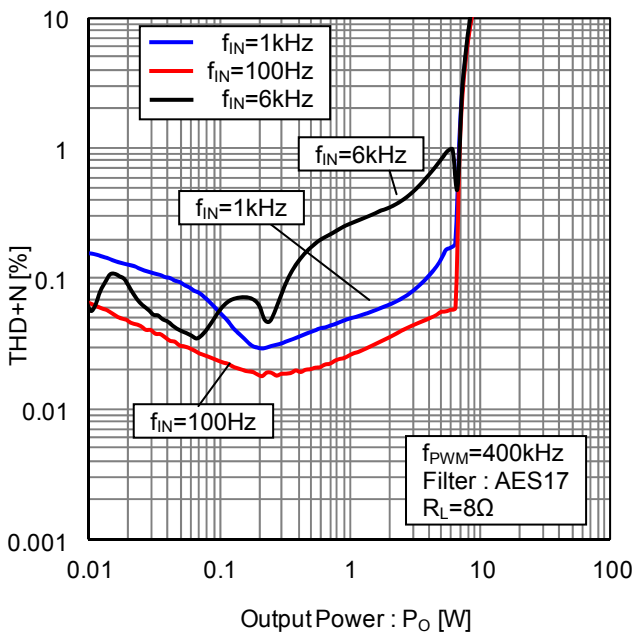


Figure 34. THD+N vs Output Power ($f_{PWM}=400\text{kHz}$, $R_L=8\Omega$)

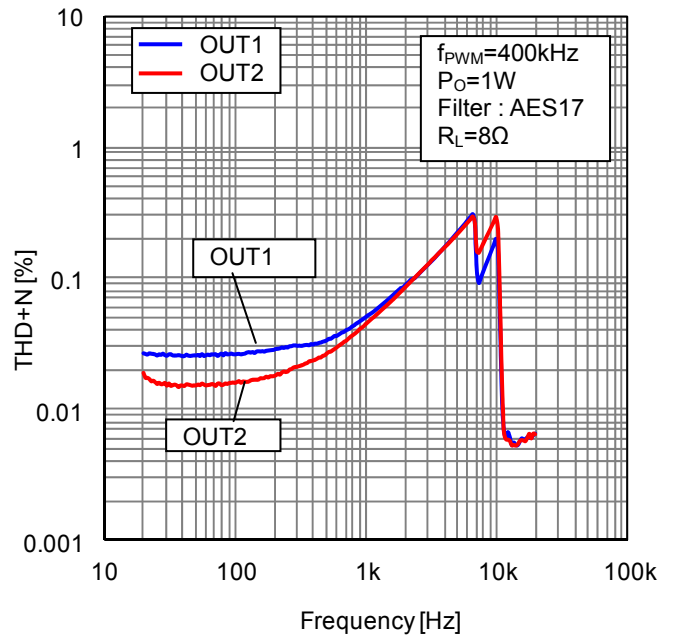


Figure 35. THD+N vs Frequency ($f_{PWM}=400\text{kHz}$, $R_L=8\Omega$)

Typical Performance Curves - continued

(Unless otherwise specified, $T_a=25^\circ\text{C}$, $V_{CC}=11\text{V}$, $f_{IN}=1\text{kHz}$, $PDX=3.3\text{V}$, $MUTEX=3.3\text{V}$, $PLIMIT=0\text{V}$, $\text{Gain}=26\text{dB}$, Output LC filter: $L=15\mu\text{H}$, $C=1\mu\text{F}$ when $V_{CC}>11\text{V}$, snubber circuit is added: $C=680\text{pF}$, $R=5.6\Omega$)

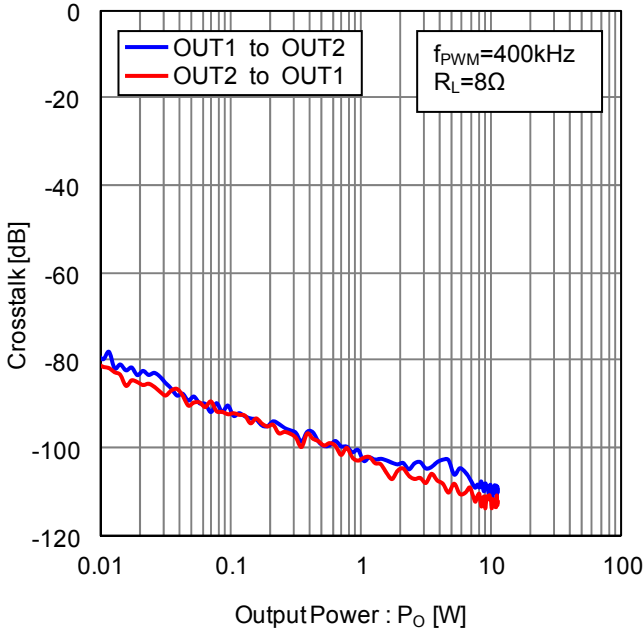


Figure 36. Crosstalk vs Output Power ($f_{PWM}=400\text{kHz}$, $R_L=8\Omega$)

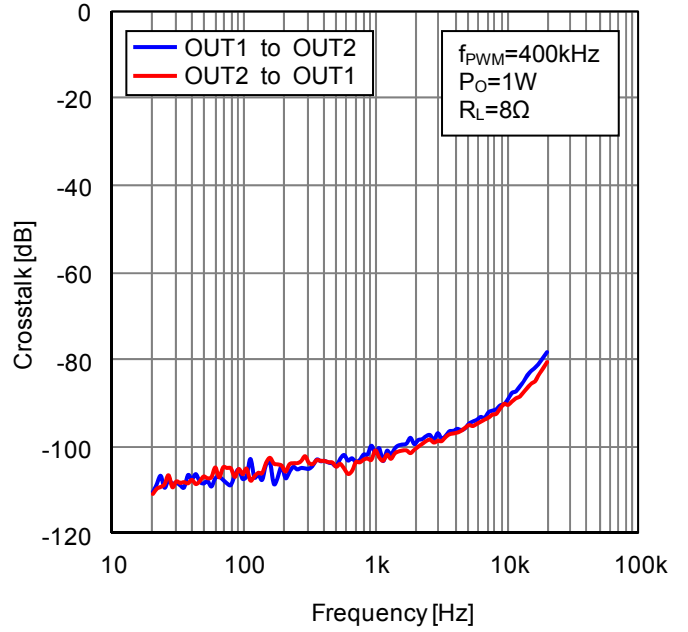


Figure 37. Crosstalk vs Frequency ($f_{PWM}=400\text{kHz}$, $R_L=8\Omega$)

Application Information

1. Power Up / Down Sequence

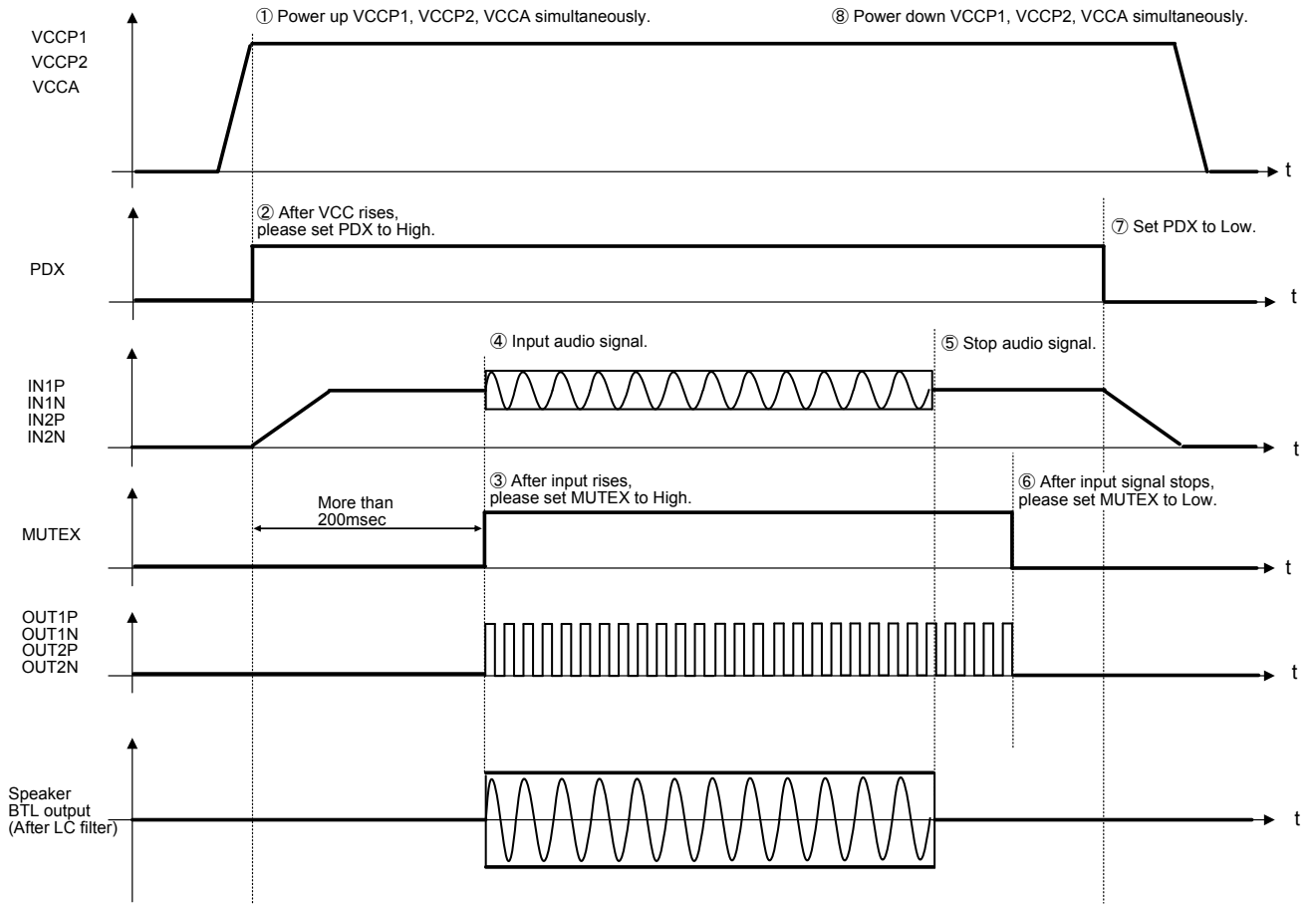


Figure 38. Power Up / Down Sequence

2. Function Description

(1) Power Down and Mute Setting

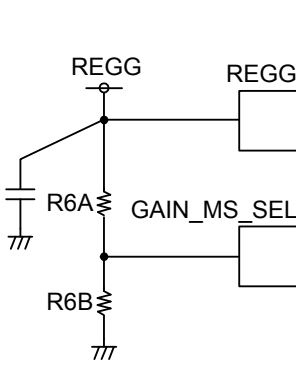
PDX	MUTEX	Normal		ERROR Detection	
		PWM output OUT1P, 1N, 2P, 2N	ERRORX ^(Note 12)	PWM output OUT1P, 1N, 2P, 2N	ERRORX ^(Note 12)
L	L/H	High-Z_Low ^(Note 11) (Power down)	H	High-Z_Low ^(Note 11) (Power down)	H
H	L	High-Z_Low ^(Note 11) (MUTE_ON)	H	High-Z_Low ^(Note 11) (MUTE_ON)	L
H	H	Active (MUTE_OFF)	H	High-Z_Low ^(Note 11) (MUTE_ON)	L

(Note 11) All power transistors are OFF and output terminals are pulled down by 40kΩ (Typ).

(Note 12) ERRORX pin is pulled up by 10kΩ resistor.

(2) Gain and Master/Slave Setting

Master/slave and gain are set by GAIN_MS_SEL pin voltage.



R6A ^(Note 13) (to REGG)	R6B ^(Note 13) (to GND)	Master/Slave	Gain	Input Impedance (IN1P,IN1N,IN2P,IN2N)
18kΩ	Open	Slave	36dB	30kΩ (Typ)
18kΩ	68kΩ	Slave	32dB	45.1kΩ (Typ)
33kΩ	68kΩ	Slave	26dB	79.3kΩ (Typ)
51kΩ	68kΩ	Slave	20dB	127.9kΩ (Typ)
68kΩ	51kΩ	Master	36dB	30kΩ (Typ)
68kΩ	33kΩ	Master	32dB	45.1kΩ (Typ)
68kΩ	18kΩ	Master	26dB	79.3kΩ (Typ)
open	18kΩ	Master	20dB	127.9kΩ (Typ)

(Note 13) Please use 1% tolerance resistor.

Figure 39. GAIN_MS_SEL Pin Setting

Setting cannot be changed when IC is active, but it can be set by rebooting (PDX=H to L to H).

Master/Slave Function

This IC has master and slave mode, and it can be synchronized by PWM frequency between two ICs. In master mode, SYNC pin becomes output pin for synchronization and in slave mode it becomes input pin, thus ensure that each SYNC pins are connected. Also, same setting for FSEL2/FSEL1/FSEL0 pins must be secured.

(3) Parallel BTL Function

Parallel BTL mode can be set by connecting IN2P and IN2N pins to GND.

Please short OUT1P – OUT2P, OUT1N – OUT2N near the IC as much as possible.

Parallel BTL mode cannot be set by connecting IN1P and IN1N pins to GND.

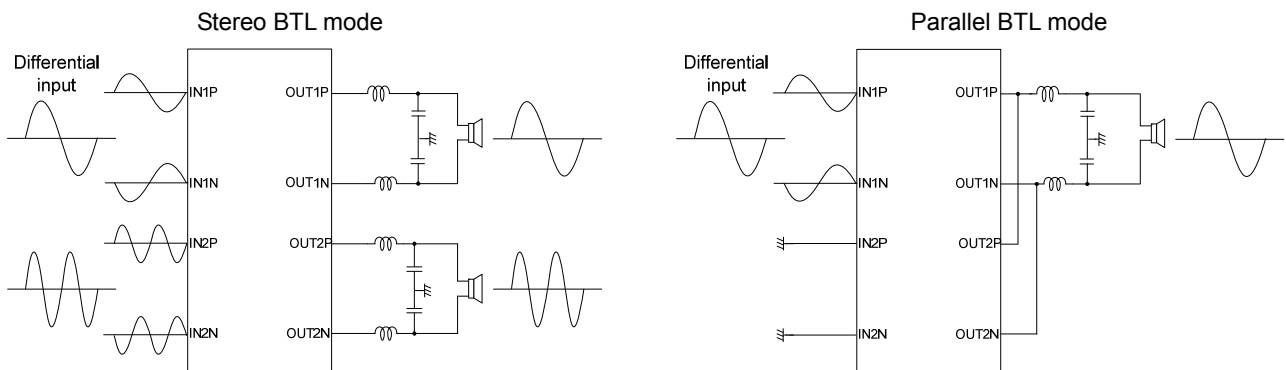


Figure 40. Parallel BTL Mode

(4) Power Limit Function

It is possible to limit the maximum output voltage by PLIMIT pin for protection of speaker.

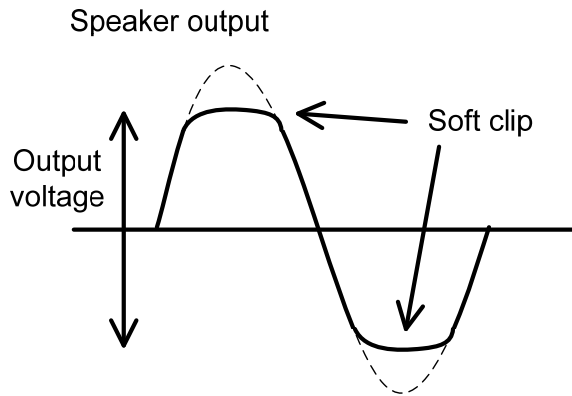


Figure 41. Power Limit

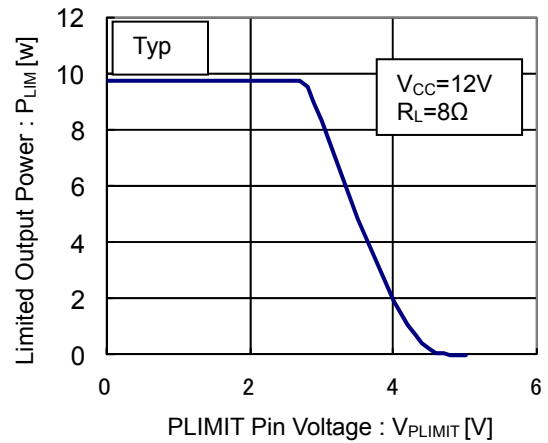


Figure 42. Limited Output Power vs PLIMIT Pin Voltage

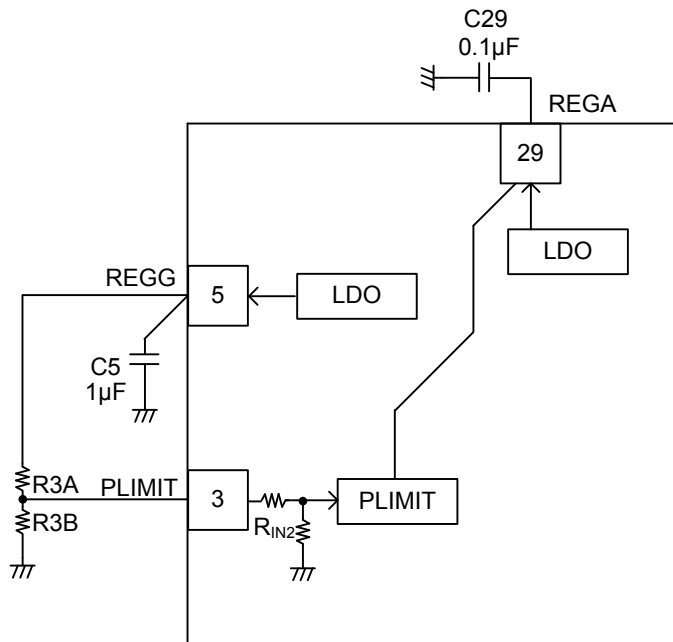


Figure 43. PLIMIT Pin Setting

Output wave is clipped like Figure 37. by applying the DC voltage to 3PIN (PLIMIT), and output power is limited. Figure 41 shows the relation between limited output power P_{LIM} and 3PIN (PLIMIT) pin voltage V_{PLIMIT} . V_{PLIMIT} is set by using external resistance R_{3A} and R_{3B} . Setting examples of R_{3A} and R_{3B} is showed below. If you don't use the power limit function, connect 3PIN (PLIMIT) to GND.

R3A [Ω]	R3B [Ω]	Max output power P_{LIM} [W] ($R_L=8\Omega$)		
		Min	Typ	Max
OPEN	Short to GND	-	(unlimited)	-
12k	20k	3.4	6.8	13.6
10k	20k	2.5	5	10
8.2k	20k	1.7	3.4	6.8

When you use the power limit function in the setting except the table, P_{LIM} is

$$P_{LIM} = \frac{(V_{REGA} - V_{PLIMIT})^2 \times 39.8}{2R_L}$$

$$V_{PLIMIT} = \frac{1}{R_{3A} \left(\frac{1}{R_{3A}} + \frac{1}{R_{3B}} + \frac{1}{R_{IN2}} \right)} V_{REGG}$$

Where:

V_{REGA} is the voltage of 29PIN (REGA), 5V(Typ)

V_{REGG} is the voltage of 5PIN (REGG), 5.55V(Typ)

R_{IN2} is pull-down resistance of 3PIN (PLIMIT), 200kΩ(Typ)

Set the R3A and R3B to become the limited power.

(5) FSEL2 / FSEL1 / FSEL0 (AM avoidance function)

FSEL2 / FSEL1 / FSEL0 pins are used for PWM frequency setting. They can change the PWM frequency like below.

FSEL2	FSEL1	FSEL0	PWM frequency
H	H	H	1200kHz (Typ)
H	H	L	1000kHz (Typ)
H	L	H	600kHz (Typ)
H	L	L	500kHz (Typ)
L	H	H	400kHz (Typ)

Do not set following conditions to become un-recommended frequency:

FSEL2=L, FSEL1=H, FSEL0=L

FSEL2=L, FSEL1=L, FSEL0=H

FSEL2=FSEL1=FSEL0=L

(6) AM avoidance function

PWM frequency is near to AM radio frequency band therefore this makes interference during AM radio is used, and may negatively affects reception of AM radio wave. This interference can be reduced by adjusting PWM frequency. Below are the recommended settings. Example, for receiving AM radio wave of 1269kHz in Asia / Europe, PWM frequency must be set to 500kHz.

AM frequency [kHz]		Recommended PWM frequency setting				
Americas	Asia / Europe	$f_{PWM}=400kHz$ FSEL2=L FSEL1=H FSEL0=H	$f_{PWM}=500kHz$ FSEL2=H FSEL1=L FSEL0=L	$f_{PWM}=600kHz$ FSEL2=H FSEL1=L FSEL0=H	$f_{PWM}=1000kHz$ FSEL2=H FSEL1=H FSEL0=L	$f_{PWM}=1200kHz$ FSEL2=H FSEL1=H FSEL0=H
	522 – 540	○	-	○	○	○
540 – 917	540 – 914	-	○	-	○	○
917 – 1125	914 – 1122	○	-	○	-	○
1125 – 1375	1122 – 1373	-	○	-	○	-
1375 – 1547	1373 – 1548	○	-	○	○	○
1547 – 1700	1548 – 1701	○	-	○	○	○

3. Application Information

(1) Application Circuit Example 1 (Stereo BTL, $V_{CC}=4.5V$ to $11V$)

Overshoot of output PWM differs depending on the board, etc. Ensure that it is lower than absolute maximum ratings. If it exceeds the absolute maximum ratings, snubber circuit need to be added, the circuit example is shown on the next page.

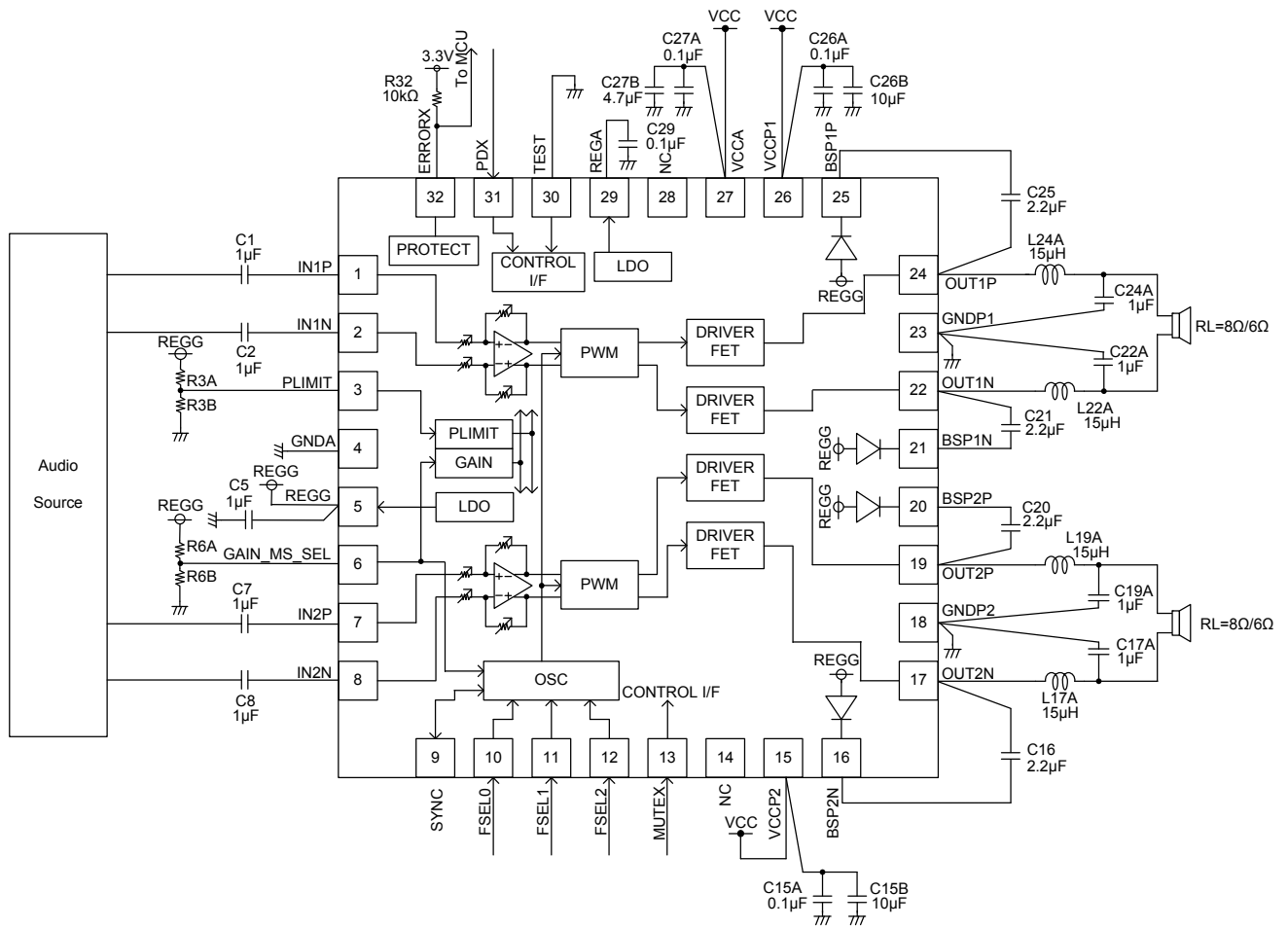


Figure 44. Application Circuit 1

BOM 1 (Stereo BTL, $V_{CC}=4.5V$ to $11V$)

Parts	Qty.	Parts No.	Description
Resistor	1	R3A	Ref. Function Description (4)Power Limit Function
	1	R3B	
	1	R6A	Ref. Function Description (2)Gain and Master/Slave setting
	1	R6B	
	1	R32	
Capacitor	4	C1, C2, C7, C8	1μF, 16V, B(±10%)
	1	C5 ^(Note 14)	1μF, 16V, B(±10%)
	3	C15A, C26A, C27A ^(Note 14)	0.1μF, 25V, B(±10%)
	2	C15B, C26B ^(Note 14)	10μF, 25V, B(±10%)
	4	C16, C20, C21, C25 ^(Note 14)	2.2μF, 16V, B(±10%)
	4	C17A, C19A, C22A, C24A	1μF, 25V, B(±10%)
	1	C27B ^(Note 14)	4.7μF, 25V, B(±10%)
	1	C29 ^(Note 14)	0.1μF, 16V, B(±10%)
Inductor	4	L17A, L19A, L22A, L24A	15μH, 2.1A, ±20%

(Note 14) Please place it near pin as much as possible.

(2) Application Circuit Example 2 (Stereo BTL, $V_{CC}=11V$ to $13V$)
 Please add the snubber circuit at OUT pin when $V_{CC}=11V$ to $13V$.

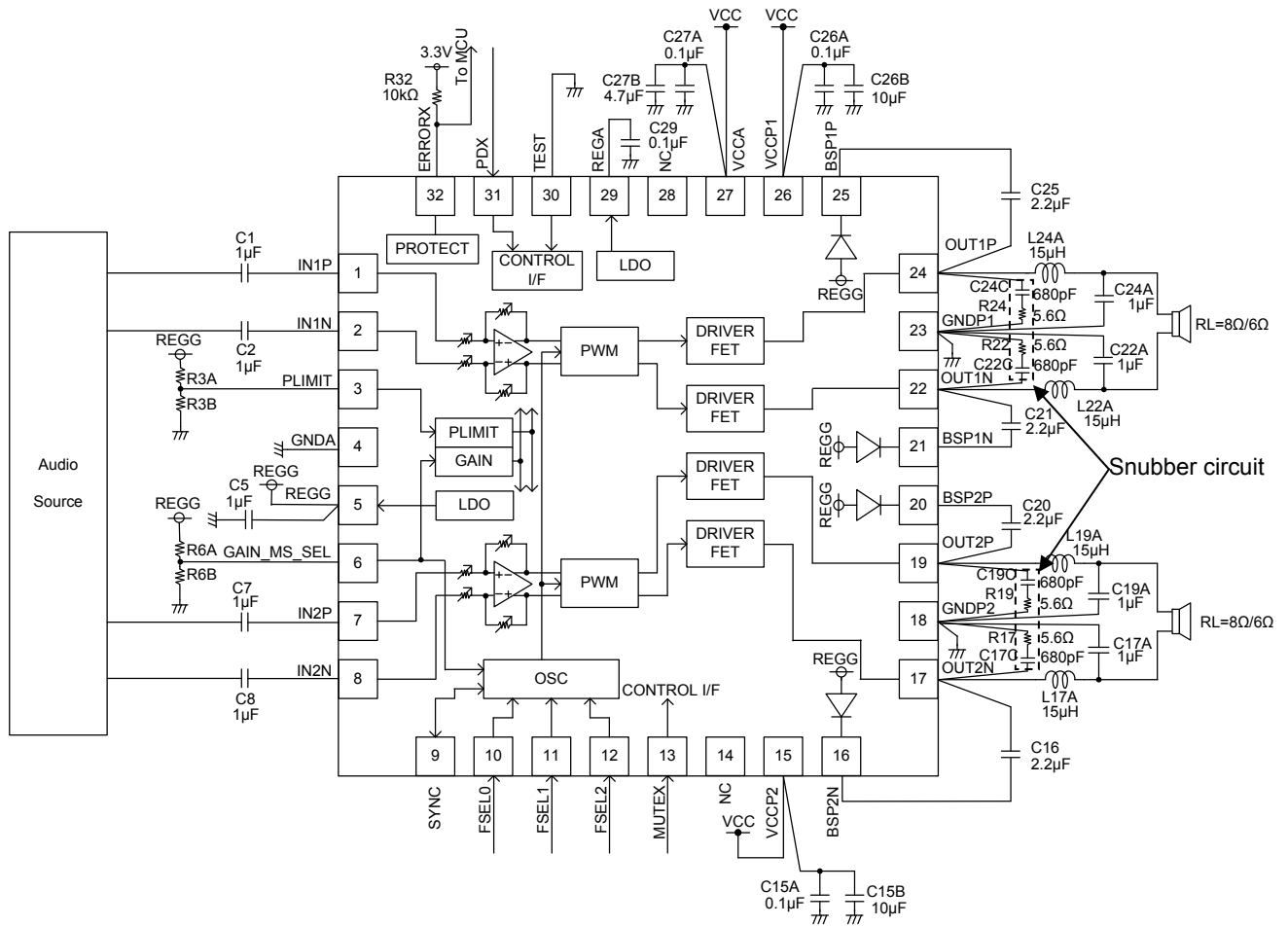


Figure 45. Application Circuit 2

BOM 2 (Stereo BTL, $V_{CC}=11V$ to $13V$)

Parts	Qty.	Parts No.	Description
Resistor	1	R3A	Ref. Function Description (4)Power Limit Function
	1	R3B	
	1	R6A	
	1	R6B	Ref. Function Description (2)Gain and Master/Slave setting
	1	R32	
	4	R17, R19, R22, R24	
Capacitor	4	C1, C2, C7, C8	1 μ F, 16V, B(\pm 10%)
	1	C5 ^(Note 15)	1 μ F, 16V, B(\pm 10%)
	3	C15A, C26A, C27A ^(Note 15)	0.1 μ F, 25V, B(\pm 10%)
	2	C15B, C26B ^(Note 15)	10 μ F, 25V, B(\pm 10%)
	4	C16, C20, C21, C25 ^(Note 15)	2.2 μ F, 16V, B(\pm 10%)
	4	C17A, C19A, C22A, C24A	1 μ F, 25V, B(\pm 10%)
	4	C17C, C19C, C22C, C24C ^(Note 15)	680pF, 25V, B(\pm 10%)
	1	C27B ^(Note 15)	4.7 μ F, 25V, B(\pm 10%)
1	C29 ^(Note 15)	0.1 μ F, 16V, B(\pm 10%)	
Inductor	4	L17A, L19A, L22A, L24A	15 μ H, 2.1A, \pm 20%

(Note 15) Please place it near pin as much as possible.

- (3) Application Circuit Example 3 (Monaural PBTl, $V_{CC}=4.5V$ to $11V$)
 Overshoot of output PWM differs depending on the board, etc. Ensure that it is lower than absolute maximum ratings. If it exceeds the absolute maximum ratings, snubber circuit need to be added, the circuit example is shown on the next page.

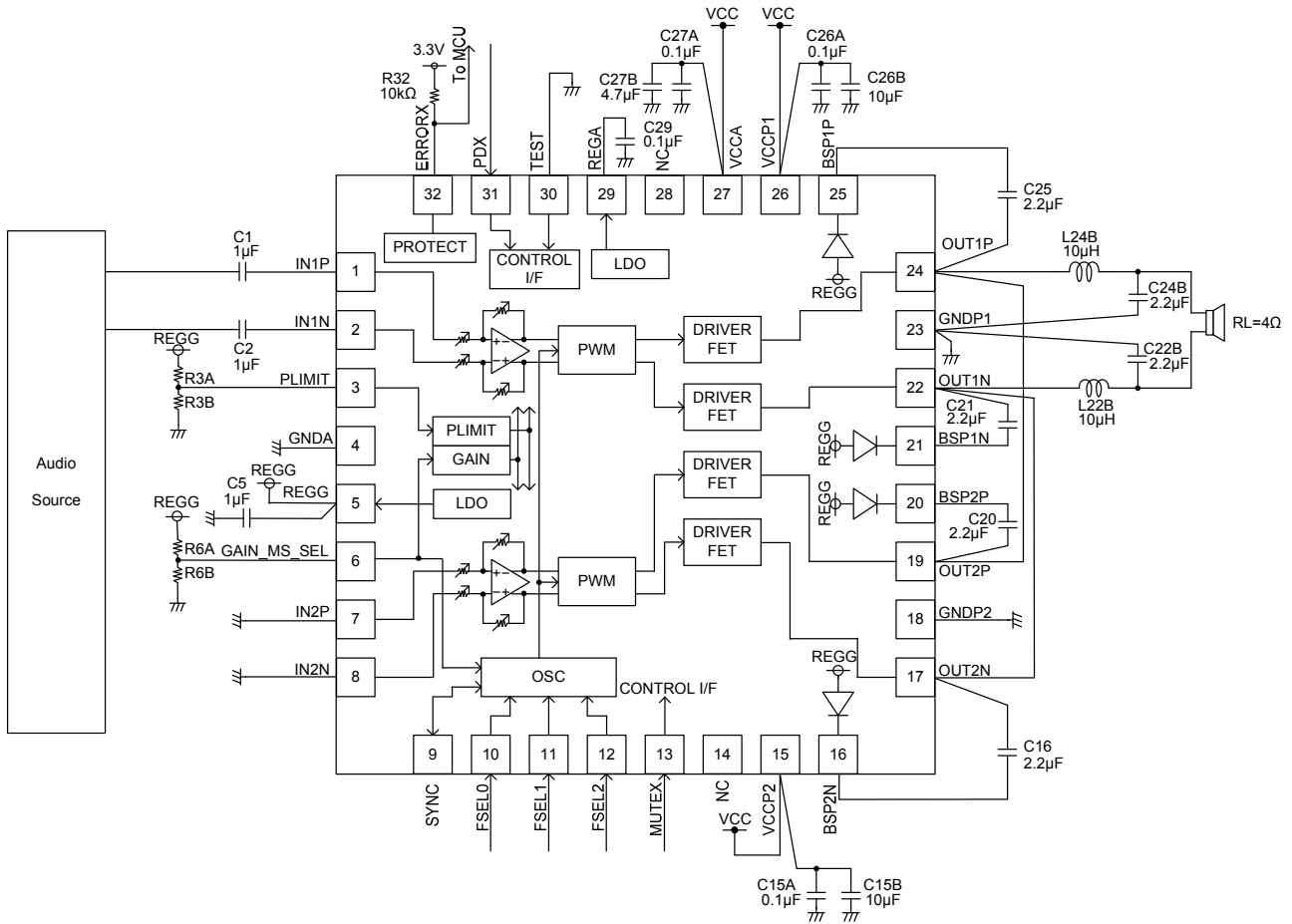


Figure 46. Application Circuit 3

BOM 3 (Monaural PBTl, $V_{CC}=4.5V$ to $11V$)

Parts	Qty.	Parts No.	Description
Resistor	1	R3A	Ref. Function Description (4)Power Limit Function
	1	R3B	
	1	R6A	Ref. Function Description (2)Gain and Master/Slave setting
	1	R6B	
	1	R32	
Capacitor	2	C1, C2	1µF, 16V, B(±10%)
	1	C5 ^(Note 16)	1µF, 16V, B(±10%)
	3	C15A, C26A, C27A ^(Note 16)	0.1µF, 25V, B(±10%)
	2	C15B, C26B ^(Note 16)	10µF, 25V, B(±10%)
	4	C16, C20, C21, C25	2.2µF, 16V, B(±10%)
	2	C22B, C24B ^(Note 16)	2.2µF, 25V, B(±10%)
	1	C27B	4.7µF, 25V, B(±10%)
	1	C29 ^(Note 16)	0.1µF, 16V, B(±10%)
Inductor	2	L22B, L24B	10µH, 2.6A, ±20%

(Note 16) Please place it near pin as much as possible.

(4) Application Circuit Example 4 (Monaural PBTl, $V_{CC}=11V$ to $13V$)
Please add the snubber circuit at OUT pin when $V_{CC}=11V$ to $13V$.

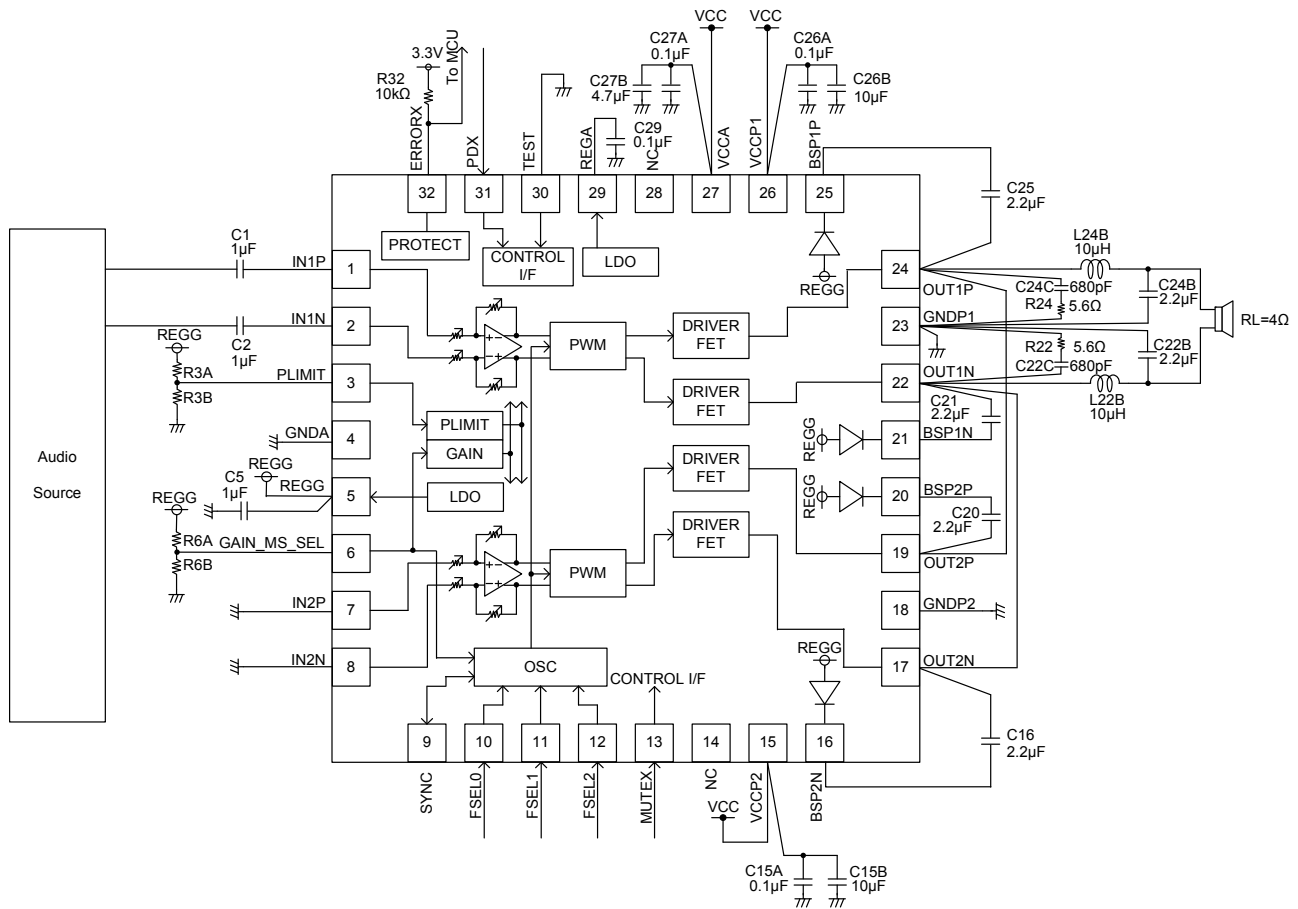


Figure 47. Application Circuit 4

BOM 4 (Monaural PBTl, $V_{CC}=11V$ to $13V$)

Parts	Qty.	Parts No.	Description
Resistor	1	R3A	Ref. Function Description (4)Power Limit Function
	1	R3B	
	1	R6A	Ref. Function Description (2)Gain and Master/Slave setting
	1	R6B	
	1	R32	10kΩ, 1/16W, J(±5%)
	2	R22, R24 ^(Note 17)	5.6Ω, 1/10W, J(±5%)
Capacitor	2	C1, C2	1μF, 16V, B(±10%)
	1	C5 ^(Note 17)	1μF, 16V, B(±10%)
	3	C15A, C26A, C27A ^(Note 17)	0.1μF, 25V, B(±10%)
	2	C15B, C26B ^(Note 17)	10μF, 25V, B(±10%)
	4	C16, C20, C21, C25 ^(Note 17)	2.2μF, 16V, B(±10%)
	2	C22B, C24B	2.2μF, 25V, B(±10%)
	2	C22C, C24C ^(Note 17)	680pF, 25V, B(±10%)
	1	C27B ^(Note 17)	4.7μF, 25V, B(±10%)
1	C29 ^(Note 17)	0.1μF, 16V, B(±10%)	
Inductor	2	L22B, L24B	10μH, 2.6A, ±20%

(Note 17) Please place it near pin as much as possible.

(5) Application Example 5 (MASTER/SLAVE mode, $V_{CC}=4.5V$ to $11V$)

This GAIN_MS_SEL setting is one example, so another Gain setting can be used.

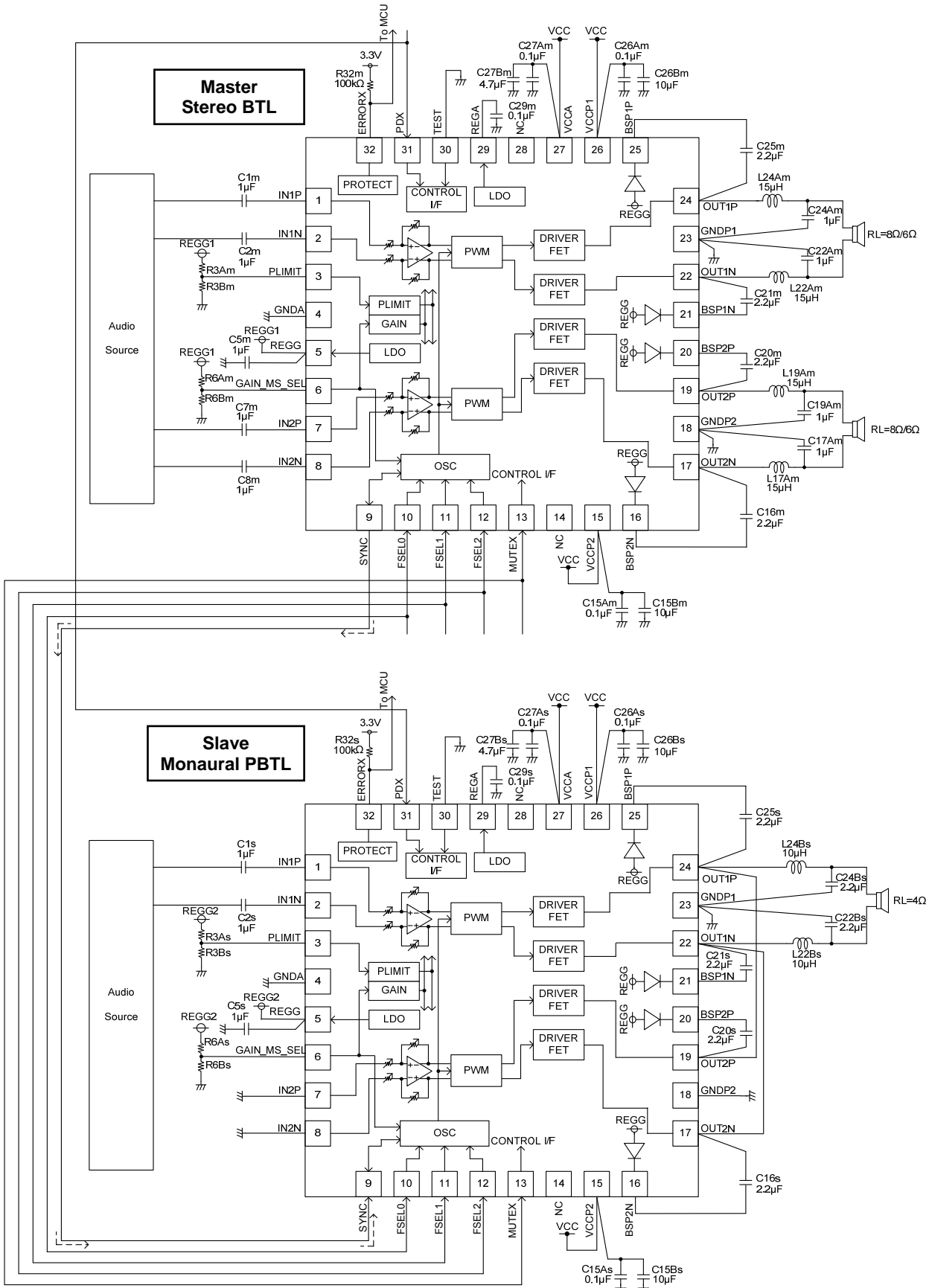


Figure 48. Application Circuit 5

4. About the Protection Function

Protection Function	Detecting & Releasing Condition		PWM Output OUT1P, 1N, 2P, 2N	ERRORX ^(Note 18)
Output short protection	Detecting condition	Detecting current = 8A (Typ)	High-Z_Low (Latch) ^(Note19)	L (Latch) ^(Note19)
DC voltage protection	Detecting condition	DC voltage is over $\pm 3.5V$ (Typ) for a period of 0.33sec to 0.66sec (Typ) at speaker output	High-Z_Low (Latch) ^(Note19)	L (Latch) ^(Note19)
Overheat protection	Detecting condition	Chip temperature to be over 150°C (Typ)	High-Z_Low	L
	Releasing condition	Chip temperature to be below 120°C (Typ)	Normal operation	
Under voltage protection	Detecting condition	Power supply voltage to be below 4.0V (Typ)	High-Z_Low	H
	Releasing condition	Power supply voltage to be above 4.1V (Typ)	Normal operation	

(Note 18) ERRORX pin is pulled up by 10k Ω resistor.

(Note 19) Once an IC is latched, the circuit is not released automatically even after an abnormal status is gone.

The following procedures ① or ② is available for recovery.

① After turning MUTEX terminal to Low (holding time to Low = 10msec (Min)) turn back to High again.

② Restore power supply after dropping to power supply voltage $V_{CC} < 3V$ (10msec (Min) holding) which internal power on reset circuit activates.

(1) Output Short Protection (Short to the Power Supply)

This IC has PWM output short protection circuit that stops the PWM output when the output speaker (after LC-filter) is short-circuited to the power supply unintentionally.

Detecting condition - It will detect when MUTEX pin is set High and the current that flows into the PWM output pin becomes 8A(Typ) or more for 250nsec (Typ). If detected, the PWM output instantaneously goes to the state of High-Z_Low and IC is latch.

Releasing method - ① After turning MUTEX terminal to Low (holding time to Low = 10msec(Min)), turn back to High again.

② Restore power supply after the voltage dropped to internal power on reset circuit activating power supply voltage $V_{CC} < 3V$ (hold for 10msec (Min)).

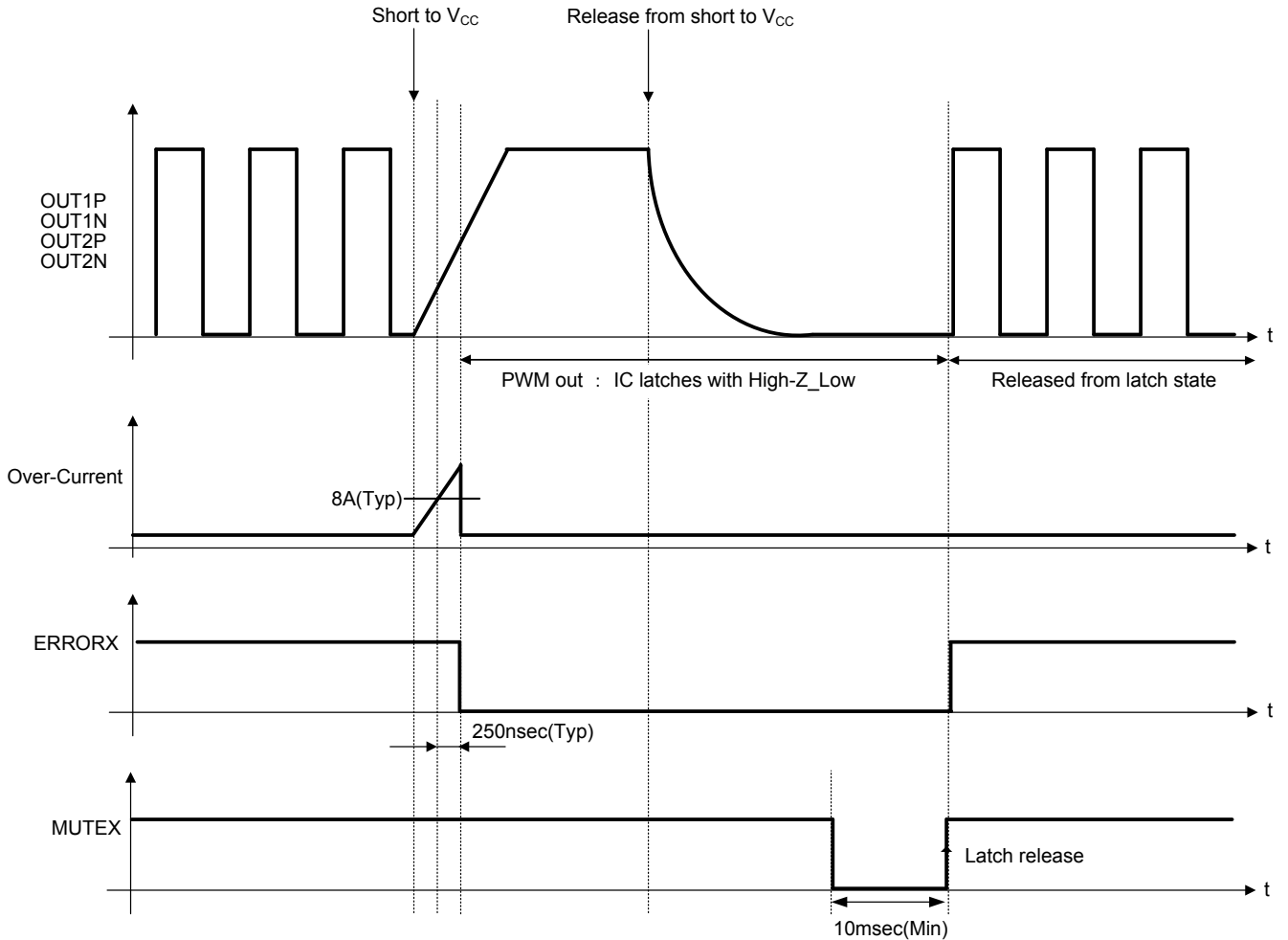


Figure 49. Output Short Protection Sequence (Short to Power Supply)

(2) Output Short Protection (Short to GND)

This IC has PWM output short protection circuit that stops the PWM output when the output speaker (after LC-filter) is short-circuited to GND unintentionally.

Detecting condition - It will detect when MUTE_X pin is set High and the current that flows into the PWM output terminal becomes 8A(Typ) or more for 250nsec (Typ). If detected, the PWM output instantaneously goes to the state of High-Z_{Low} and IC is latched.

Releasing method - ① After turning MUTE_X terminal to Low (holding time to Low = 10msec(Min)), turn back to High again.

② Restore power supply after the voltage dropped to internal power on reset circuit activating power supply voltage $V_{CC} < 3V$ (hold for 10msec (Min)).

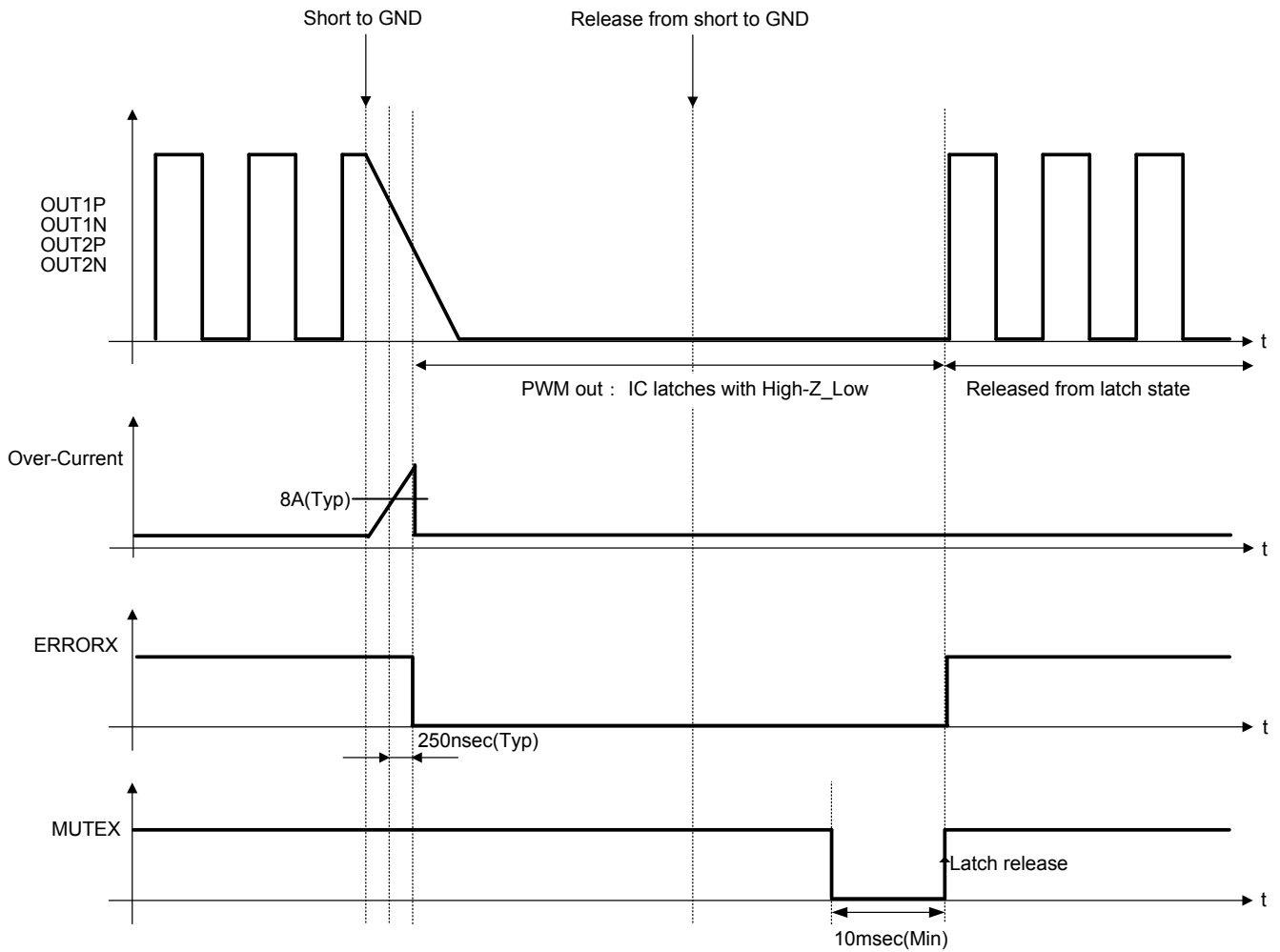


Figure 50. Sequence of the Output Short Protection (Short to GND)

(3) DC Voltage Protection

This IC is integrated with DC voltage protection circuit. When DC voltage is apply to the speaker unintentionally, speaker output will mute, and this protection will prevent the speaker from destruction.

Detecting condition - It will detect when MUTEX pin is set High and speaker output is more than $\pm 3.5V$ (Typ) over 0.33sec to 0.66sec(Typ).

Once detected, The PWM output instantaneously goes to the state of High-Z_Low, and IC will latch.

Releasing method - ① After turning MUTEX terminal to Low (holding time to Low = 10msec(Min)), turn back to High again.

② Restore power supply after the voltage dropped to internal power on reset circuit activating power supply voltage $V_{CC} < 3V$ (hold for 10msec (Min)).

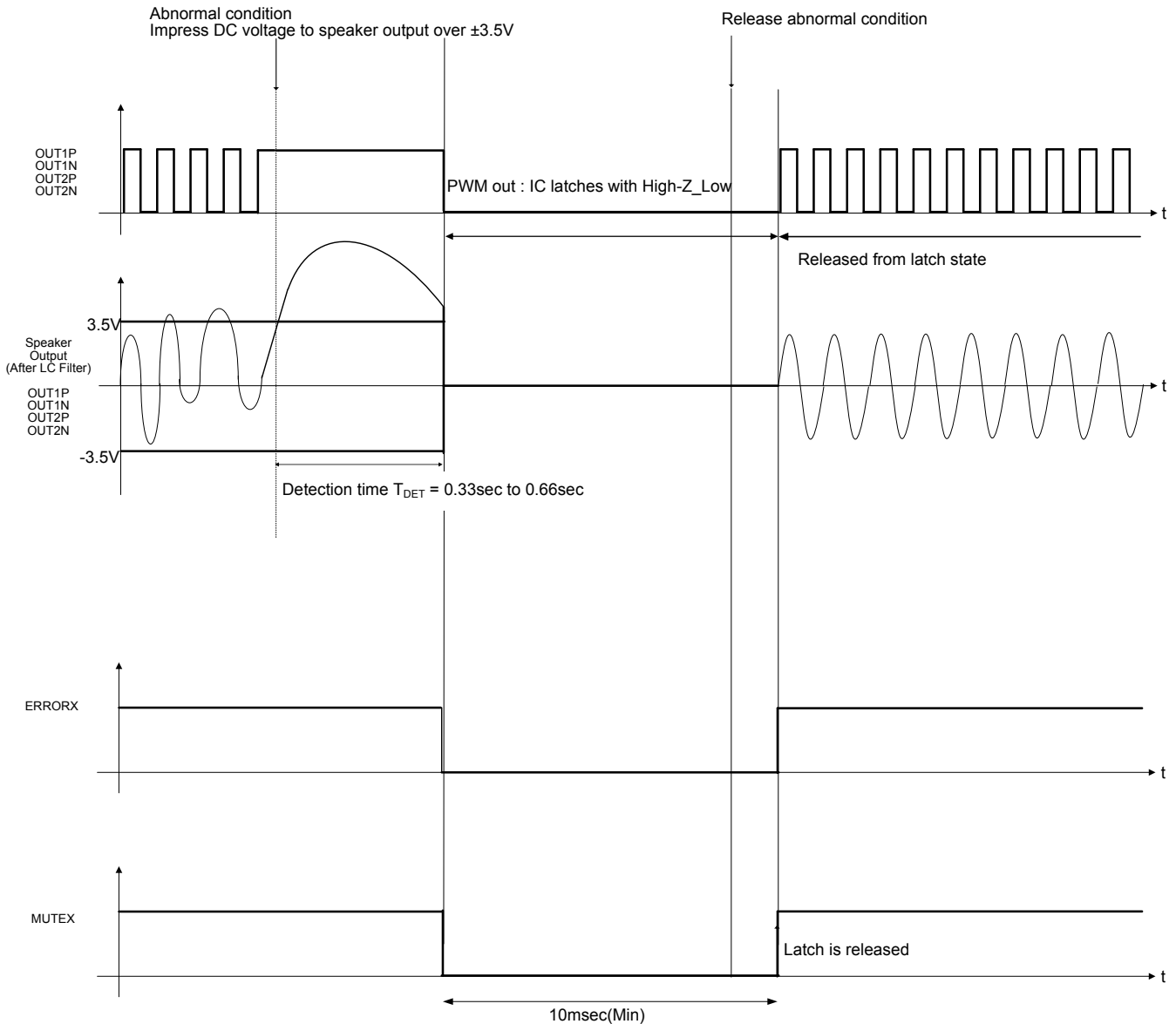


Figure 51. DC Voltage Protection Sequence

(4) Overheat Protection

This IC has overheat protection circuit that prevents thermal runaway under an abnormal state for the chip temperature exceeded $T_{jmax}=150^{\circ}\text{C}$.

Detecting condition - It will detect when MUTEX pin is set High and the temperature of the chip becomes 150°C (Typ) or more. Speaker output mutes immediately when High temperature protection is activated.

Releasing condition - It will release when MUTEX pin is set High and the temperature of the chip becomes 120°C (Typ) or less. The speaker output is back to its normal operation immediately when released. (Auto recovery)

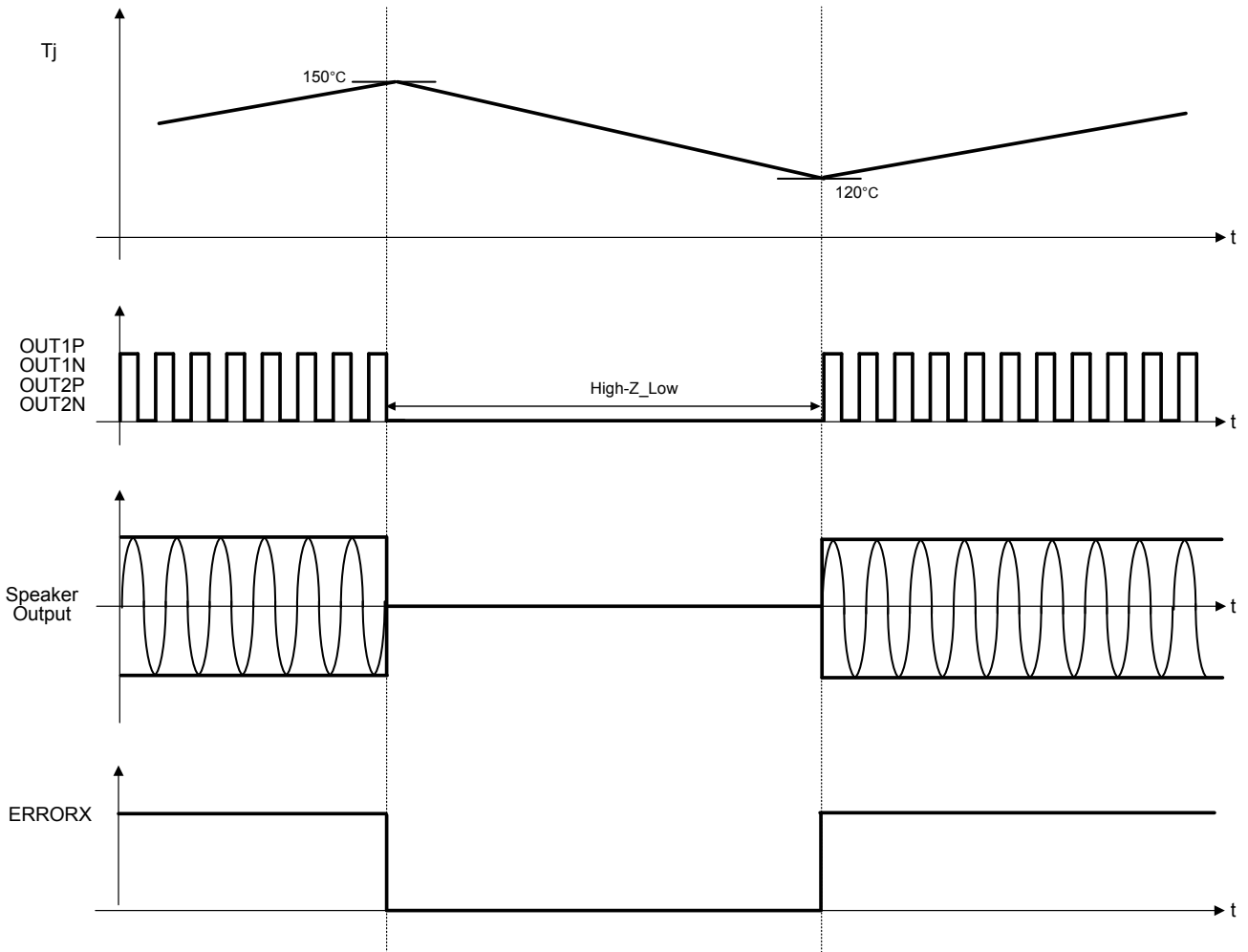


Figure 52. Overheat Protection Sequence

(5) Under Voltage Protection

This IC has under voltage protection circuit that mutes the output speaker once extreme drop in the power supply voltage is detected.

Detecting condition - It will detect when MUTEX pin is set High and the power supply voltage becomes lower than 4V(Typ).Speaker output mutes immediately when under voltage protection is detected.

Releasing condition - It will release when MUTEX pin is set High and the power supply voltage becomes more than 4.1V(Typ).The speaker output is back to its normal operation immediately when released. (Auto recovery)

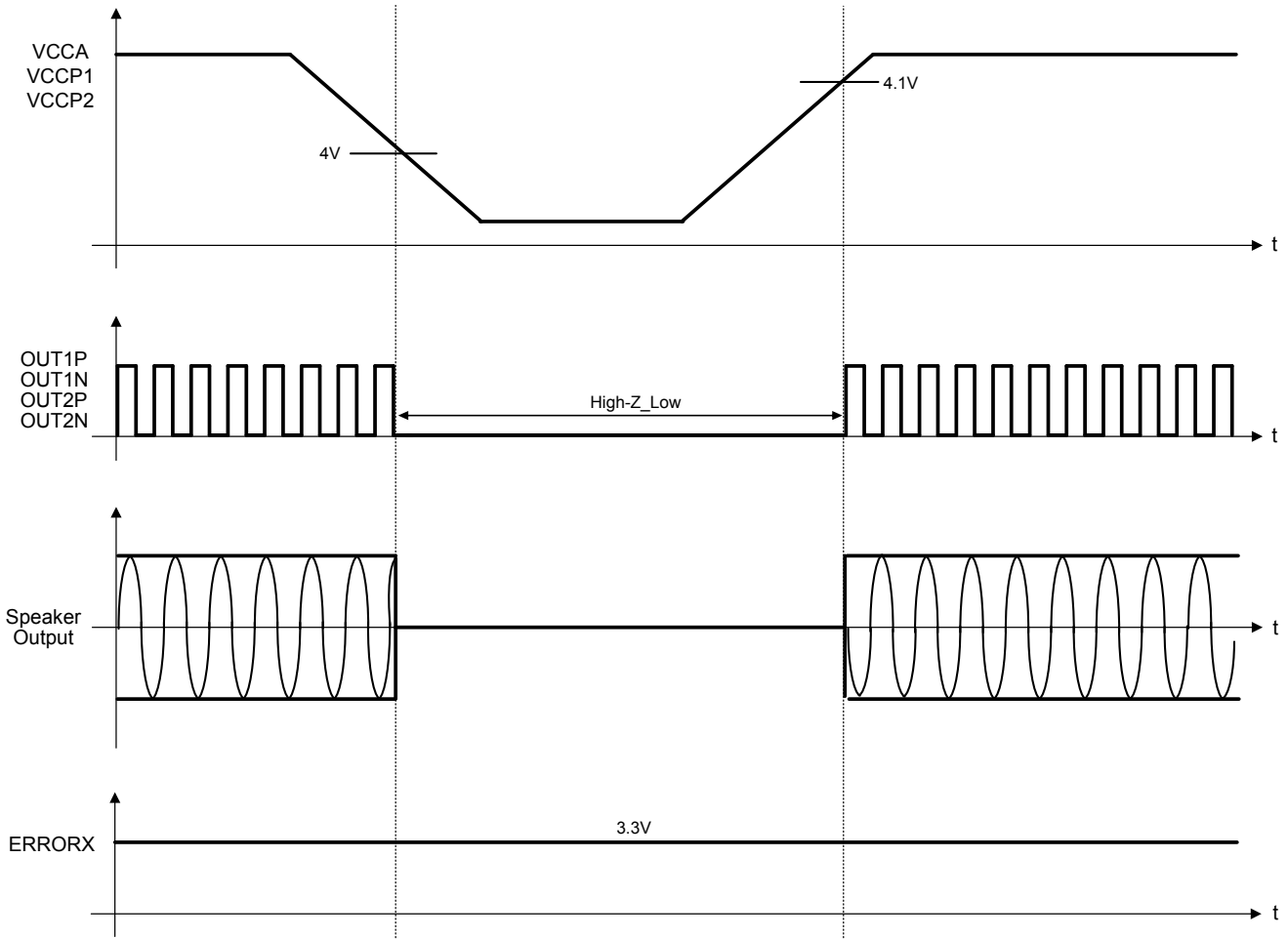


Figure 53. Under Voltage Protection Sequence

5. Selecting External Components

(1) Output LC Filter Circuit

An output filter is required to eliminate radio-frequency components exceeding the audio-frequency region supplied to a load (speaker). Because this IC uses output PWM frequencies any of 400kHz, 500kHz, 600kHz, 1000kHz or 1200kHz, the high-frequency components must be appropriately removed.

This section takes an example of an LC type LPF shown below, in which coil L and capacitor C compose a differential filter with an attenuation property of -12dB/oct. A large part of switching currents flow to capacitor C, and only a small part of the currents flow to speaker R_L . This filter reduces unwanted emission this way. In addition, coil L and capacitor C compose a filter against in-phase components, reducing unwanted emission further.

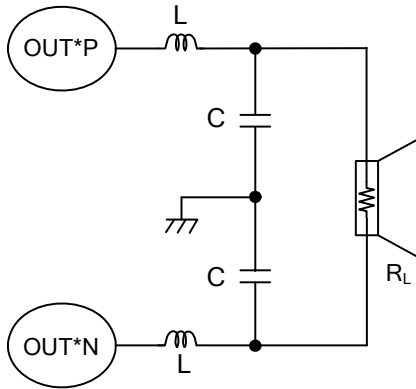


Figure 54. Output LC Filter

The following shows output LC filter constants and cutoff frequencies f_c with typical load impedances.

Stereo BTL

R_L	L	C	f_c
6Ω, 8Ω	15μH	1μF	41kHz

Monaural PBTL

R_L	L	C	f_c
4Ω	10μH	2.2μF	34kHz

Use inductors with low ESR and with sufficient margin of allowable currents. Power loss will increase if inductors with high ESR are used.

Select a closed magnetic circuit type product in normal cases to prevent emission noise.

Use capacitors with low equivalent series resistance, and good impedance characteristics at high frequency ranges (100kHz or higher). Also, select an item with sufficient voltage rating because massive amount of high-frequency current flow is expected.

(2) Snubber Circuit Constant

When overshoot / undershoot of PWM Output exceeds absolute maximum rating, or when overshoot / undershoot of PWM output negatively affects EMC, snubber circuit is used as shown below. And if $V_{CC} > 11V$, the snubber circuit must be added.

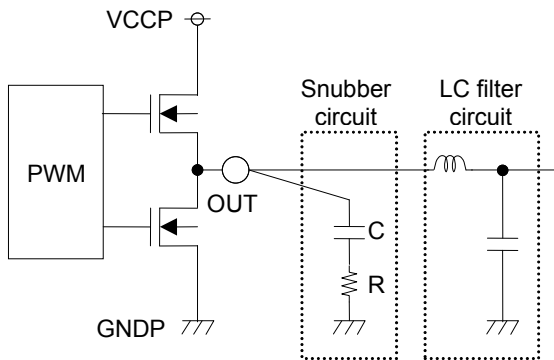


Figure 55. Snubber Circuit

The following table shows ROHM recommended value of “Snubber filter constants” when using ROHM board.

Stereo BTL

R_L	C	R
6Ω	680pF, 25V B(±10%)	5.6Ω, 1/10W J(±5%)
8Ω	680pF, 25V B(±10%)	5.6Ω, 1/10W J(±5%)

Monaural PBTL

R_L	C	R
4Ω	680pF, 25V B(±10%)	5.6Ω, 1/10W J(±5%)

Caution1: If the impedance characteristics of the speakers at high-frequency range increase rapidly, the IC might not have stable operation in the resonance frequency range of the LC filter. Therefore, consider adding damping-circuit, etc., depending on the impedance of the speaker.

Caution2: Though this IC has a short protection function, when short to VCC or GND after the LC filter, over-current occurs during short protection function operation. Be careful about over/undershoot which exceeds the maximum standard ratings because back electromotive force of the inductor will occur which sometimes leads to IC destruction.

(3)Operating condition with the application component

Parameter	Parts No.	Limit			Unit	Conditions
		Min	Typ	Max		
Tolerance of Capacitor for BSP	C16, C20, C21, C25	1.0 ^(Note 20)	2.2	2.95 ^(Note 21)	μF	B characteristics, 16V Ceramic type capacitor recommended

(Note 20) Should use the capacity of the capacitor not to be less than a minimum in consideration of temperature characteristics and dc-bias characteristics.
 (Note 21) It is value in consideration of +/-10% of capacity unevenness, capacity rate of change 22%. Please use the capacitor within this limit.

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

OR

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the maximum junction temperature rating.

6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When $GND > Pin A$ and $GND > Pin B$, the P-N junction operates as a parasitic diode.

When $GND > Pin B$, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

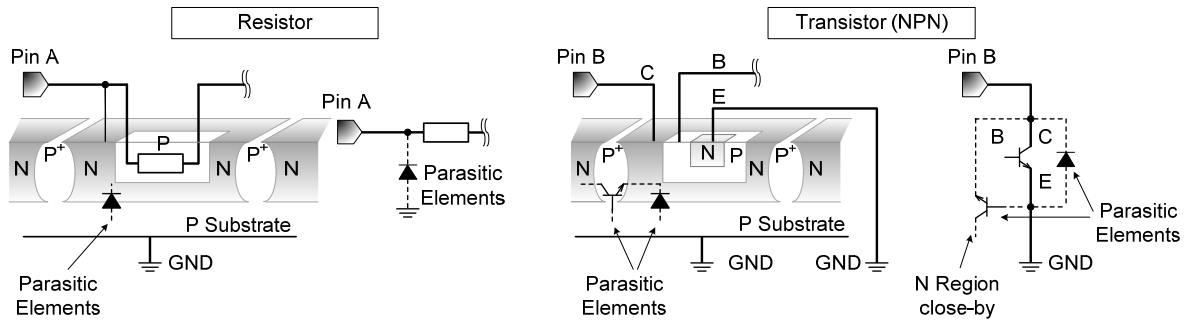


Figure 56. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Thermal Shutdown Circuit(TSD)

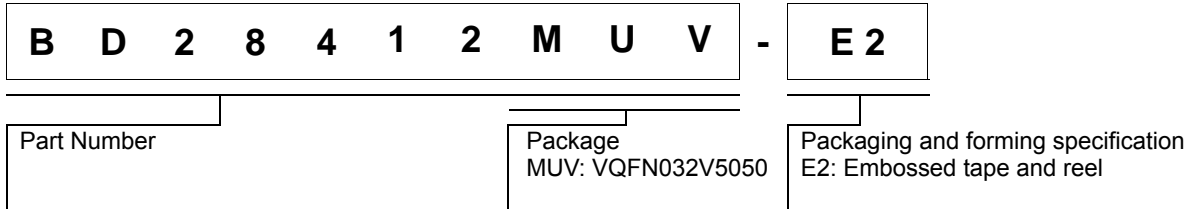
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (T_j) will rise which will activate the TSD circuit that will turn OFF all output pins. When the T_j falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

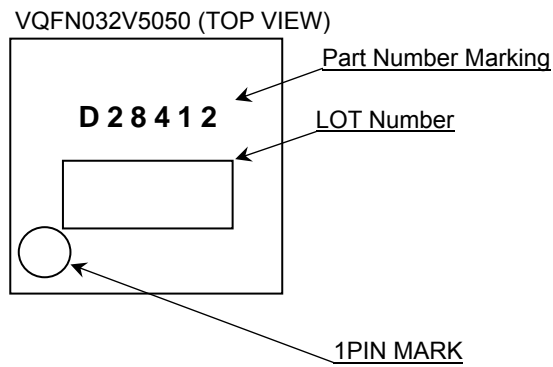
15. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information

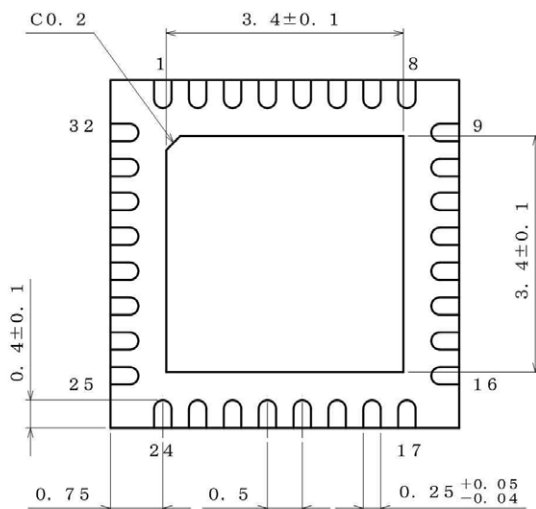
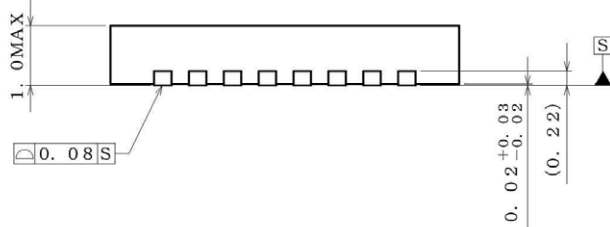
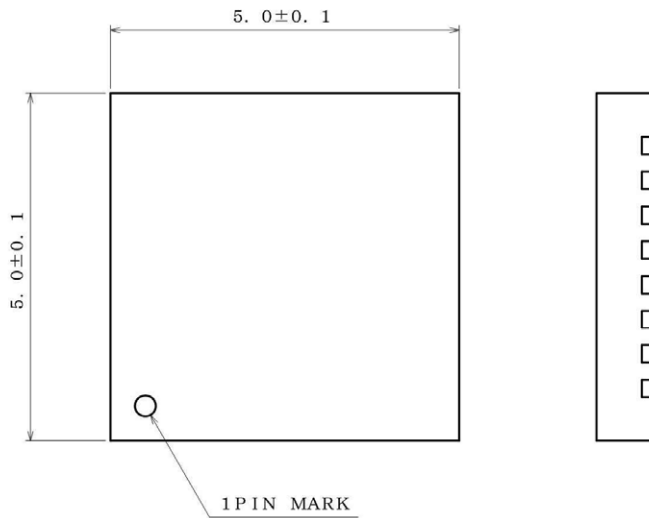


Marking Diagram



Physical Dimension, Tape and Reel Information

Package Name	VQFN032V5050
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(UNIT : mm)
 PKG : VQFN032V5050
 Drawing No. EX461-5001-2

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)

*Order quantity needs to be multiple of the minimum quantity.

Revision History

Date	Revision	Changes
29.Jan.2016	001	New Release
06.Jun.2016	002	P.3 to P.5 Pin Description P.7 Absolute Maximum Ratings P.7 Thermal Resistance P.8 Thermal Resistance, Copper Pattern P.9 Electrical Characteristics, Input Impedance 1 P.11 to P.18 Typical Performance Curves P.19 Power Up / Down Sequence Figure 38. P.21 Power Limit Function P.23 to P.27 Application Circuit Example P.35 Operating condition with the application component ADD
21.Sep.2016	003	P.28 DC voltage protection P.31 DC voltage protection

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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 - Installation of redundant circuits to reduce the impact of single or multiple circuit failure
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 - Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
 - Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - Sealing or coating our Products with resin or other coating materials
 - Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
- Please verify and confirm characteristics of the final or mounted products in using the Products.
- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
- Confirm that operation temperature is within the specified range described in the product specification.
- ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

- When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
- In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
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 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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