



**MICROCHIP**

# PIC18F87J11 FAMILY

## PIC18F87J11 Family Rev. A5 Silicon Errata

The PIC18F87J11 Family parts you have received conform functionally to the Device Data Sheet (DS39778C), except for the anomalies described below.

Any Data Sheet Clarification issues related to the PIC18F87J11 Family devices will be reported in a separate Data Sheet errata. Please check the Microchip web site for any existing issues.

**The following silicon errata apply only to PIC18F87J11 Family devices with these Device/Revision IDs:**

Part Number	Device ID	Revision ID
PIC18F66J11	0100 0100 010	0 0101
PIC18F66J16	0100 0100 011	0 0101
PIC18F67J11	0100 0100 100	0 0101
PIC18F86J11	0100 0100 111	0 0101
PIC18F86J16	0100 0101 000	0 0101
PIC18F87J11	0100 0101 001	0 0101

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in binary in the format "DEVID2 DEVID1".

### 1. Module: Master Synchronous Serial Port (MSSP)

When configured for I<sup>2</sup>C™ slave reception, the MSSP module may not receive the correct data, in extremely rare cases. This occurs only if the Serial Receive/Transmit Buffer Register (SSPBUF) is not read within a window after the SSPIF interrupt (PIR1<3>) has occurred.

#### Work around

The issue can be resolved in either of these ways:

- Prior to the I<sup>2</sup>C slave reception, enable the clock stretching feature.  
This is done by setting the SEN bit (SSPCON2<0>).
- Each time the SSPIF is set, read the SSPBUF before the first rising clock edge of the next byte being received.

#### Date Codes that pertain to this issue:

All engineering and production devices.

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## REVISION HISTORY

Rev A Document (10/2008)

First revision of this document. Includes silicon issue 1 (Master Synchronous Serial Port – MSSP).

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