NCP5360A

Integrated Driver and MOSFET

The NCP5360A integrates a MOSFET driver, high-side MOSFET and low-side MOSFET into a 8mm x 8mm 56-pin QFN package. The driver and MOSFETs have been optimized for high-current DC-DC buck power conversion applications. The NCP5360A integrated solution greatly reduces package parasitics and board space compared to a discrete component solution.

Features

- Capable of Switching Frequencies up to 1 MHz
- Capable of Output Currents up to 40 A
- Integrated Bootstrap Diode
- Undervoltage Lockout
- Thermal Shutdown / Thermal Shutdown
- These are Pb-free Devices

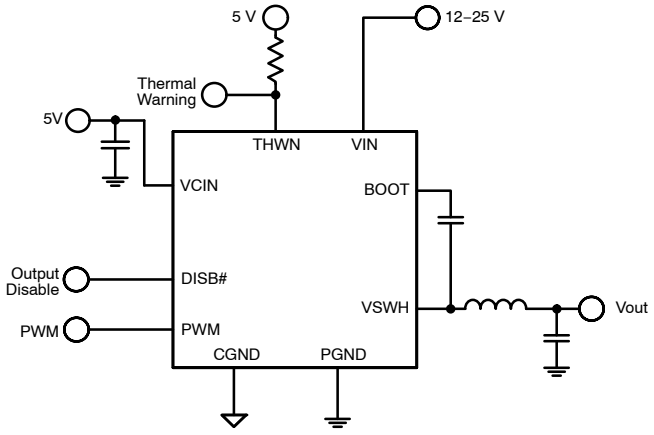

Figure 1. Application Schematic

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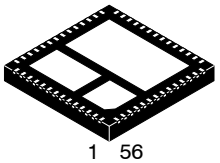
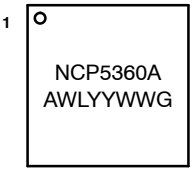


QFN56
MN SUFFIX
CASE 485AY

MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb–Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NCP5360AMNR2G	QFN56 (Pb–Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

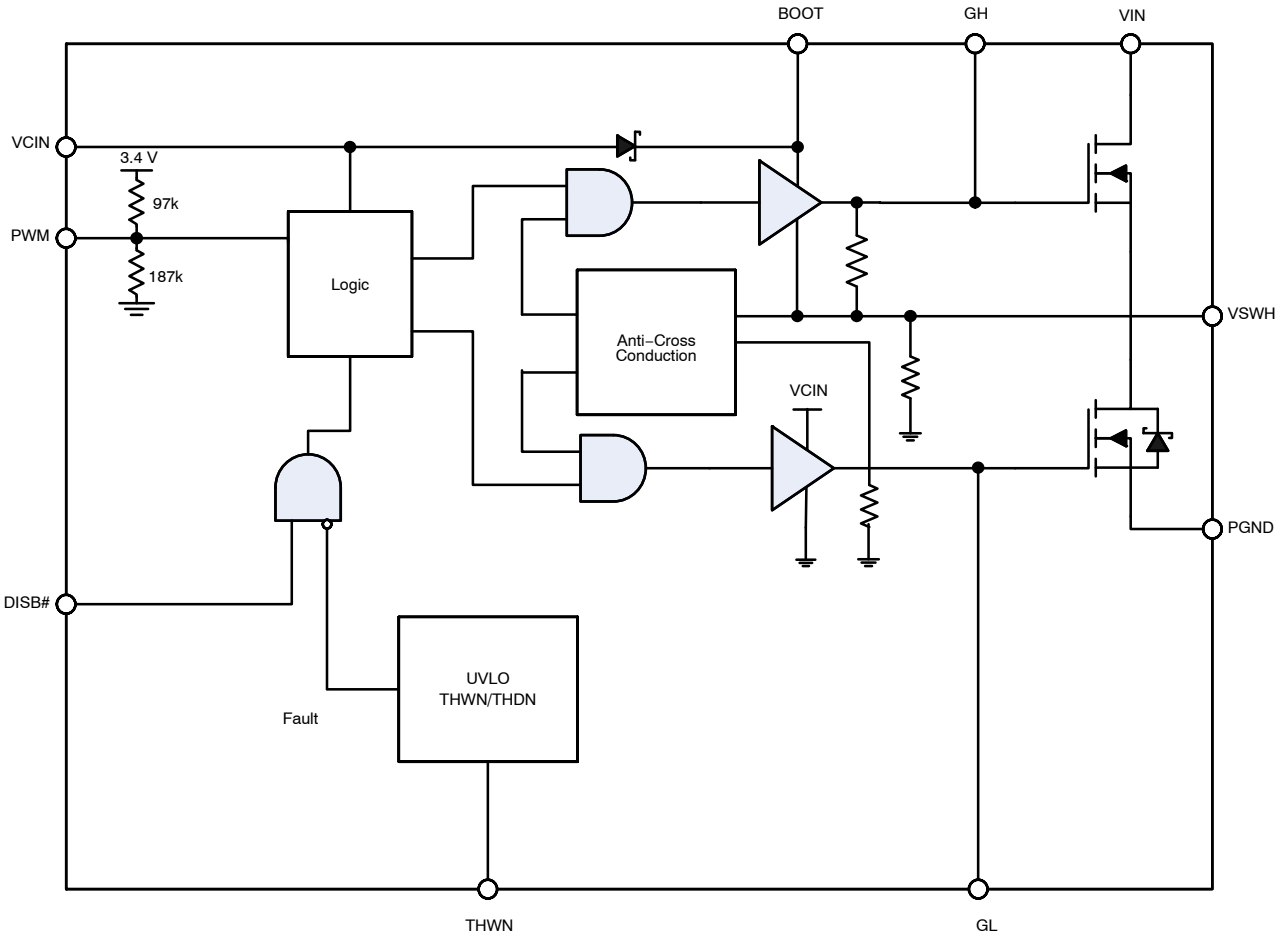
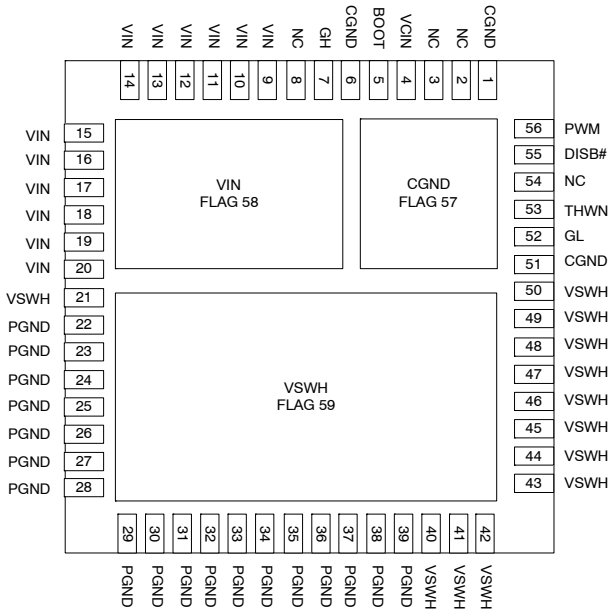


Figure 2. Simplified Block Diagram

PIN CONNECTIONS



(Top View)

Figure 3. Pin Connections

Table 1. PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
2, 3, 8, 54	NC	No Connect
4	VCIN	Control Input Voltage
1, 6, 51, Flag 57	CGND	Control Signal Ground
21, 40–50, Flag 59	VSWH	Switch Node Output
52	GL	Low Side FET Gate Access Pin
22–39	PGND	Power Ground
9–20, Flag 58	VIN	Input Voltage
7	GH	High Side FET Gate Access Pin
5	BOOT	Bootstrap Voltage Pin
53	THWN	Thermal Warning
55	DISB#	Output Disable Pin
56	PWM	PWM Drive Logic

Table 2. ABSOLUTE MAXIMUM RATINGS

Pin Symbol	Pin Name	Min	Max
VCIN	Control Input Voltage	−0.3 V	7 V
VIN	Power Input Voltage	−0.3 V	30 V
BOOT	Bootstrap Voltage	−0.3 V	35 V wrt/PGND 40 V < 50 ns wrt/PGND 7 V wrt/VSWH
VSWH	Switch Node Output	−0.3 V	30 V
PWM	PWM Drive Logic	−0.3 V	6.5 V
DISB#	Output Disable	−0.3 V	6.5 V
THWN	Thermal Warning	−0.3 V	6.5 V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance, High−Side FET	$R_{\theta JPCB}$	7.0	°C/W
Thermal Resistance, Low−Side FET	$R_{\theta JPCB}$	3.0	°C/W
Operating Junction Temperature	T_J	−55 to 150	°C
Storage Temperature	T_S	−55 to 150	°C
Moisture Sensitivity Level	MSL	3	

Table 4. OPERATING RANGES

Rating	Symbol	Min	Typ	Max	Unit
Control Input Voltage	V_{CIN}	4.5	5.0	5.5	V
Input Voltage	V_{IN}	4.5	12	25	V

ELECTRICAL CHARACTERISTICS (Note 1) (VCIN = 5 V, VIN = 12 V, T_A = −10°C to +100°C, unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
SUPPLY CURRENT						
VCIN Current (Normal Mode)	–	DISB# = 5 V, PWM = OSC, Fsw = 400 kHz		20	30	mA
VCIN Current (Shutdown Mode)	–	DISB# = GND		15	30	μA
UNDERVOLTAGE LOCKOUT						
UVLO Startup	–		3.8	4.35	4.5	V
UVLO Hysteresis	–		150	200	250	mV
BOOTSTRAP DIODE						
Forward Voltage	–	VCIN = 5 V, Forward Bias Current = 2 mA	0.1	0.4	0.6	V
PWM INPUT						
PWM Input Voltage High	V_{PWM_HI}		3.6			V
PWM Input Voltage Mid−State	V_{PWM_MID}		1.3		3.0	V
PWM Input Voltage Low	V_{PWM_LO}				0.7	V
Tri−State Shutdown Holdoff Time	–			250		ns
PWM Input Resistance	_			63		kΩ
PWM Input Bias Voltage	_			2.2		V
OUTPUT DISABLE						
Output Disable Input Voltage High	$V_{DISB\#\_HI}$		2.0			V
Output Disable Input Voltage Low	$V_{DISB\#\_LO}$				0.8	V
Output Disable Hysteresis	–			500		mV
Output Disable Propagation Delay				20	40	ns
THERMAL WARNING / SHUTDOWN						
Thermal Warning Temperature	–			150		°C
Thermal Warning Hysteresis	–			15		°C
Thermal Shutdown Temperature	–			180		°C
Thermal Shutdown Hysteresis	–			25		°C

1. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_J = T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

APPLICATIONS INFORMATION

Theory of Operation

The NCP5360A is an integrated driver and MOSFET module designed for use in a synchronous buck converter topology. A single PWM input signal is all that is required to properly drive the high−side and low−side MOSFETs.

Low−Side Driver

The low−side driver is designed to drive a ground−referenced low $R_{DS(on)}$ N−Channel MOSFET. The voltage rail for the low−side driver is internally connected to VCIN and PGND.

High−Side Driver

The high−side driver is designed to drive a floating low RDS(on) N−channel MOSFET. The gate voltage for the high side driver is developed by a bootstrap circuit referenced to Switch Node (VSWH) pin.

The bootstrap circuit is comprised of the internal diode and an external bootstrap capacitor. When the NCP5360A is starting up, the VSWH pin is at ground, so the bootstrap capacitor will charge up to VCIN through the bootstrap diode See Figure 1. When the PWM input goes high, the high−side driver will begin to turn on the high−side MOSFET using the stored charge of the bootstrap capacitor. As the high−side MOSFET turns on, the VSWH pin will rise. When the high−side MOSFET is fully on, the switch node will be at 12 V, and the BST pin will be at 5 V plus the charge of the bootstrap capacitor (approaching 17 V).

The bootstrap capacitor is recharged when the switch node goes low during the next cycle.

Safety Timer and Overlap Protection Circuit

It is very important that MOSFETs in a synchronous buck regulator do not both conduct at the same time. Excessive shoot−through or cross conduction can damage the MOSFETs, and even a small amount of cross conduction will cause a decrease in the power conversion efficiency.

The NCP5360A prevents cross conduction by monitoring the status of the MOSFETs and applying the appropriate amount of “dead−time” or the time between the turn off of one MOSFET and the turn on of the other MOSFET.

When the PWM input pin goes high, the gate of the low−side MOSFET (GL pin) will go low after a propagation delay (tpdlGL). The time it takes for the low−side MOSFET to turn off (tfGL) is dependent on the total charge on the low−side MOSFET gate. The NCP5360A monitors the gate voltage of both MOSFETs and the switchnode voltage to determine the conduction status of the MOSFETs. Once the low−side MOSFET is turned off an internal timer will delay (tpdhGH) the turn on of the high−side MOSFET.

Likewise, when the PWM input pin goes low, the gate of the high−side MOSFET (GH pin) will go low after the propagation delay (tpdlGH). The time to turn off the high−side MOSFET (tfGH) is dependent on the total gate charge of the high−side MOSFET. A timer will be triggered once the high−side MOSFET has stopped conducting, to delay (tpdhGL) the turn on of the low−side MOSFET.

Thermal Warning / Thermal Shutdown

When the temperature of the driver reaches 150°C, the THWN pin will be pulled low indicating a thermal warning. At this point, the part continues to function normally. When the temperature drops below 135°C, the THWN will go high.

If the driver temperature exceeds 180°C, the part will enter thermal shutdown and turn off both MOSFETs. Once the temperature falls below 155°C, the part will resume normal operation.

The THWN pin has a maximum current capability of 30 mA.

Power Supply Decoupling

The NCP5360A can source and sink relatively large current to the gate pins of the MOSFETs. In order to maintain a constant and stable supply voltage (VCIN) a low ESR capacitor should be placed near the power and ground pins. A 1 μF to 4.7 μF multi layer ceramic capacitor (MLCC) is usually sufficient.

Bootstrap Circuit

The bootstrap circuit uses a charge storage capacitor (C_{BST}) and the internal diode. The bootstrap capacitor must have a voltage rating that is able to withstand twice the maximum supply voltage. A minimum 50 V rating is recommended. A bootstrap capacitance greater than 100 nF and a minimum 50 V rating is recommended. A good quality ceramic capacitor should be used.

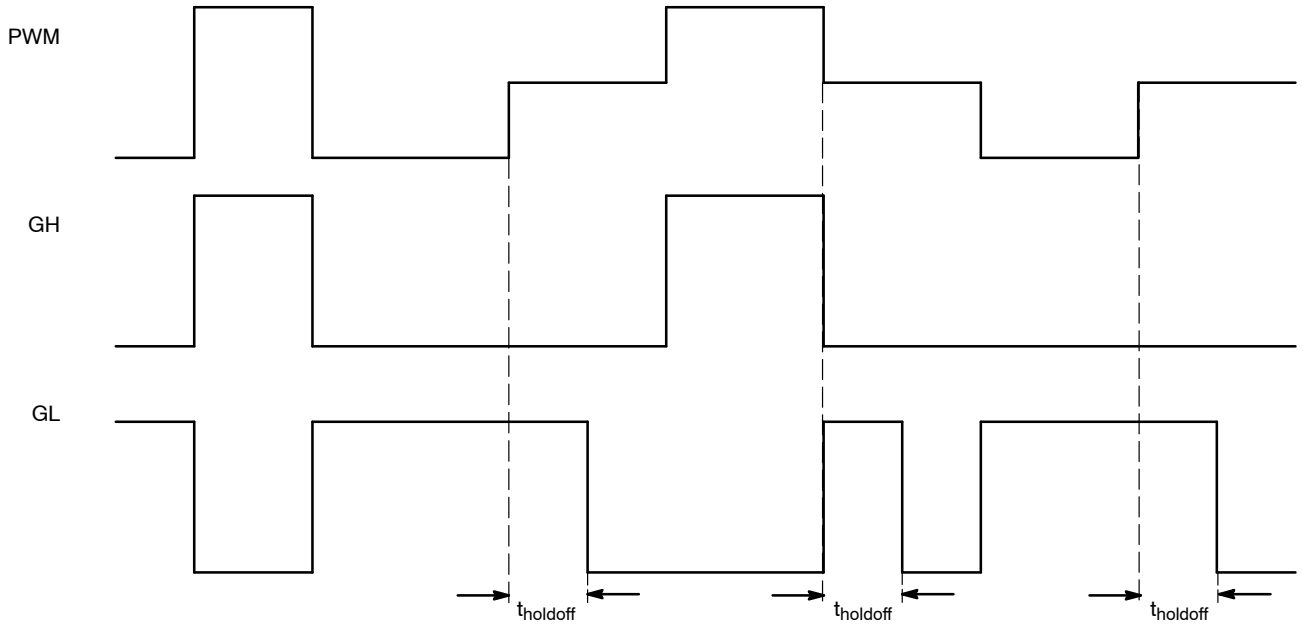
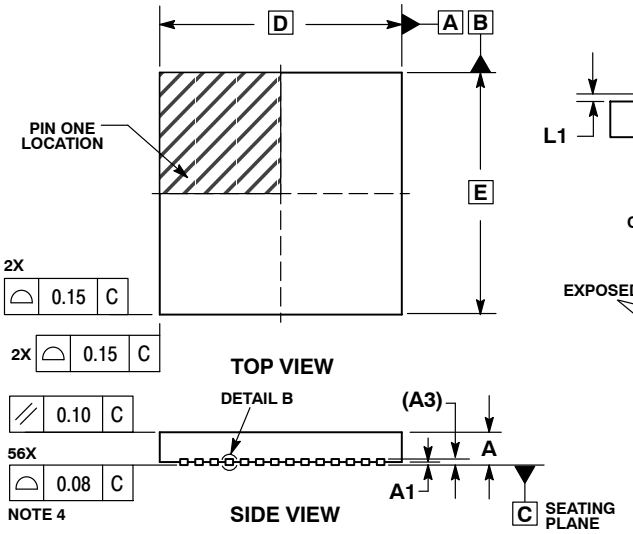
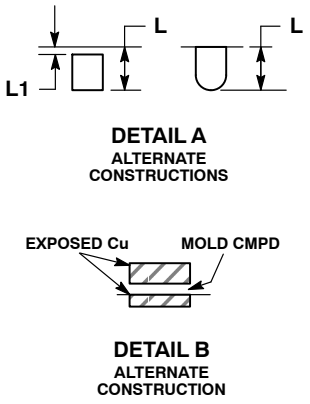


Figure 4. Tri−State Operation

PACKAGE DIMENSIONS

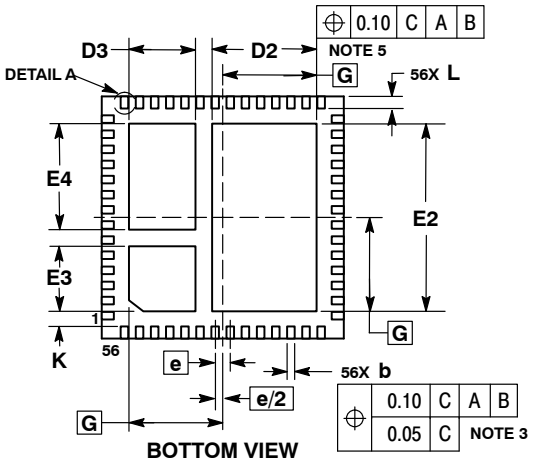
QFN56 8x8, 0.5P
MN SUFFIX
CASE 485AY−01
ISSUE O

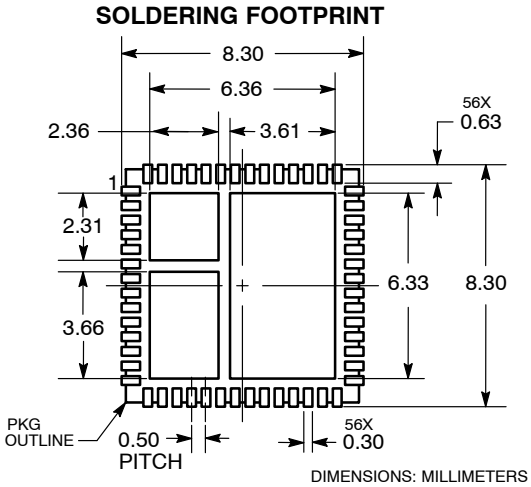




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. POSITIONAL TOLERANCE APPLIES TO ALL THREE EXPOSED PADS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	−−−	0.05
A3	0.20 REF	
b	0.18	0.30
D	8.00 BSC	
D2	3.35	3.55
D3	2.10	2.30
E	8.00 BSC	
E2	6.10	6.30
E3	2.05	2.25
E4	3.40	3.60
e	0.50 BSC	
G	3.10	
K	0.20	−−−
L	0.30	0.50
L1	−−−	0.15





DIMENSIONS: MILLIMETERS

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