PIC16F62X

PIC16F62X Rev. C Silicon/Data Sheet Errata

The PIC16F62X (Rev. C) parts you have received conform functionally to the Device Data Sheet (DS40300**C**), except for the anomalies described below.
Microchip intends to address all issues listed here in future revisions of the PIC16F62X silicon.

1. Module: I/O Ports

A read of the PORTB Data Direction Register (TRISB) returns the Data Direction state on the port pins themselves and not the contents of the TRISB register latch.

FIGURE 5-8: BLOCK DIAGRAM OF RB0/INT PIN

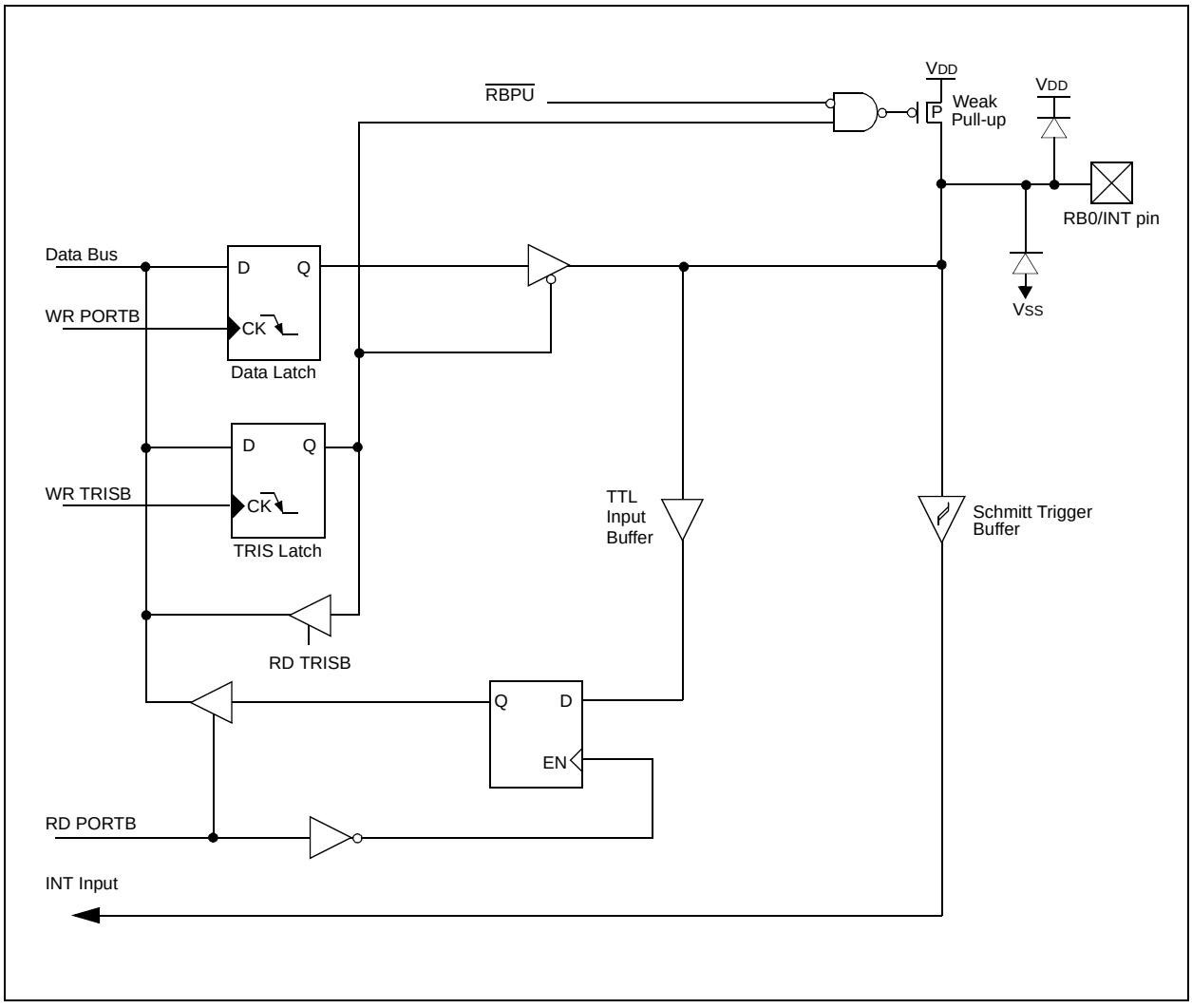
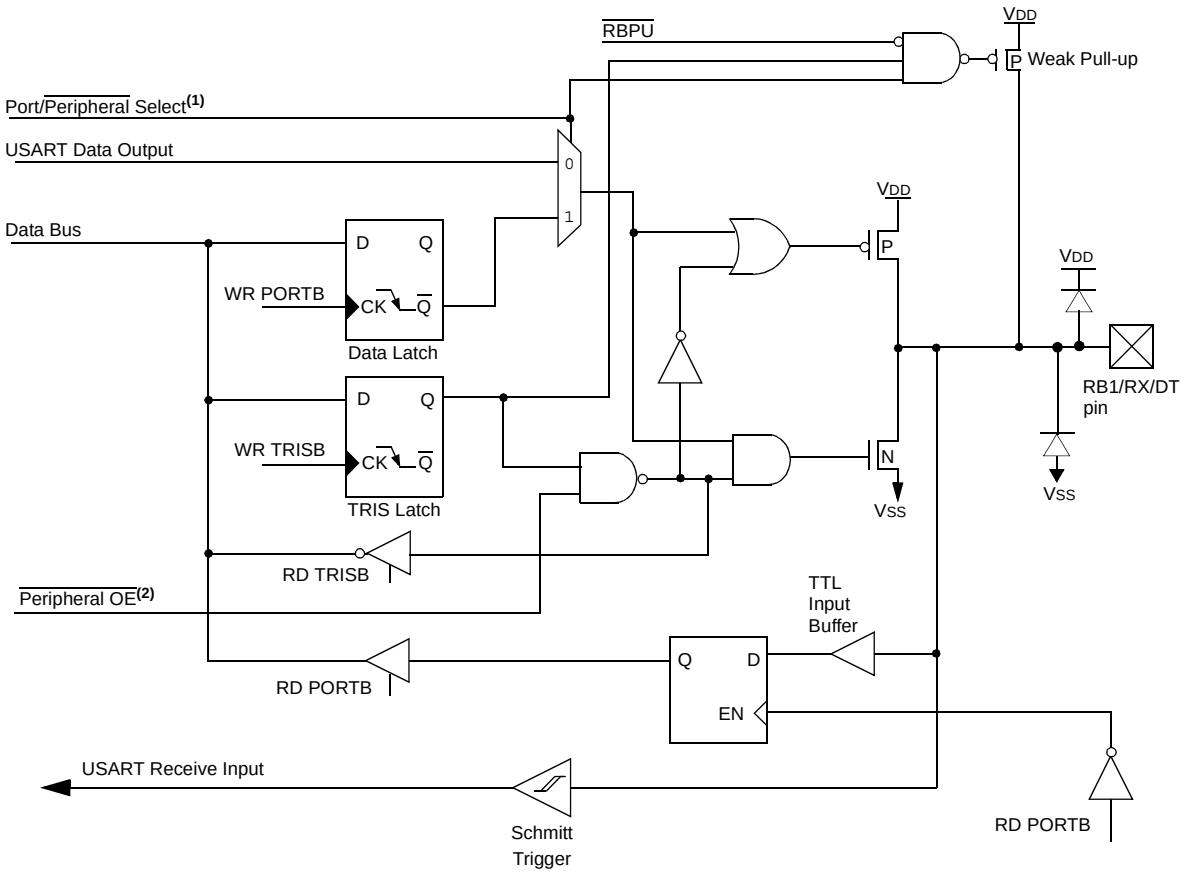
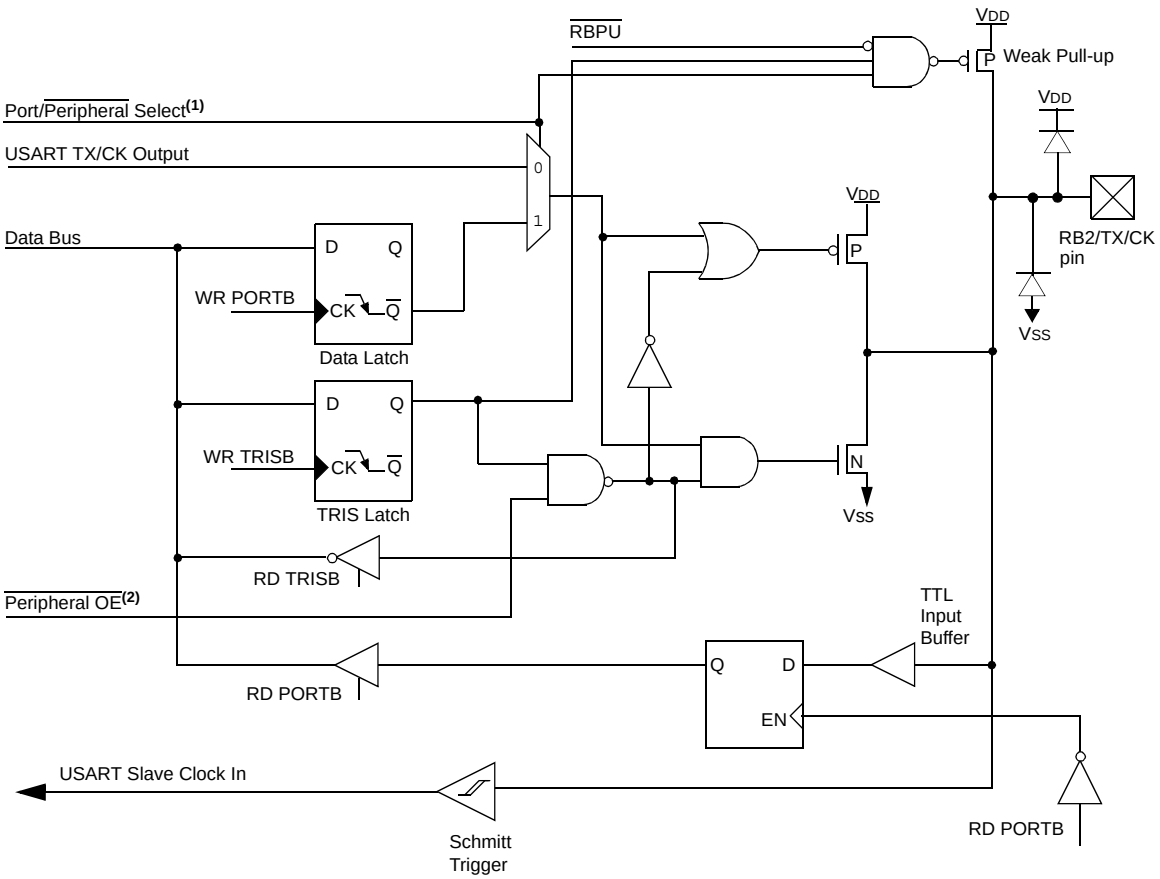


FIGURE 5-9: BLOCK DIAGRAM OF RB1/RX/DT PIN



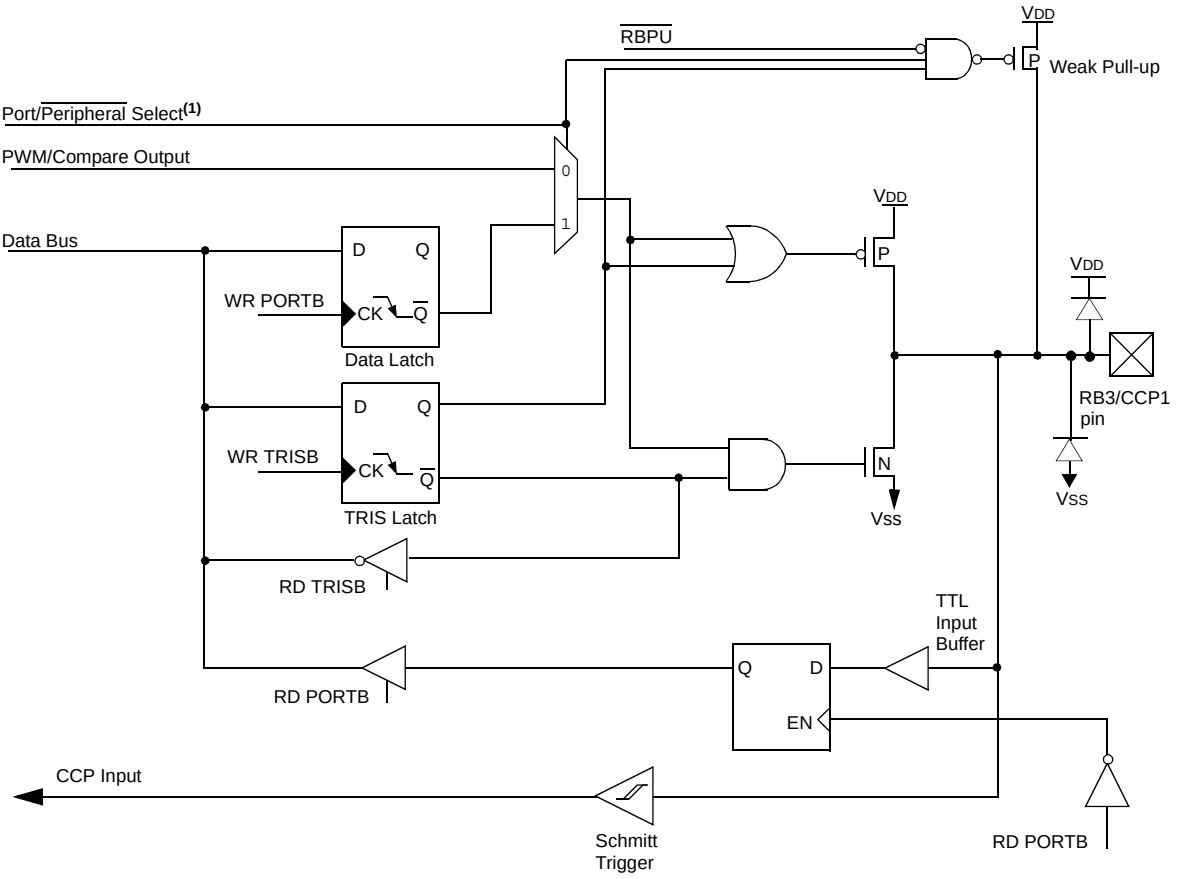
Note 1: Port/Peripheral select signal selects between port data and peripheral output.
2: Peripheral OE (output enable) is only active if peripheral select is active.

FIGURE 5-10: BLOCK DIAGRAM OF RB2/TX/CK PIN



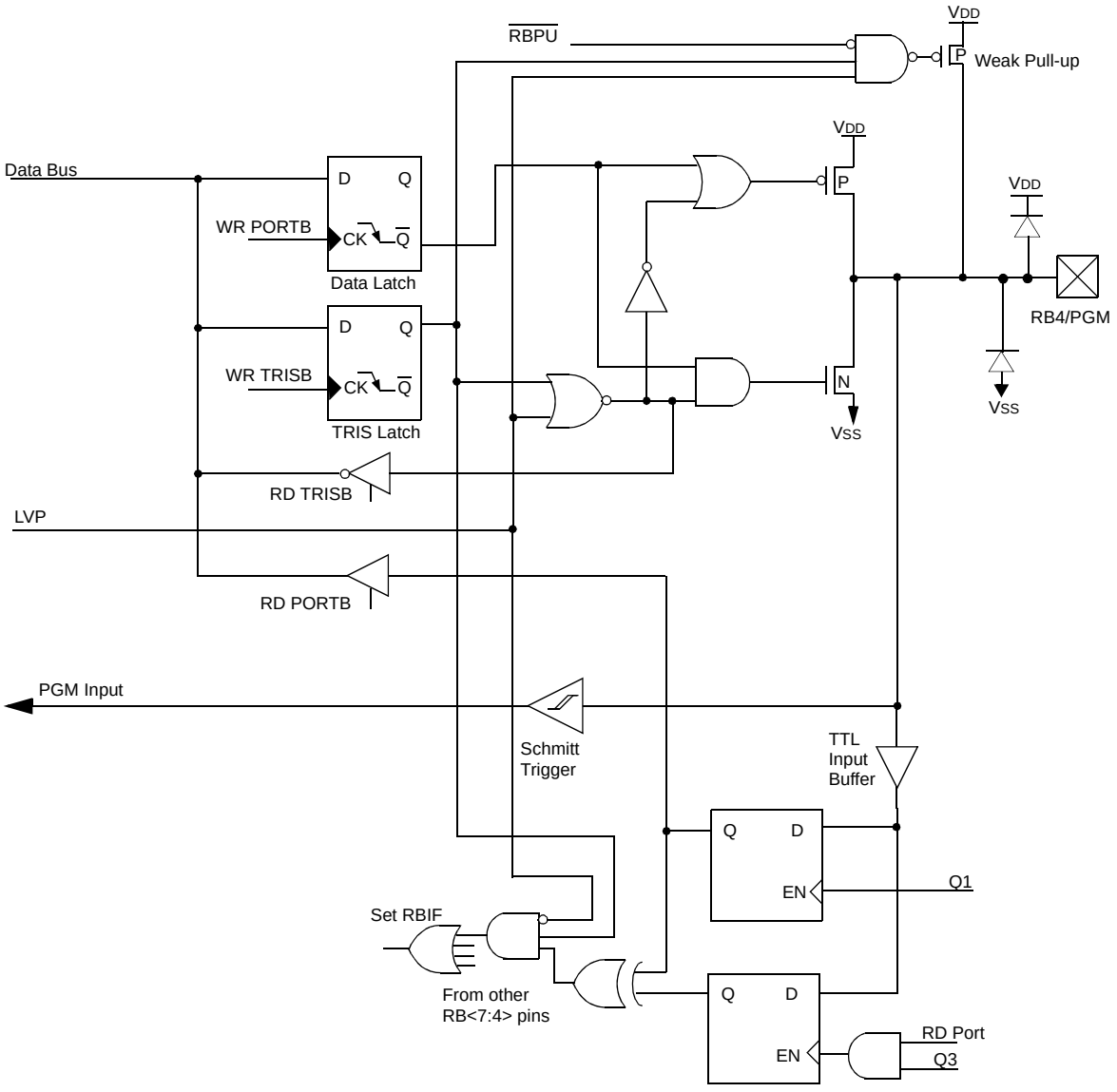
Note 1: Port/Peripheral select signal selects between port data and peripheral output.
2: Peripheral OE (output enable) is only active if peripheral select is active.

FIGURE 5-11: BLOCK DIAGRAM OF RB3/CCP1 PIN



Note 1: Peripheral select is defined by CCP1M3:CCP1M0 (CCP1CON<3:0>).

FIGURE 5-12: BLOCK DIAGRAM OF RB4/PGM PIN



Note 1: The Low-Voltage Programming disables the interrupt-on-change and the weak pull-ups on RB4.

FIGURE 5-13: BLOCK DIAGRAM OF RB5 PIN

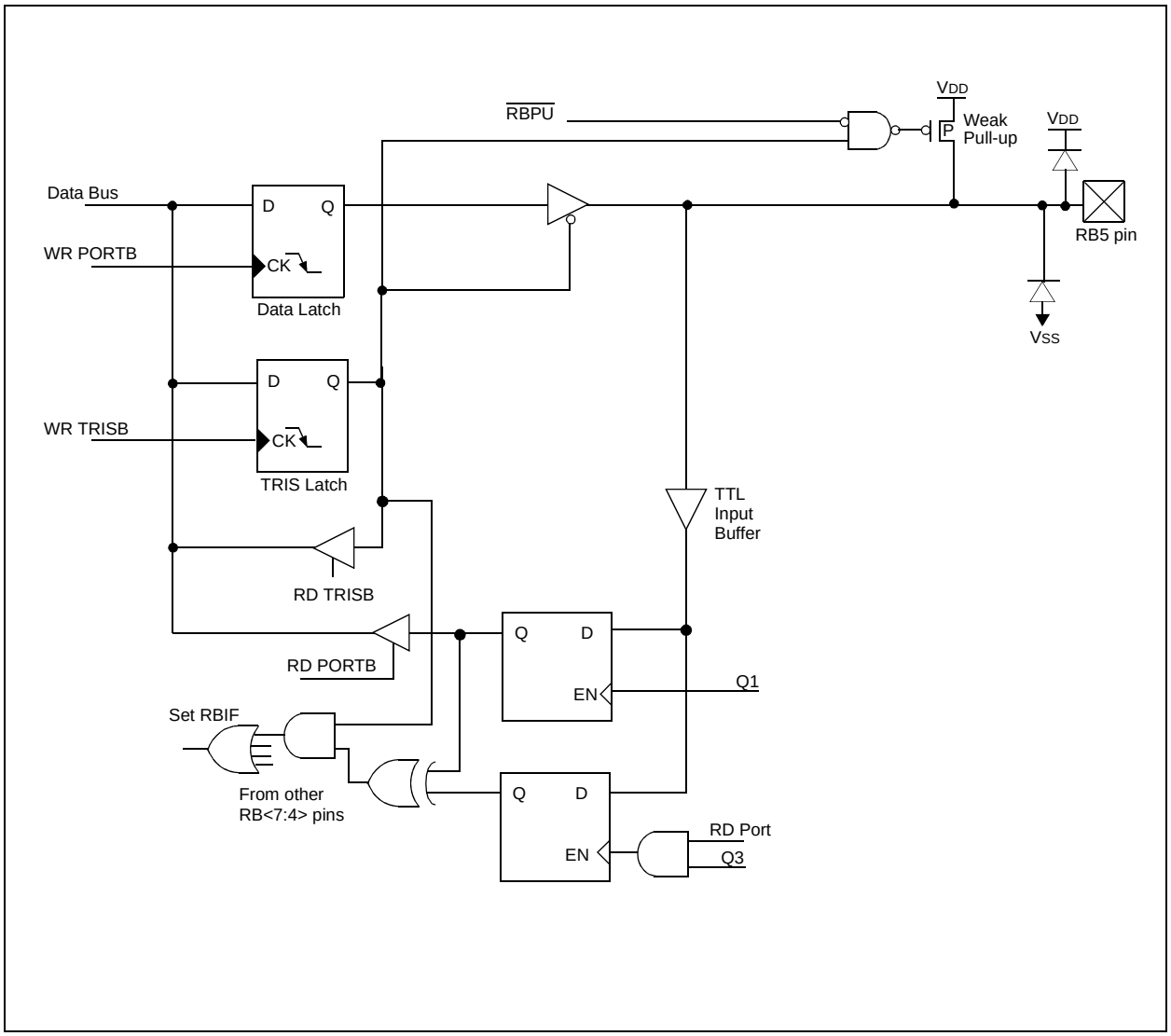


FIGURE 5-14: BLOCK DIAGRAM OF RB6/T1OSO/T1CKI PIN

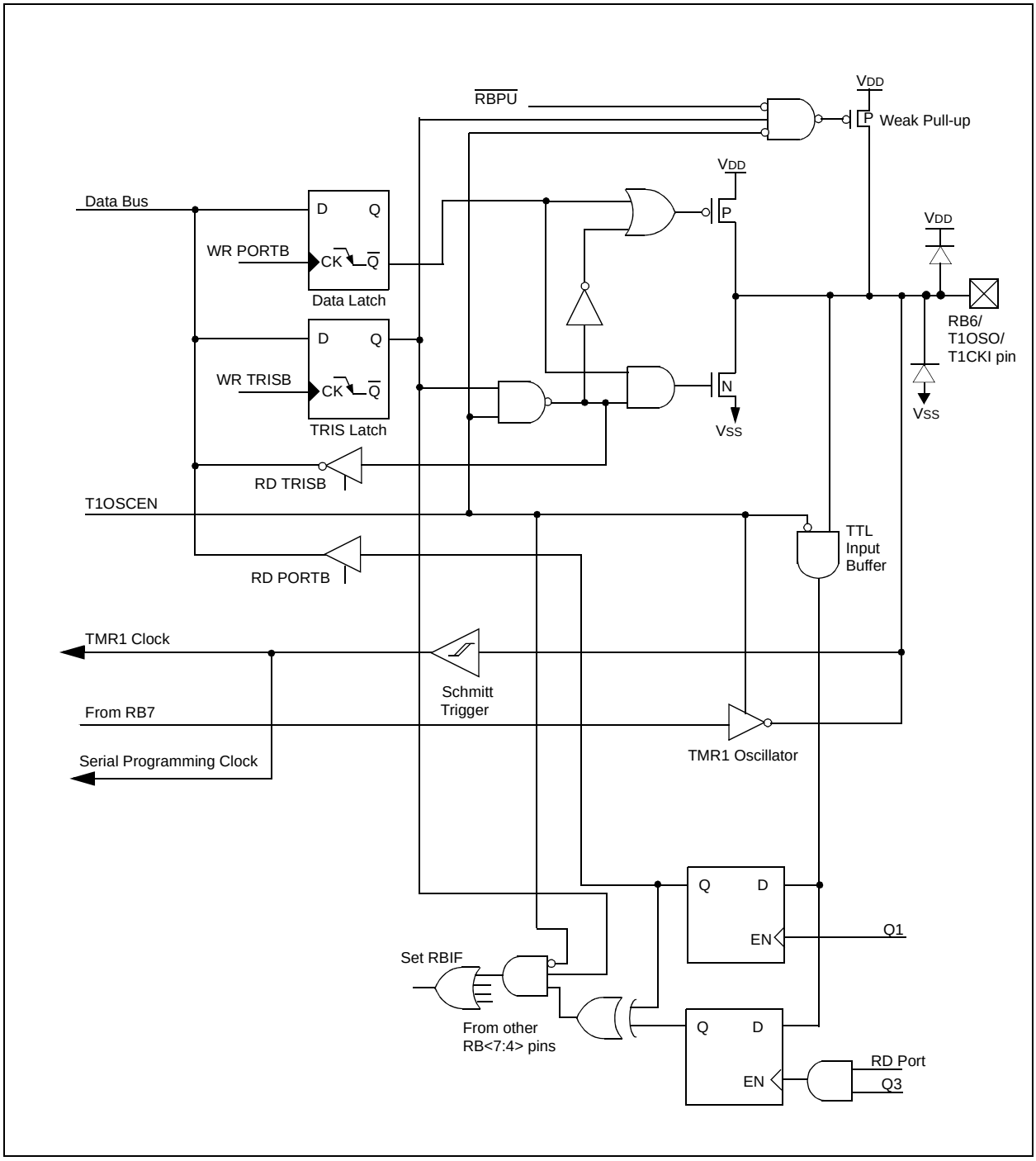
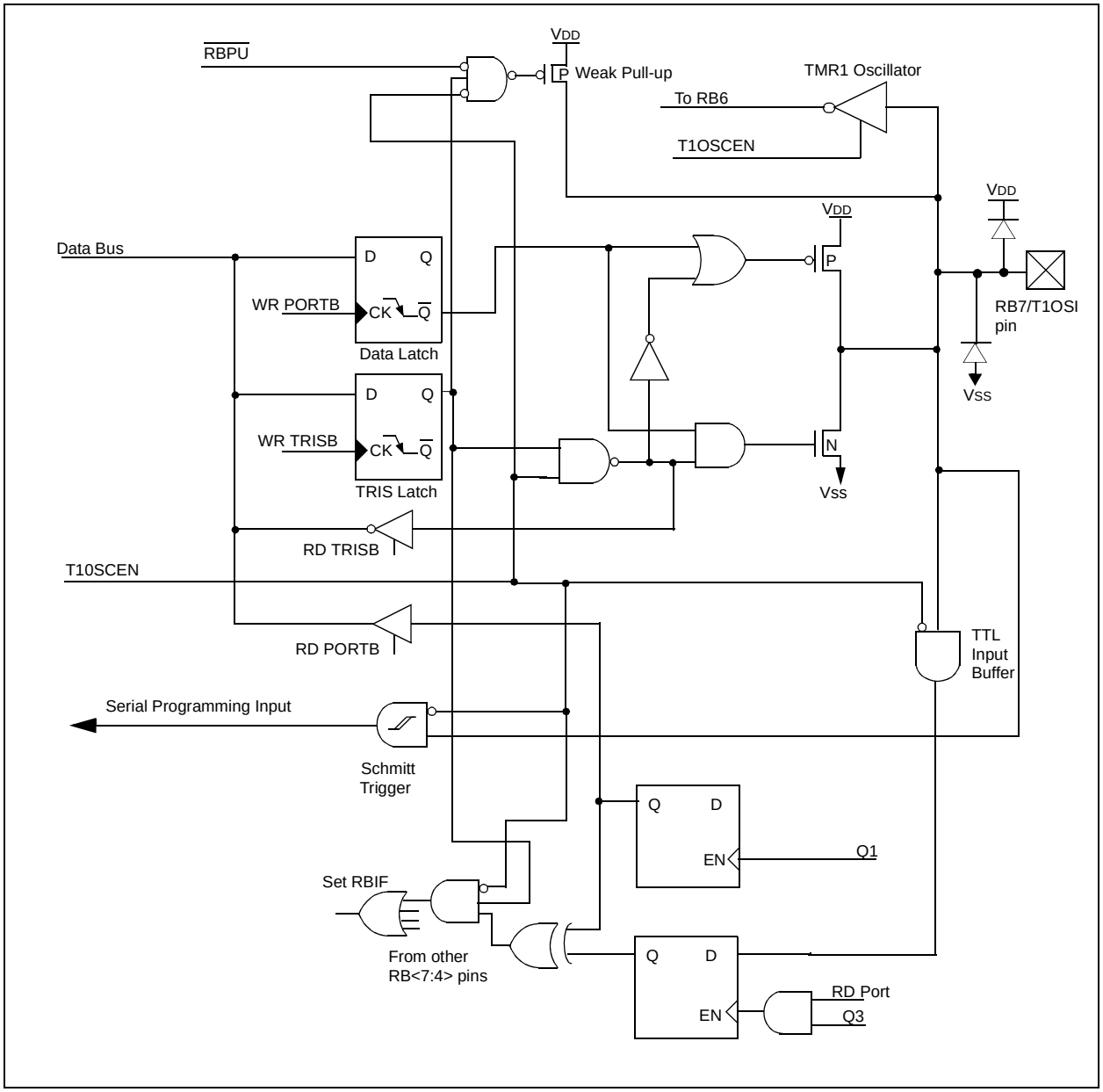


FIGURE 5-15: BLOCK DIAGRAM OF RB7/T1OSI PIN



2. Module: Comparator Mode 1

Mode 1 allows AN2 to drive the (+) inputs of both comparators. AN1 continues to drive the (-) input of Comparator 2, but AN0 and AN3 can be switched into the (-) input of Comparator 1. The state of the CIS bit chooses which input is to be connected to the comparator. When CIS = 0, AN0 is attached and the comparator functions correctly. When CIS = 1, AN3 is not completely connected to the comparator, resulting in incorrect behavior.

Mode 2 is also a Multiplex mode using the CIS bit. This mode functions correctly.

All other modes are unaffected by this Errata.

3. Module: Low-Voltage Programming Mode

The high-voltage override for low-voltage programming does not operate as specified in the programming specification. In the Low-Voltage Programming (LVP) mode, the device can be programmed without using 12V on VPP (pin 4). However, when high-voltage programming is used while the part has low-voltage programming enabled, the Low-Voltage mode is not overridden. If RB4 goes high for any reason during high-voltage programming with LVP enabled, the programming will be interrupted.

Work around

Pull RB4 (pin 10) to ground during the initial programming to prevent programming interruptions. Once LVP has been disabled, it remedies this issue with RB4.

4. Module: CCP (Compare Mode)

The CCP1 output latch, observed on RB3/CCP1/P1A, can change unexpectedly when the CCP module is changed from a set output on match (CCP1CON<3:0> = "1000") to clear output on match (CCP1CON<3:0> = "1001"), or vice versa. This condition will occur following a CCP Reset at the beginning of the third iteration of the following sequence.

- CCPR1<3:0> is changed from "1001" to "1000" or vice versa
- The TMR1H:TMR1L register pair matches the CCP1R1H:CCPR1L register pair

Step 1 of the third iteration will cause the CCP1 output latch to immediately and erroneously change to the inverse of the CCPR1<0> bit. This gives the appearance of an inverted CCP response to the third and subsequent compare match events.

The apparent inverted response will persist until the CCP1CON<3> bit is cleared (exiting Compare mode). Interrupts always occur correctly on the match condition. The error is only in the state of the CCP1 output latch.

Work around

Option 1

Use the CCP toggle output on Compare Match mode (CCP1CON<3.0> = "0010").

Option 2

Since the problem occurs after two changes to the Compare and Match modes, it is only necessary to reset the CCP1CON register before the third change is made. To remain backwards compatible with earlier versions of the CCP module, always reset the CCP1CON register when changing from the clear output on Match mode to the set output on Match mode, as described in the following steps.

1. Ensure the RB3 data latch is set to '0'.
2. Clear the CCP1CON register (clrf CCP1CON).
3. Set the CCP1CON<3:0> bits to "1000" for set output on match.

5. Module: $\overline{\text{MCLR}}$/RA5 in LVP Mode

When the PIC16F62X device has LVP enabled, $\overline{\text{MCLR}}$ is always enabled, regardless of the CONFIG register settings.

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS40300**C**), the following clarifications and corrections should be noted.

1. Module: Special Function Registers (T1SYNC, Register T1CON)

In Table 3-1, “Special Function Registers Summary Bank 0”, bit T1SYNC, in Register T1CON (address 10h), should be asserted logic low (i.e., $\overline{\text{T1SYNC}}$) as shown in bold below.

2. Module: Special Function Registers (ADEN, Register RCSTA)

In Table 3-1, “Special Function Registers Summary Bank 0”, bit ADEN, in Register RCSTA (address 18h), is misspelled. The correct spelling should be ADDEN, as shown in bold below.

This misspelling also appears in Register 12-2. Tables 12-2, 12-6, 12-7, 12-8, 12-9, 12-10, 12-11 and 12-12. Figures 12-8, 12-9, 12-10 and 12-11. Sections 12.2.2, 12.3.1 and 12.3.1.1.

TABLE 3-1: SPECIAL REGISTERS SUMMARY BANK 0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR Reset	Value on all other Resets(1)
Bank 0											
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	**$\overline{\text{T1SYNC}}$**	TMR1CS	TMR1ON	--00 0000	--uu uuuu
18h	RCSTA	SPEN	RX9	SREN	CREN	**ADDEN**	FERR	OERR	RX9D	0000 -00x	0000 -00x

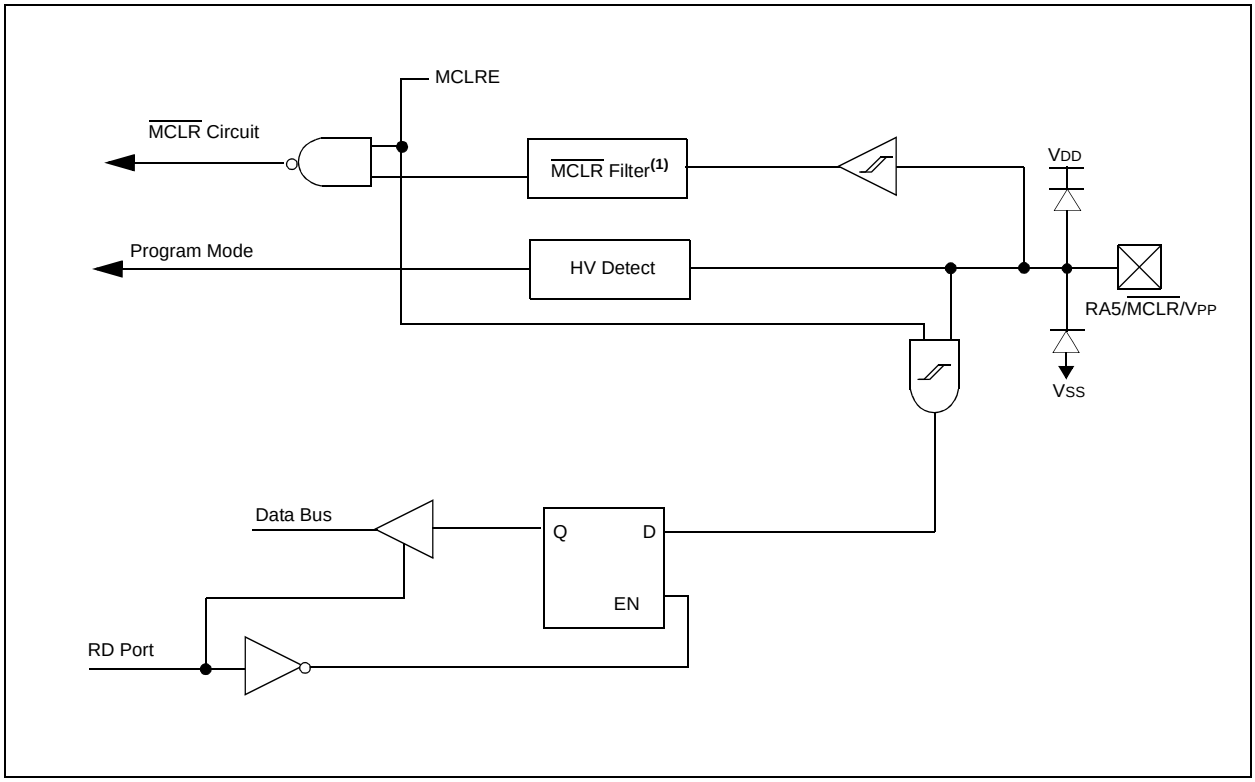
Legend: x = unknown, u = unchanged, - = unimplemented locations, read as ‘0’, q = value depends on condition, shaded = unimplemented

Note 1: Other (non power-up) Resets include $\overline{\text{MCLR}}$ Reset, Brown-out Reset and Watchdog Timer Reset during normal operation.

3. Module: I/O Ports (RA5/$\overline{MCLR}$/V_{PP})

Figure 5-5, “Block Diagram of the RA5/$\overline{MCLR}$/V_{PP} Pin”, is incorrect. The following diagram should be used instead.

FIGURE 5-5: BLOCK DIAGRAM OF RA5/$\overline{MCLR}$/V_{PP} PIN



4. Module: Comparator

Example 9-1, “Initializing Comparator Module”, is incorrect. The following code example should be used instead.

EXAMPLE 1: INITIALIZING COMPARATOR MODULE

```
        BCF         INTCON,GIE      ; Turn OFF Global Interrupts
        BCF         INTCON,PEIE     ; Turn OFF Peripheral Interrupts
        CLRF        PORTA           ; Init Port A
        MOVLW       0X03            ; Init comparator mode
        MOVWF       CMCON           ; CM<2:0> = 011
        BSF         STATUS,RP0      ; Select BANK 1
        MOVLW       0x07            ; Initialize Port A Direction
        MOVWF       TRISA           ; Set RA<2:0> as Inputs
                                    ; RA<4:3> as outputs
                                    ; TRIS<5> always reads '0'
        BCF         STATUS,RP0      ; Select BANK 0
        CALL        DELAY10         ; Wait 10us for comparator output to become valid
                                    ; See Table 17-1 Parameter 301
        MOVF        CMCON,F         ; Read CMCON to end change condition
        BCF         PIR1,CMIF       ; Clear pending interrupts
        BSF         STATUS,RP0      ; Select BANK 1
        BSF         PIE1,CMIE       ; Enable Comparator Interrupts
        BCF         STATUS,RP0      ; Select BANK 0
        BSF         INTCON,PEIE     ; Enable Peripheral Interrupts
        BSF         INTCON,GIE      ; Global Interrupt Enable

        ; Insert Your code....

        ; Helper function is the Delay for 10us routine show below.

DELAY10             ; burns 8 cycles + the call for 10 cycles or 10us at 4Mhz
        goto $+1    ; goto the next instruction and burn 2 cycles
        call retlbl ; goto the next instruction and burn 2 more cycles

retlblreturn; go back and burn 2 cycles (actually done 2x for 4 cycles consumed)
```

5. Module: Data EEPROM Memory

Examples 13-1, “Data EEPROM Read”, 13-2, “Data EEPROM Write”, and 13-3, “Write Verify”, are incorrect. The EEPROM registers are all located in Bank 1. The examples show the registers in Bank 0 and Bank 1. The following code examples should be used instead.

EXAMPLE 13-1: DATA EEPROM READ

```
  BSF     STATUS, RP0  ; Bank 1
  MOVLW   CONFIG_ADDR  ;
  MOVWF   EEADR        ; Address to write
  BSF     EECON1, RD   ; EE Read
  MOVF    EEDATA, W    ; W = EEDATA
  BCF     STATUS, RP0  ; Bank 0
```

EXAMPLE 13-2: DATA EEPROM WRITE

```
  ; set up the data and the address
  BSF     STATUS, RP0  ; Bank 1
  MOVLW   CONFIG_ADDR  ;
  MOVWF   EEADR        ; Address to write
  MOVLW   CONFIG_DATA  ;
  MOVWF   EEDATA       ; Data to write

                       ; perform the write
                         operation
  BSF     EECON1, WREN ; Enable Write
  BCF     INTCON, GIE  ; Disable INTs
  MOVLW   055h         ;
  MOVWF   EECON2       ; Write 55
  MOVLW   0AAh         ;
  MOVWF   EECON2       ; Write AA
  BSF     EECON1, WR   ; Set WR bit
  BCF     STATUS, RP0  ; Bank 0
```

EXAMPLE 13-3: WRITE VERIFY

```
; after the write in complete (i.e. in the
  write interrupt)
  BSF     STATUS, RP0 ; Bank 1
  MOVF    EEDATA, W   ; load the last
                        written value into W
  BSF     EECON1, RD  ; start a read
;
; Is the value written (in W Reg) and
; read (in EEDATA) the same?
;
  SUBWF   EEDATA, W   ; the EEDATA has fresh
                        data
  BTFSS   STATUS, Z   ; Is the Zero flag set?
  GOTO    WRITE_ERR   ; NO, Write Error
                      ; YES, Good Write
                      ; continue program
```

6. Module: Timer1 Module

In **Section 7.0, "Timer1 Module"**, in Register 7-1, bit TMR1ON, "Timer1 On" should read as shown in bold below:

REGISTER 7-1: T1CON: TIMER1 CONTROL REGISTER (ADDRESS: 10h)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON
bit 7							bit 0

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **T1CKPS1/T1CKPS0:** Timer1 Input Clock Prescale Select bits
11 = 1:8 prescale value
10 = 1:4 prescale value
01 = 1:2 prescale value
11 = 1:1 prescale value

bit 3 **T1OSCEN:** Timer1 Oscillator Enable Control bit
1 = Oscillator is enabled
0 = Oscillator is shut off**(1)**

bit 2 **$\overline{\text{T1SYNC}}$:** Timer1 External Clock Input Synchronization Control bit
TMR1CS = 1
1 = Do not synchronize external clock input
0 = Synchronize external clock input
TMR1CS = 0
This bit is ignored. Timer1 uses the internal clock when TRM1CS = 0.

bit 1 **TMR1CS:** Timer1 Clock Source Select bit
1 = External clock from pin RB6/T1OSO/T1CKI (on the rising edge)
0 = Internal clock (FOSC/4)

bit 0 **TMR1ON:** Timer1 On bit
1 = Enables Timer1
0 = Disables Timer1

Note 1: The oscillator inverter and feedback resistor are turned off to eliminate power drain.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

REVISION HISTORY

Rev A Document (6/00)

Original errata document.

Rev B Document (11/00)

Issue 3 (CCP Compare Mode), Table 1 and 2 were added (page 2).

Under the Clarifications/Corrections Section, Item 1, Table 15-12 was updated with additional information (page 3).

Rev C Document (6/01)

Issues 2 and 3 were added.

Under Clarifications/Corrections, Items 2 and 3 were changed and Item numbers were renumbered accordingly.

Rev D Document (9/01)

Item 3 was rewritten (page 9).

Under the Clarifications/Corrections to the Data Sheet Section, the following items were changed:

Item 2, Tables 17.1 and 17.2, were updated with minor changes.

Item 6 was added.

Rev E Document (2/02)

Under Clarifications/Corrections to the Data Sheet, added Module 3: I/O Ports (RA5/$\overline{MCLR}$/V_{PP}).

Rev G Document (05/19/05)

Under Clarifications/Corrections to the Data Sheet, Added Module 6: Timer1 Module.

Rev H Document (06/12)

Corrected Silicon Revision.

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