

# PHD98N03LT

N-channel TrenchMOS logic level FET

Rev. 05 — 1 December 2006

Product data sheet

## 1. Product profile

### 1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology.

### 1.2 Features

- Low on-state resistance
- Fast switching

### 1.3 Applications

- Computer motherboard high-frequency DC-to-DC converters

### 1.4 Quick reference data

- $V_{DS} \leq 25\text{ V}$
- $I_D \leq 75\text{ A}$
- $R_{DS(on)} \leq 5.9\text{ m}\Omega$
- $Q_{GD} = 15\text{ nC (typ)}$

## 2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Symbol
1	gate (G)	<p>SOT428 (DPAK)</p>	
2	drain (D) <a href="#">[1]</a>		
3	source (S)		
mb	mounting base; connected to drain (D)		

[1] It is not possible to make a connection to pin 2.

### 3. Ordering information

**Table 2. Ordering information**

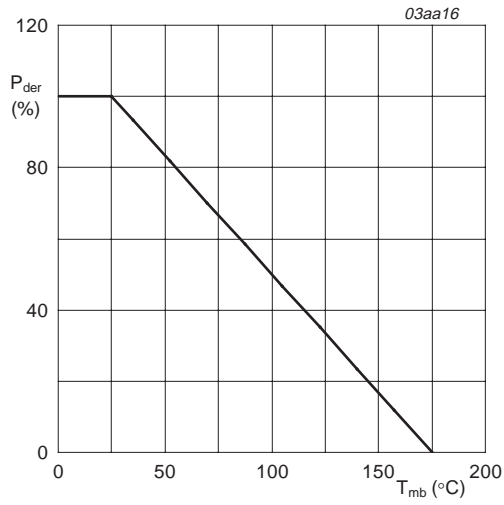
Type number	Package		Version
	Name	Description	
PHD98N03LT	DPAK	plastic single-ended surface-mounted package; 3 leads (one lead cropped)	SOT428

### 4. Limiting values

**Table 3. Limiting values**

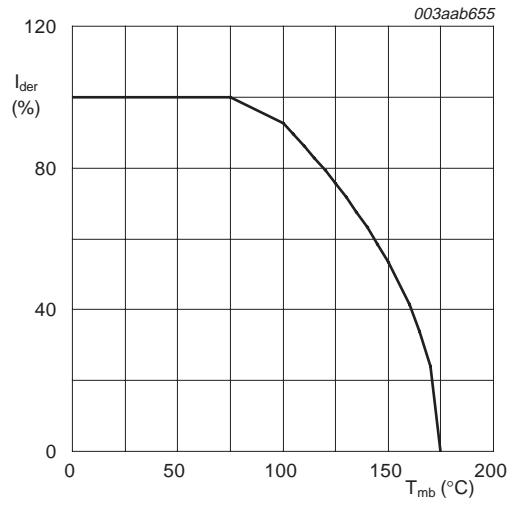
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	25	V
$V_{DGR}$	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 175\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	25	V
$V_{GS}$	gate-source voltage		-	$\pm 20$	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}$ ; $V_{GS} = 5\text{ V}$ ; see <a href="#">Figure 2</a> and <a href="#">3</a>	-	75	A
		$T_{mb} = 100\text{ °C}$ ; $V_{GS} = 5\text{ V}$ ; see <a href="#">Figure 2</a>	-	66	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; see <a href="#">Figure 3</a>	-	240	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 1</a>	-	111	W
$T_{stg}$	storage temperature		-55	+175	$^{\circ}\text{C}$
$T_j$	junction temperature		-55	+175	$^{\circ}\text{C}$
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25\text{ °C}$	-	75	A
$I_{SM}$	peak source current	$T_{mb} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	240	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 43\text{ A}$ ; $t_p = 0.27\text{ ms}$ ; $V_{DS} = 15\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 5\text{ V}$ ; starting at $T_j = 25\text{ °C}$	-	183	mJ



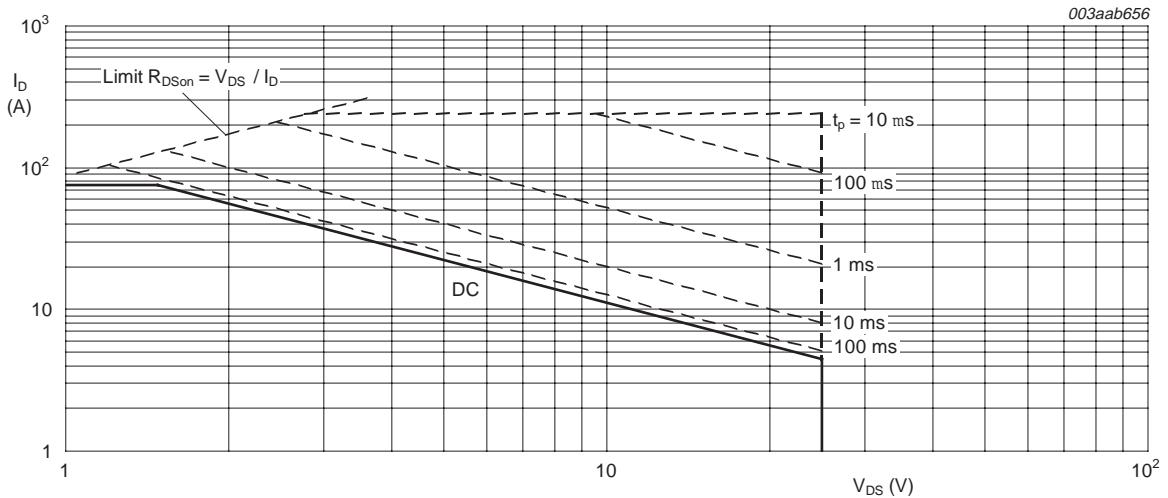
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature



T<sub>mb</sub> = 25 °C; I<sub>DM</sub> is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

### 5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	-	1.35	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient					
	SOT428	minimum footprint	-	75	-	K/W
		SOT404 minimum footprint	[1]	50	-	K/W

[1] Mounted on a printed-circuit board; vertical in still air.

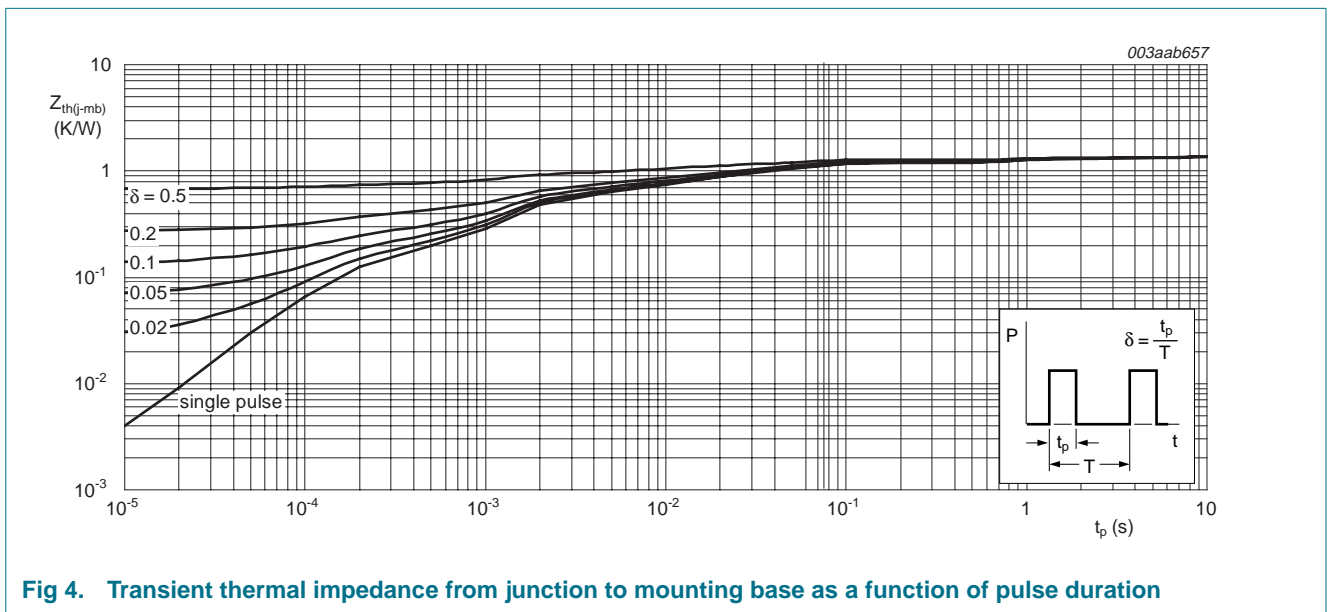
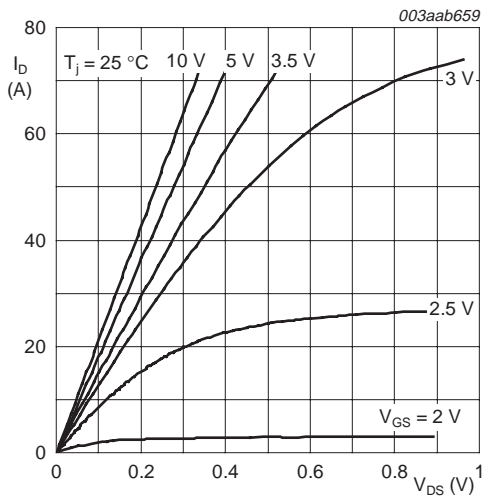


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 6. Characteristics

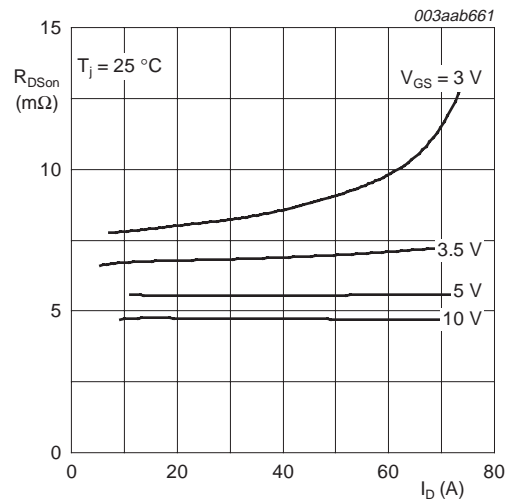
**Table 5. Characteristics**
*T<sub>j</sub> = 25 °C unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V				
		T <sub>j</sub> = 25 °C	25	-	-	V
		T <sub>j</sub> = -55 °C	22	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; see <a href="#">Figure 9</a> and <a href="#">10</a>				
		T <sub>j</sub> = 25 °C	1	1.5	2	V
		T <sub>j</sub> = 175 °C	0.5	-	-	V
		T <sub>j</sub> = -55 °C	-	-	2.3	V
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = 25 V; V <sub>GS</sub> = 0 V				
		T <sub>j</sub> = 25 °C	-	0.05	1	μA
		T <sub>j</sub> = 175 °C	-	-	500	μA
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = ±15 V; V <sub>DS</sub> = 0 V	-	10	100	nA
R <sub>DS(on)</sub>	drain-source on-state resistance	V <sub>GS</sub> = 5 V; I <sub>D</sub> = 25 A; see <a href="#">Figure 6</a> and <a href="#">8</a>				
		T <sub>j</sub> = 25 °C	-	6.2	7.3	mΩ
		T <sub>j</sub> = 175 °C	-	10.5	12.4	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; see <a href="#">Figure 6</a> and <a href="#">8</a>	-	5.2	5.9	mΩ
<b>Dynamic characteristics</b>						
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 50 A; V <sub>DS</sub> = 15 V; V <sub>GS</sub> = 5 V; see <a href="#">Figure 11</a> and <a href="#">12</a>	-	40	-	nC
Q <sub>GS</sub>	gate-source charge		-	16	-	nC
Q <sub>GD</sub>	gate-drain charge		-	15	-	nC
C <sub>iss</sub>	input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 20 V; f = 1 MHz; see <a href="#">Figure 14</a>	-	3000	-	pF
C <sub>oss</sub>	output capacitance		-	710	-	pF
C <sub>rss</sub>	reverse transfer capacitance		-	510	-	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 15 V; I <sub>D</sub> = 12.5 A; V <sub>GS</sub> = 5 V; R <sub>G</sub> = 5.6 Ω	-	18	-	ns
t <sub>r</sub>	rise time		-	80	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	104	-	ns
t <sub>f</sub>	fall time		-	104	-	ns
<b>Source-drain diode</b>						
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 25 A; V <sub>GS</sub> = 0 V; see <a href="#">Figure 13</a>	-	0.9	1.2	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 10 A; di <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V	-	37	-	ns
Q <sub>r</sub>	recovered charge		-	20	-	nC



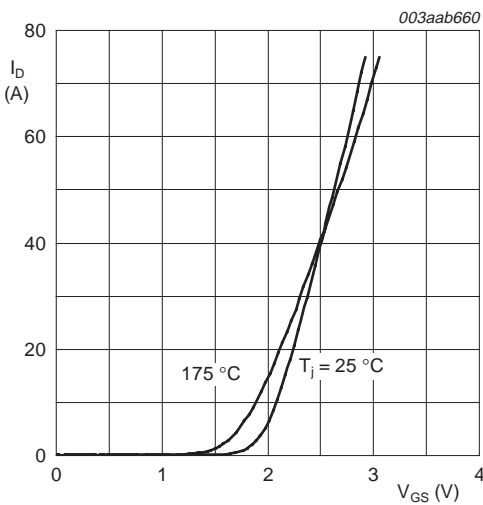
$T_j = 25\text{ °C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



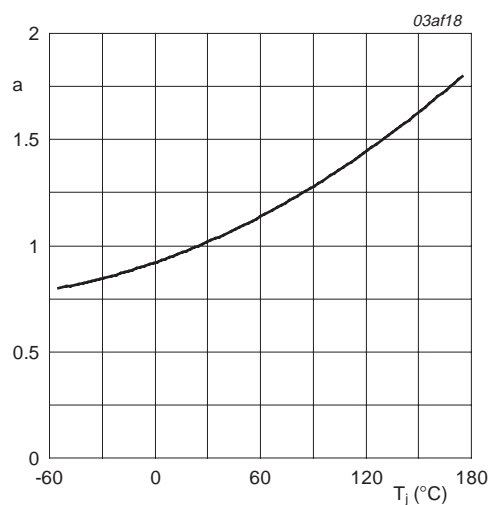
$T_j = 25\text{ °C}$

Fig 6. Drain-source on-state resistance as a function of drain current; typical values



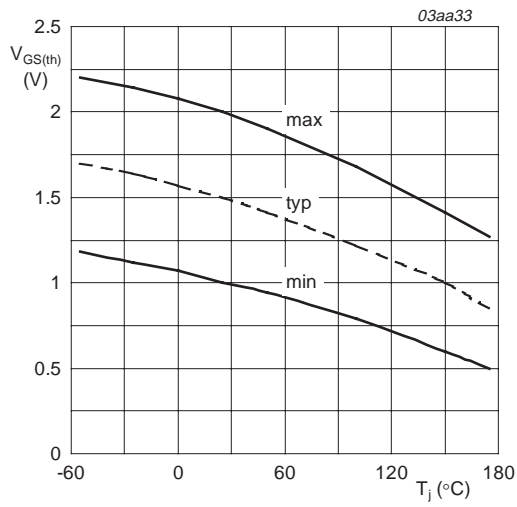
$T_j = 25\text{ °C and } 175\text{ °C}; V_{DS} > I_D \times R_{DS(on)}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



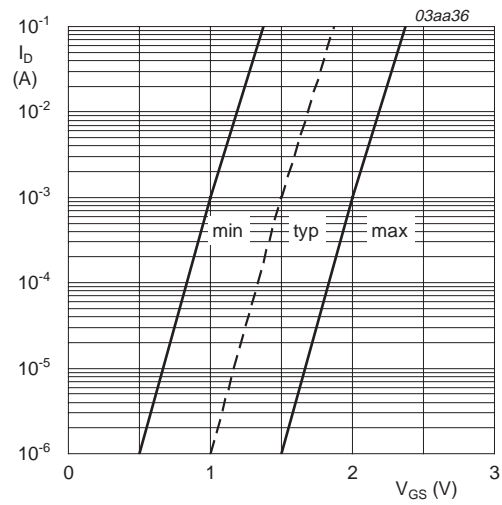
$$a = \frac{R_{DS(on)}}{R_{DS(on)(25\text{ °C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



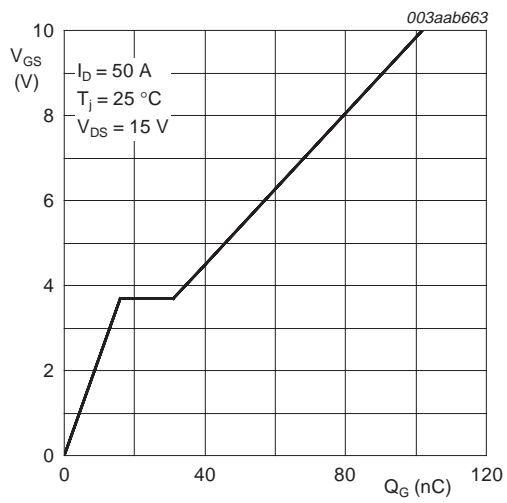
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

**Fig 9. Gate-source threshold voltage as a function of junction temperature**



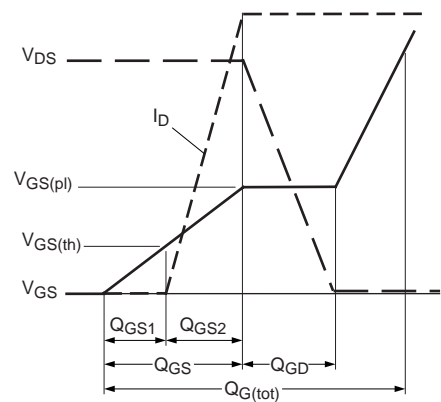
$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = 5 \text{ V}$

**Fig 10. Sub-threshold drain current as a function of gate-source voltage**

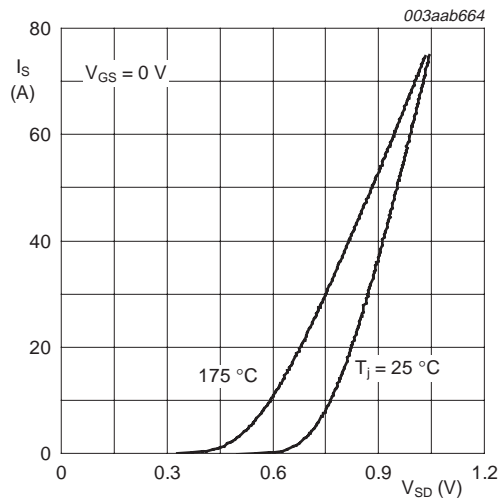


$I_D = 50 \text{ A}; V_{DS} = 15 \text{ V}$

**Fig 11. Gate-source voltage as a function of gate charge; typical values**

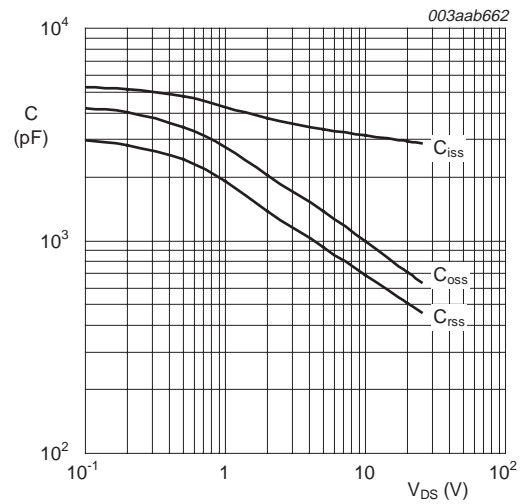


**Fig 12. Gate charge waveform definitions**



$T_j = 25\text{ }^\circ\text{C}$  and  $175\text{ }^\circ\text{C}$ ;  $V_{GS} = 0\text{ V}$

**Fig 13. Source current as a function of source-drain voltage; typical values**



$V_{GS} = 0\text{ V}$ ;  $f = 1\text{ MHz}$

**Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



7. Package outline

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)

SOT428

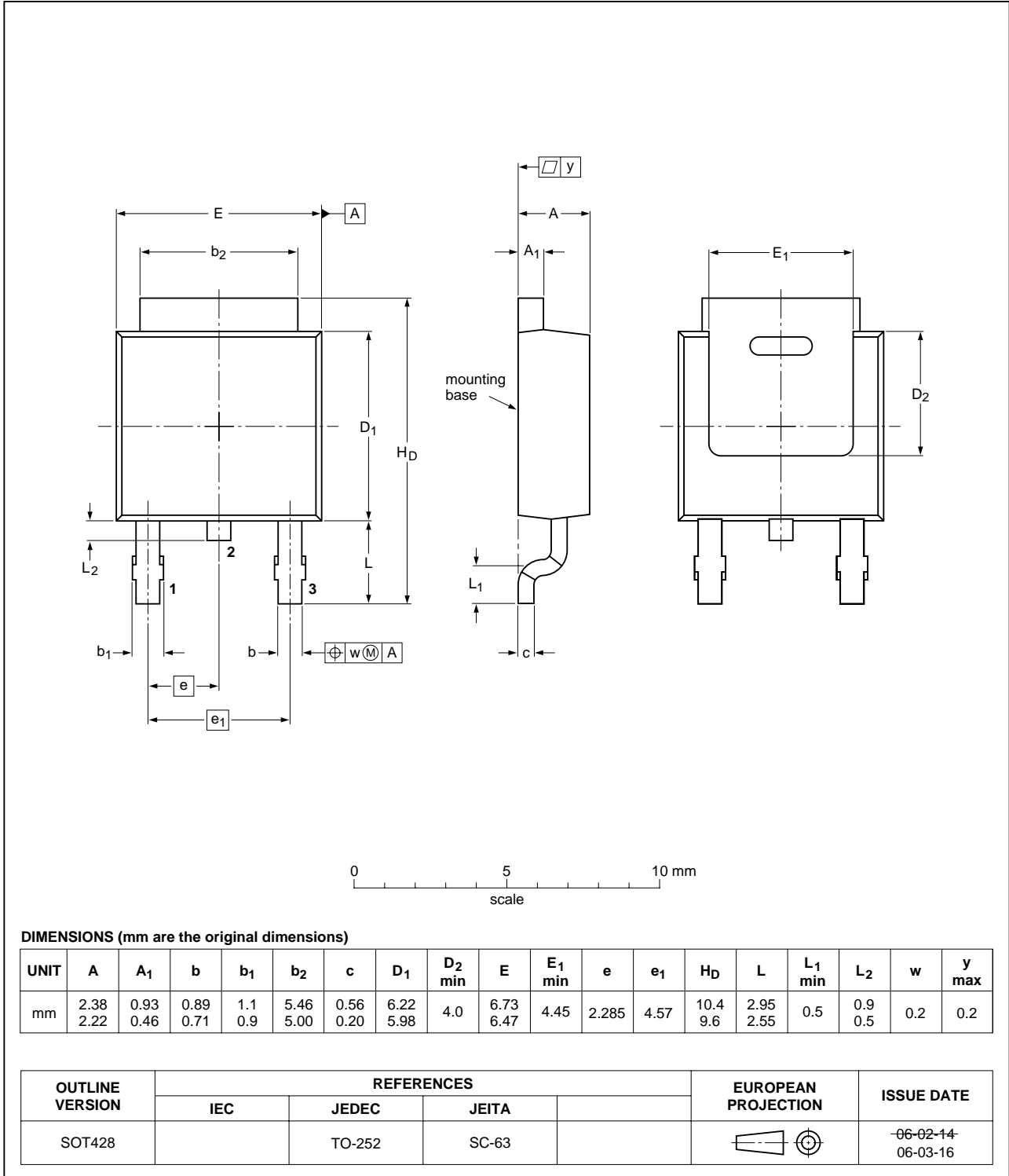


Fig 15. Package outline SOT428 (DPAK)

## 8. Revision history

**Table 6. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHD98N03LT_5	20061201	Product data sheet	-	PHP98N03LT-04
Modifications:				
				<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>• Legal texts have been adapted to the new company name where appropriate.</li><li>• PHP_PHB98N03LT have been discontinued.</li></ul>
PHP98N03LT-04	20021021	Product data	-	PHP98N03LT-03
PHP98N03LT-03 (9397 750 09287)	20020220	Product data	-	PHP98N03LT-02
PHP98N03LT-02 (9397 750 08726)	20011018	Product data	-	PHP98N03LT-01
PHP98N03LT-01 (9397 750 08338)	20010716	Product data	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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