

FEATURES

- Specified from -55°C to $+125^{\circ}\text{C}$
 - 0.9 $\mu\text{V}/^{\circ}\text{C}$ maximum input offset average TC
 - 10 ppm/ $^{\circ}\text{C}$ maximum gain vs. temperature ($G = 1$)
- Excellent ac specifications
 - 80 dB minimum CMRR at 10 kHz ($G = 1$)
 - 3 dB bandwidth: 825 kHz typical ($G = 1$)
 - 2 V/ μs typical slew rate
- Low noise
 - 8 nV/ $\sqrt{\text{Hz}}$, at 1 kHz, maximum input voltage noise
 - 0.25 μV p-p RTI ($G = 100$ to 1000)
- High accuracy dc performance
 - 80 dB minimum CMRR DC to 60 Hz ($G = 1$)
 - 70 μV maximum input offset voltage
 - 2 nA maximum input bias current
- Wide power supply range: ± 2.3 V to ± 18 V
- Available in space-saving MSOP
- Gain set with 1 external resistor (gain range 1 to 1000)

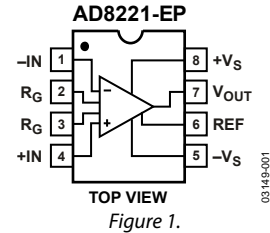
ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC standard)
- Military temperature range (-55°C to $+125^{\circ}\text{C}$)
- Controlled manufacturing baseline
- One assembly/test site
- One fabrication site
- Enhanced product change notification
- Qualification data available on request

APPLICATIONS

- Bridge amplifiers
- Precision data acquisition systems
- Strain gages
- Transducer interfaces

TYPICAL CONNECTION DIAGRAM



GENERAL DESCRIPTION

The **AD8221-EP** is a gain programmable, high performance instrumentation amplifier that delivers the industry's highest CMRR over frequency in its class. The CMRR of instrumentation amplifiers on the market today falls off at 200 Hz. In contrast, the **AD8221-EP** maintains a minimum CMRR of 80 dB to 10 kHz at $G = 1$. High CMRR over frequency allows the **AD8221-EP** to reject wideband interference and line harmonics, greatly simplifying filter requirements.

Possible applications include precision data acquisition, biomedical analysis, and aerospace instrumentation.

Low voltage offset, low offset drift, low gain drift, high gain accuracy, and high CMRR make this device an excellent choice in applications that demand the best dc performance possible, such as bridge signal conditioning.

Programmable gain affords the user design flexibility. A single resistor sets the gain from 1 to 1000. The **AD8221-EP** operates on both single and dual supplies and is well suited for applications where ± 10 V input voltages are encountered.

The **AD8221-EP** is specified over the -55°C to $+125^{\circ}\text{C}$ military temperature range. It is available in an 8-lead MSOP package.

Additional application and technical information can be found in the **AD8221** data sheet.

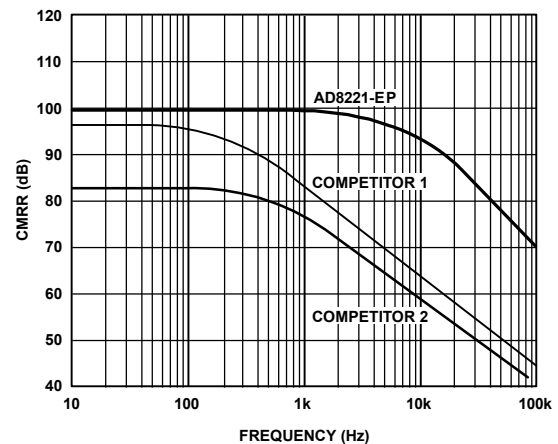


Figure 2. Typical CMRR vs. Frequency for $G = 1$

Rev. 0

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REVISION HISTORY

4/16—Revision 0: Initial Version

SPECIFICATIONS

$V_S = \pm 15\text{ V}$, $V_{REF} = 0\text{ V}$, $T_A = 25^\circ\text{C}$, $G = 1$, $R_L = 2\text{ k}\Omega$, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
COMMON-MODE REJECTION RATIO (CMRR)					
CMRR DC to 60 Hz with 1 k Ω Source Imbalance	$V_{CM} = -10\text{ V to }+10\text{ V}$				
$G = 1$		80			dB
$G = 10$		100			dB
$G = 100$		120			dB
$G = 1000$		130			dB
CMRR at 10 kHz	$V_{CM} = -10\text{ V to }+10\text{ V}$				
$G = 1$		80			dB
$G = 10$		90			dB
$G = 100$		100			dB
$G = 1000$		100			dB
NOISE					
Voltage Noise, 1 kHz	RTI noise = $\sqrt{e_{NI}^2 + (e_{NO}/G)^2}$				
Input Voltage Noise, e_{NI}	$V_{IN+}, V_{IN-}, V_{REF} = 0$			8	nV/ $\sqrt{\text{Hz}}$
Output Voltage Noise, e_{NO}				75	nV/ $\sqrt{\text{Hz}}$
Referred to Input (RTI)	$f = 0.1\text{ Hz to }10\text{ Hz}$				
$G = 1$			2		$\mu\text{V p-p}$
$G = 10$			0.5		$\mu\text{V p-p}$
$G = 100\text{ to }1000$			0.25		$\mu\text{V p-p}$
Current Noise	$f = 1\text{ kHz}$		40		fA/ $\sqrt{\text{Hz}}$
	$f = 0.1\text{ Hz to }10\text{ Hz}$		6		pA p-p
VOLTAGE OFFSET¹					
Input Offset, V_{OSI}	$V_S = \pm 5\text{ V to } \pm 15\text{ V}$			70	μV
Over Temperature	$T_A = -55^\circ\text{C to }+125^\circ\text{C}$			150	μV
Average Temperature Coefficient (TC)				0.9	$\mu\text{V}/^\circ\text{C}$
Output Offset, V_{OSO}	$V_S = \pm 5\text{ V to } \pm 15\text{ V}$			600	μV
Over Temperature	$T_A = -55^\circ\text{C to }+125^\circ\text{C}$			1.2	mV
Average TC				9	$\mu\text{V}/^\circ\text{C}$
Offset RTI vs. Supply (PSR)	$V_S = \pm 2.3\text{ V to } \pm 18\text{ V}$				
$G = 1$		90	100		dB
$G = 10$		100	120		dB
$G = 100$		120	140		dB
$G = 1000$		120	140		dB
INPUT CURRENT					
Input Bias Current			0.5	2	nA
Over Temperature	$T_A = -55^\circ\text{C to }+125^\circ\text{C}$			3.75	nA
Average TC			11		pA/ $^\circ\text{C}$
Input Offset Current			0.3	1	nA
Over Temperature	$T_A = -55^\circ\text{C to }+125^\circ\text{C}$			2.25	nA
Average TC			7		pA/ $^\circ\text{C}$
REFERENCE INPUT					
R_{IN}			20		k Ω
I_{IN}	$V_{IN+}, V_{IN-}, V_{REF} = 0$		50	60	μA
Voltage Range		$-V_S$		$+V_S$	V
Gain to Output			1 ± 0.0001		V/V

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Range	$V_S = \pm 2.3 \text{ V to } \pm 18 \text{ V}$	± 2.3		± 18	V
Quiescent Current			0.9	1	mA
Over Temperature	$T_A = -55^\circ\text{C to } +125^\circ\text{C}$		1	1.2	mA
DYNAMIC RESPONSE					
Small Signal -3 dB Bandwidth					
$G = 1$			825		kHz
$G = 10$			562		kHz
$G = 100$			100		kHz
$G = 1000$			14.7		kHz
Settling Time 0.01%	10 V step				
$G = 1 \text{ to } 100$			10		μs
$G = 1000$			80		μs
Settling Time 0.001%	10 V step				
$G = 1 \text{ to } 100$			13		μs
$G = 1000$			110		μs
Slew Rate	$G = 1$	1.5	2		$\text{V}/\mu\text{s}$
	$G = 5 \text{ to } 100$	2	2.5		$\text{V}/\mu\text{s}$
GAIN					
Gain Range	$G = 1 + (49.4 \text{ k}\Omega/R_G)$	1		1000	V/V
Gain Error	$V_{\text{OUT}} \pm 10 \text{ V}$				
$G = 1$				0.1	%
$G = 10$				0.3	%
$G = 100$				0.3	%
$G = 1000$				0.3	%
Gain Nonlinearity	$V_{\text{OUT}} = -10 \text{ V to } +10 \text{ V}$				
$G = 1 \text{ to } 10$	$R_L = 10 \text{ k}\Omega$		5	15	ppm
$G = 100$	$R_L = 10 \text{ k}\Omega$		7	20	ppm
$G = 1000$	$R_L = 10 \text{ k}\Omega$		10	50	ppm
$G = 1 \text{ to } 100$	$R_L = 2 \text{ k}\Omega$		15	100	ppm
Gain vs. Temperature					
$G = 1$			3	10	ppm/ $^\circ\text{C}$
$G > 1^2$				-50	ppm/ $^\circ\text{C}$
INPUT					
Input Impedance					
Differential			100 2		$\text{G}\Omega \text{pF}$
Common Mode			100 2		$\text{G}\Omega \text{pF}$
Input Operating Voltage Range ³	$V_S = \pm 2.3 \text{ V to } \pm 5 \text{ V}$	$-V_S + 1.9$		$+V_S - 1.1$	V
Over Temperature	$T_A = -55^\circ\text{C to } +125^\circ\text{C}$	$-V_S + 2.0$		$+V_S - 1.2$	V
Input Operating Voltage Range	$V_S = \pm 5 \text{ V to } \pm 18 \text{ V}$	$-V_S + 1.9$		$+V_S - 1.2$	V
Over Temperature	$T_A = -55^\circ\text{C to } +125^\circ\text{C}$	$-V_S + 2.0$		$+V_S - 1.3$	V
OUTPUT					
Output Swing	$R_L = 10 \text{ k}\Omega$				
$V_S = \pm 2.3 \text{ V to } \pm 5 \text{ V}$		$-V_S + 1.1$		$+V_S - 1.2$	V
Over Temperature	$T_A = -55^\circ\text{C to } +125^\circ\text{C}$	$-V_S + 1.4$		$+V_S - 1.3$	V
Output Swing	$V_S = \pm 5 \text{ V to } \pm 18 \text{ V}$	$-V_S + 1.2$		$+V_S - 1.4$	V
Over Temperature	$T_A = -55^\circ\text{C to } +125^\circ\text{C}$	$-V_S + 1.6$		$+V_S - 1.5$	V
Short-Circuit Current			18		mA
TEMPERATURE RANGE					
Specified Performance		-55		+125	$^\circ\text{C}$

¹ Total RTI $V_{\text{OS}} = (V_{\text{OSI}}) + (V_{\text{OSO}}/G)$.

² Does not include the effects of external resistor R_G .

³ One input grounded. $G = 1$.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	± 18 V
Internal Power Dissipation	200 mW
Output Short-Circuit Current	Indefinite
Input Voltage (Common-Mode)	$\pm V_s$
Differential Input Voltage	$\pm V_s$
Storage Temperature Range	-65°C to $+150^{\circ}\text{C}$
Operating Temperature Range	-55°C to $+125^{\circ}\text{C}$

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

Specification for a device in free air.

Table 3.

Package	θ_{JA}	Unit
8-Lead MSOP, 4-Layer JEDEC Board	135	$^{\circ}\text{C}/\text{W}$

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

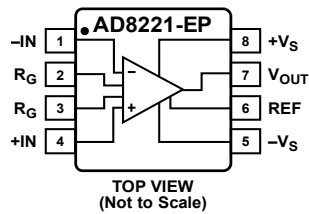


Figure 3. Pin Configuration

13702-103

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	-IN	Negative Input Terminal.
2, 3	R _G	Gain Setting Terminal. Place resistor across the R _G pins to set the gain. $G = 1 + (49.4 \text{ k}\Omega/R_G)$.
4	+IN	Positive Input Terminal.
5	-V _S	Negative Power Supply Terminal.
6	REF	Reference Voltage Terminal. Drive this terminal with a low impedance voltage source to level-shift the output.
7	V _{OUT}	Output Terminal.
8	+V _S	Positive Power Supply Terminal.

TYPICAL PERFORMANCE CHARACTERISTICS

T = 25°C, V_S = ±15 V, R_L = 10 kΩ, unless otherwise noted.

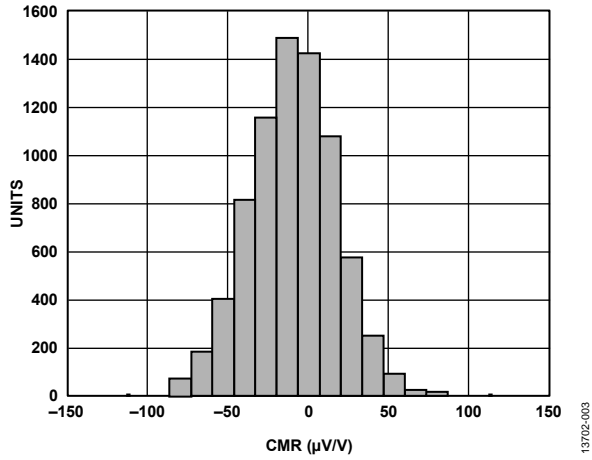


Figure 4. Typical Distribution for CMR (G = 1)

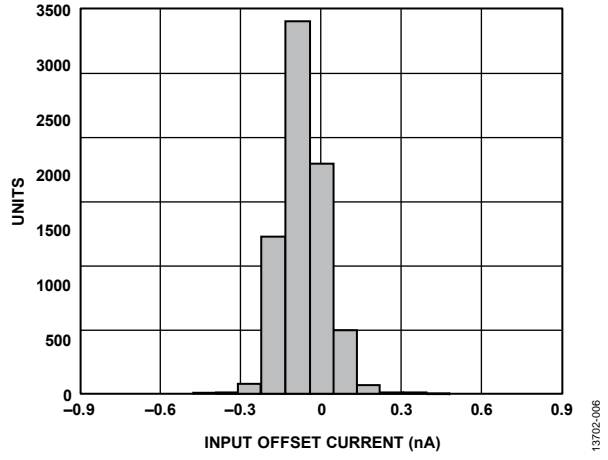


Figure 7. Typical Distribution of Input Offset Current

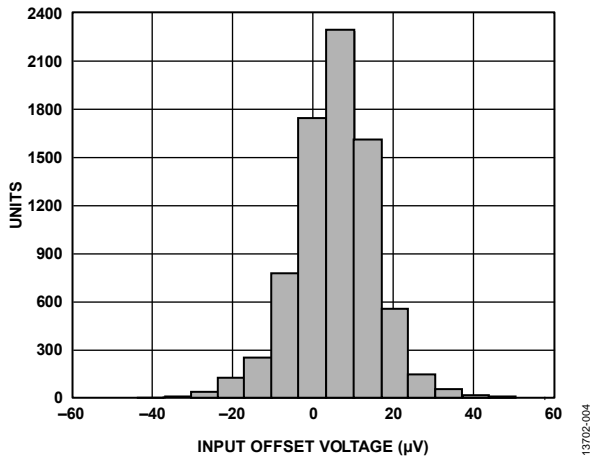


Figure 5. Typical Distribution of Input Offset Voltage

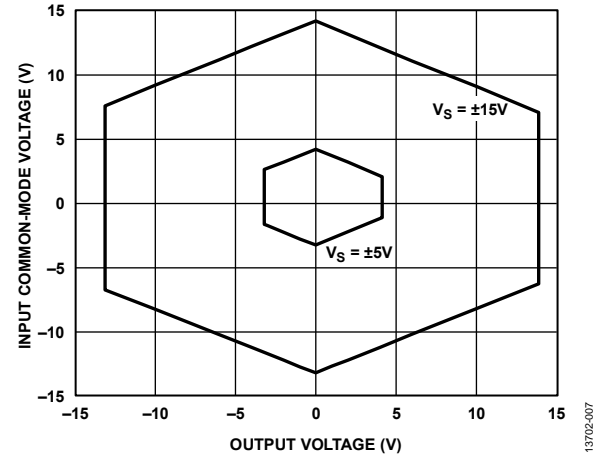


Figure 8. Input Common-Mode Voltage vs. Output Voltage, G = 1

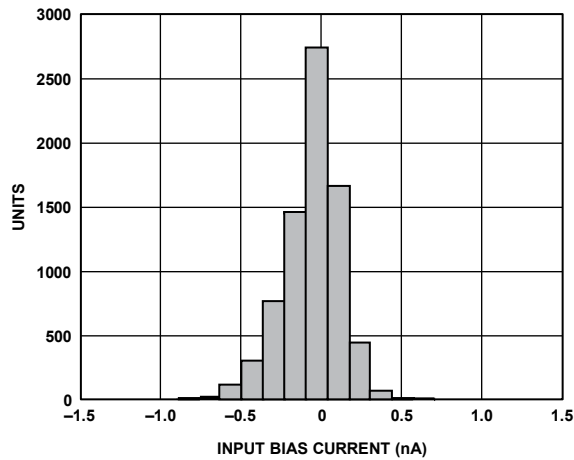


Figure 6. Typical Distribution of Input Bias Current

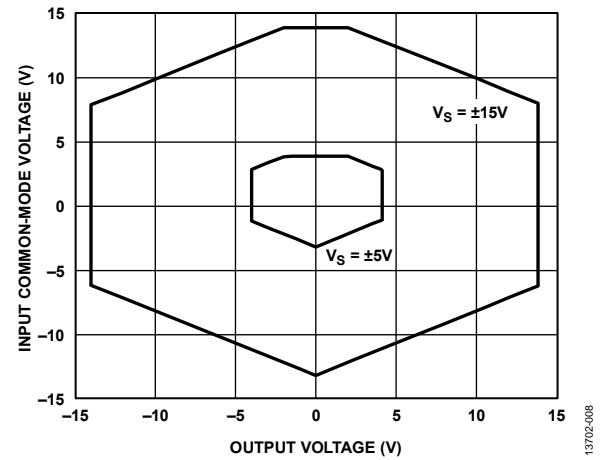


Figure 9. Input Common-Mode Voltage vs. Output Voltage, G = 100

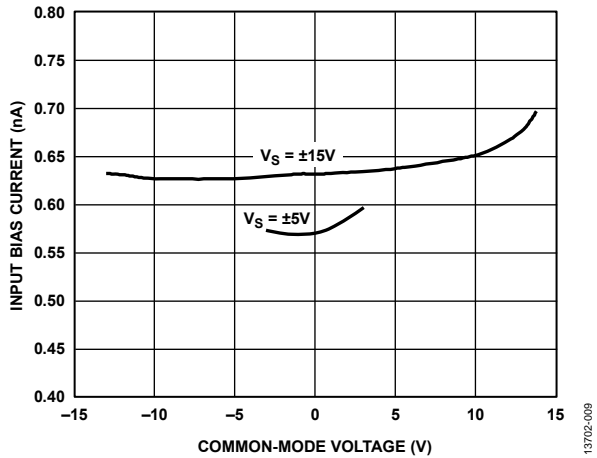


Figure 10. Input Bias Current (I_{BIAS}) vs. Common-Mode Voltage (CMV)

13702-009

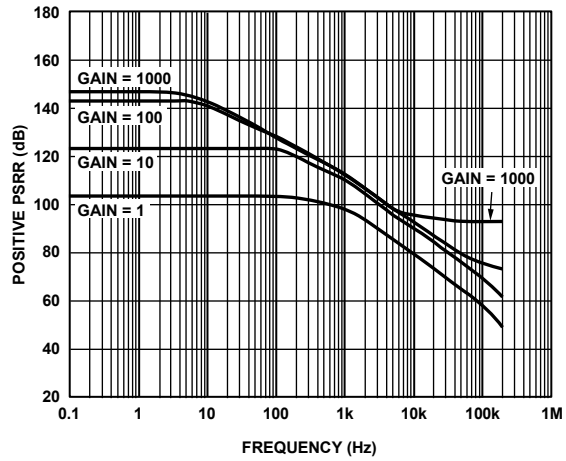


Figure 13. Positive PSRR vs. Frequency, RTI ($G = 1$ to 1000)

13702-012

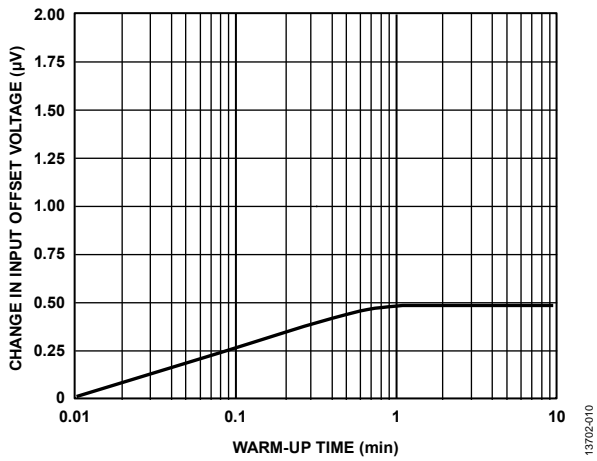


Figure 11. Change in Input Offset Voltage vs. Warm-Up Time

13702-010

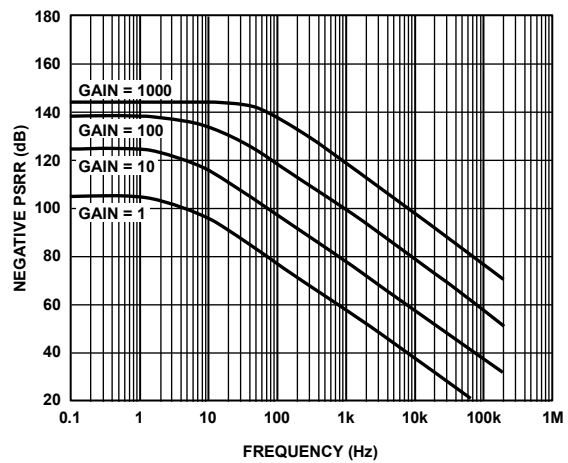


Figure 14. Negative PSRR vs. Frequency, RTI ($G = 1$ to 1000)

13702-013

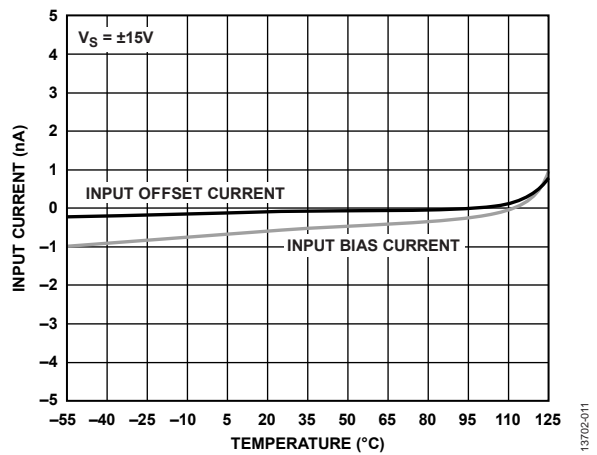


Figure 12. Input Offset Current and Input Bias Current vs. Temperature

13702-011

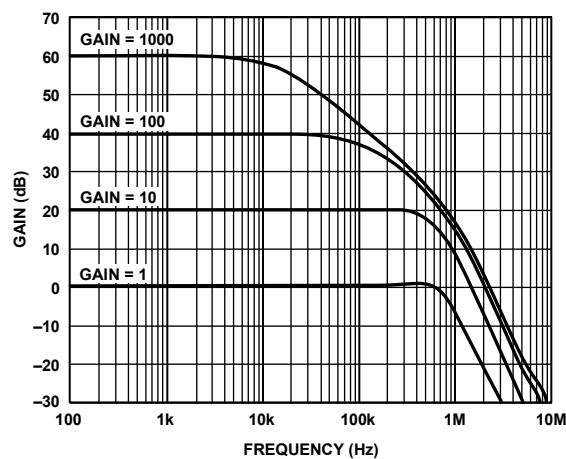


Figure 15. Gain vs. Frequency

13702-015

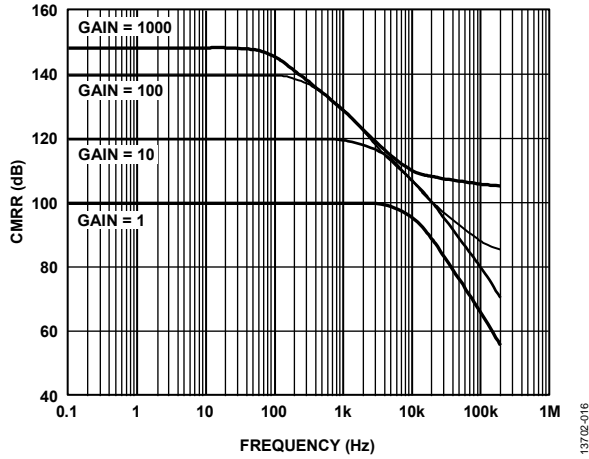


Figure 16. CMRR vs. Frequency, RTI

13702-016

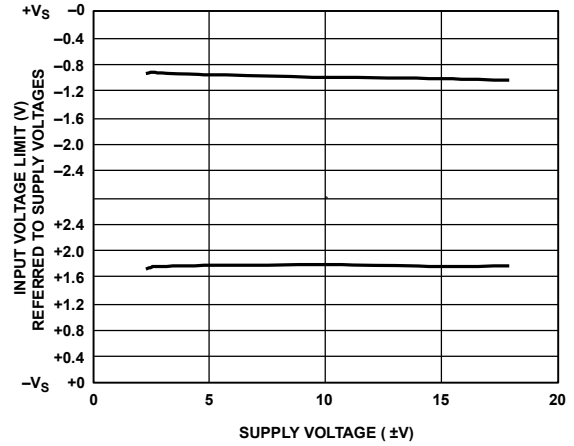


Figure 19. Input Voltage Limit vs. Supply Voltage, $G = 1$

13702-019

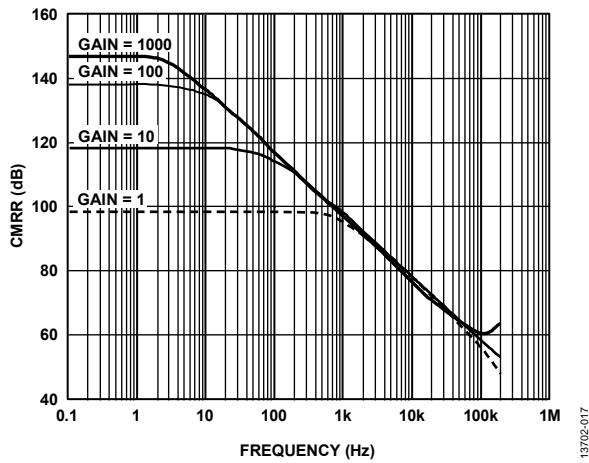


Figure 17. CMRR vs. Frequency, RTI, 1 k Ω Source Imbalance

13702-017

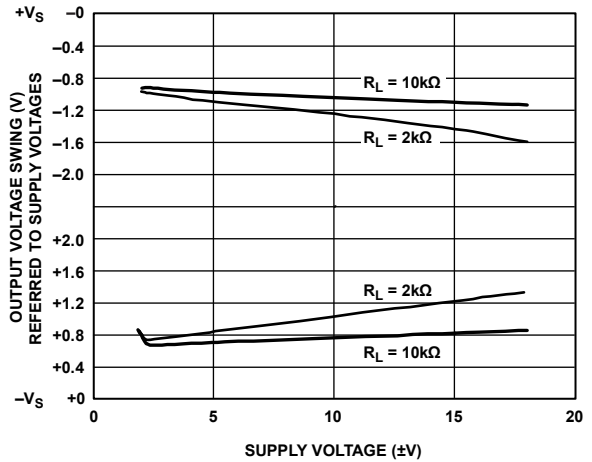


Figure 20. Output Voltage Swing vs. Supply Voltage, $G = 1$

13702-020

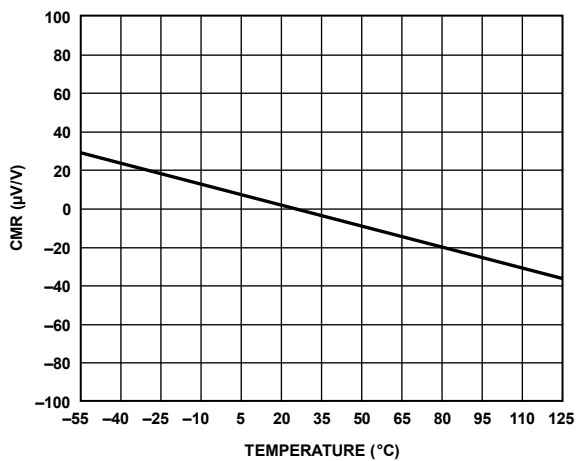


Figure 18. CMR vs. Temperature

13702-018

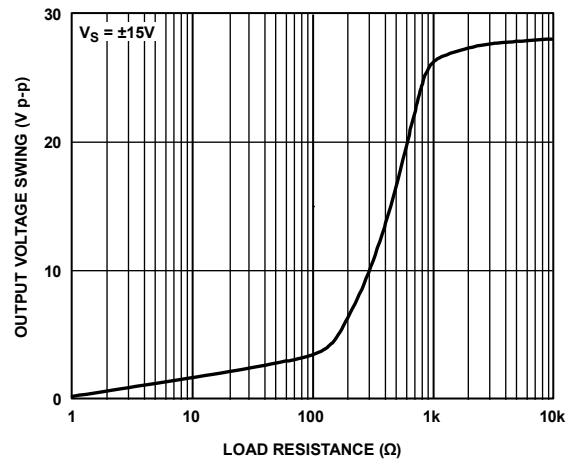


Figure 21. Output Voltage Swing vs. Load Resistance

13702-021

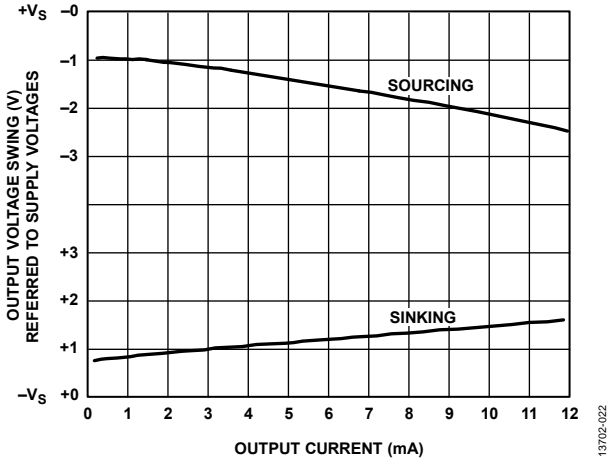


Figure 22. Output Voltage Swing vs. Output Current, $G = 1$

13702-022

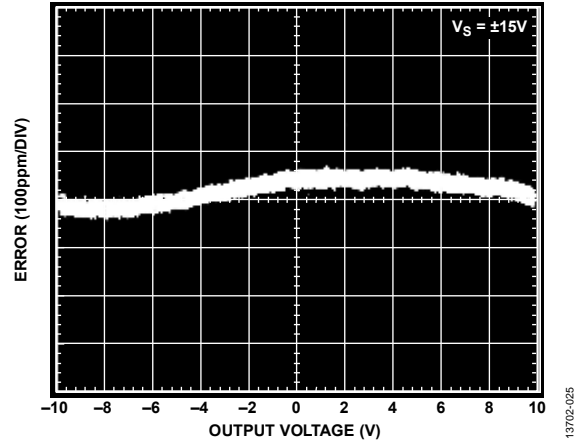


Figure 25. Gain Nonlinearity, $G = 1000$, $R_L = 10\text{ k}\Omega$

13702-025

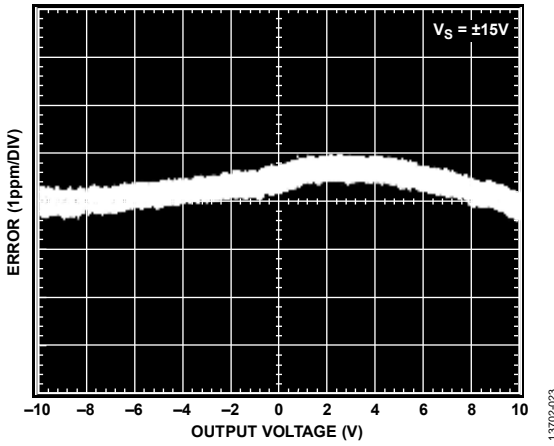


Figure 23. Gain Nonlinearity, $G = 1$, $R_L = 10\text{ k}\Omega$

13702-023

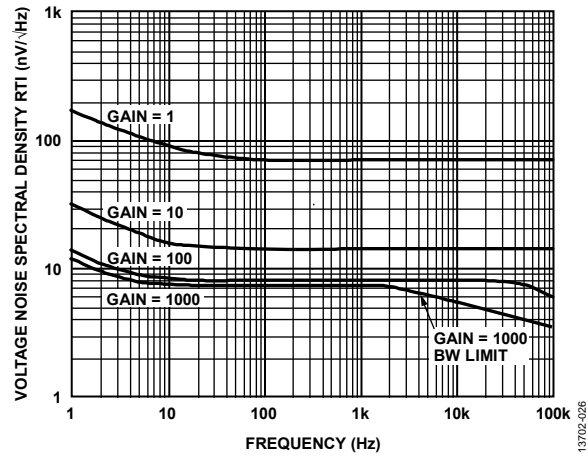


Figure 26. Voltage Noise Spectral Density vs. Frequency ($G = 1$ to 1000)

13702-026

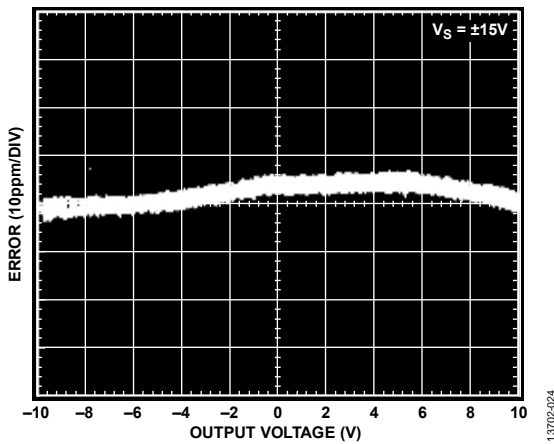


Figure 24. Gain Nonlinearity, $G = 100$, $R_L = 10\text{ k}\Omega$

13702-024

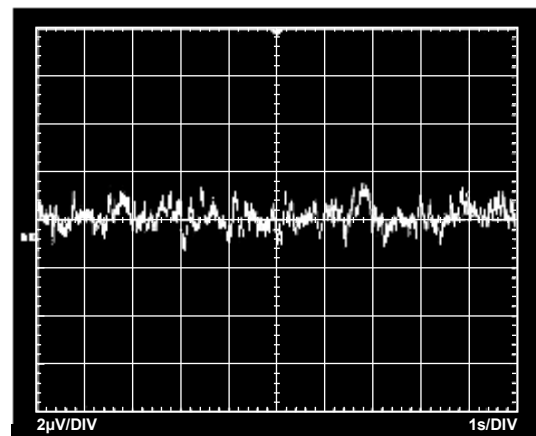


Figure 27. 0.1 Hz to 10 Hz RTI Voltage Noise ($G = 1$)

13702-027

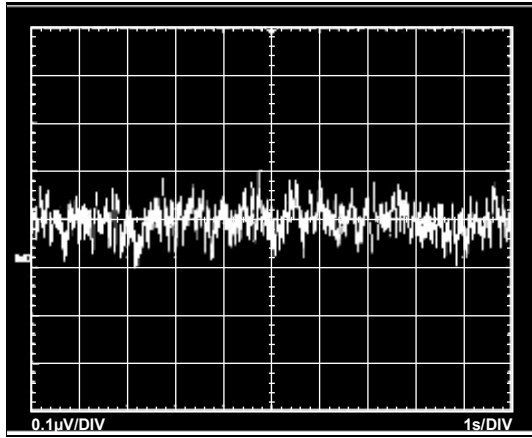


Figure 28. 0.1 Hz to 10 Hz RTI Voltage Noise ($G = 1000$)

13702-028

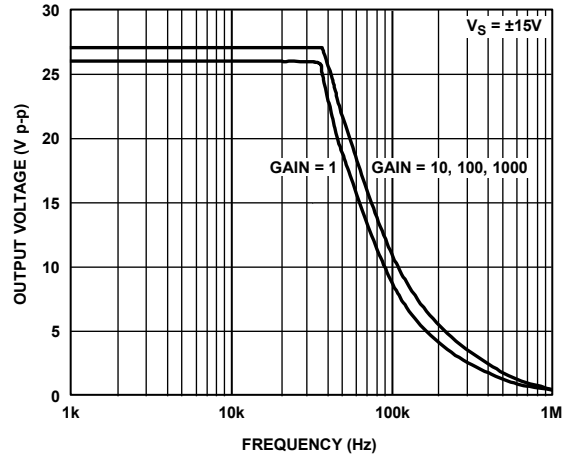


Figure 31. Large Signal Frequency Response

13702-031

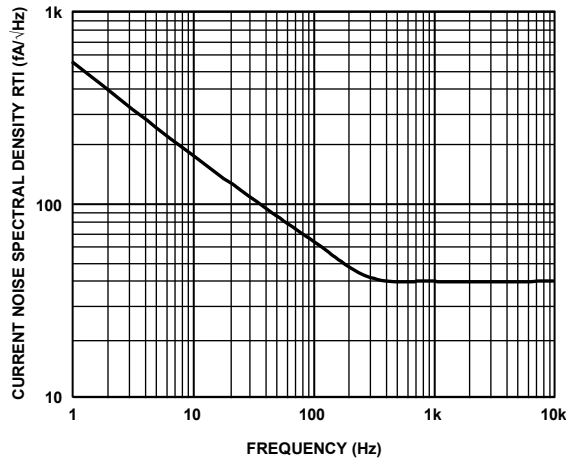


Figure 29. Current Noise Spectral Density vs. Frequency

13702-029

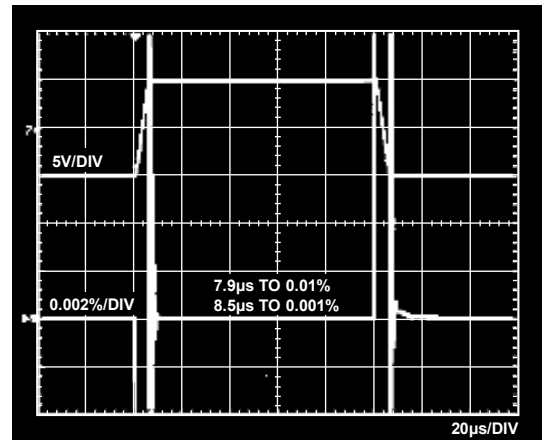


Figure 32. Large Signal Pulse Response and Settling Time ($G = 1$), 0.002%/DIV

13702-032

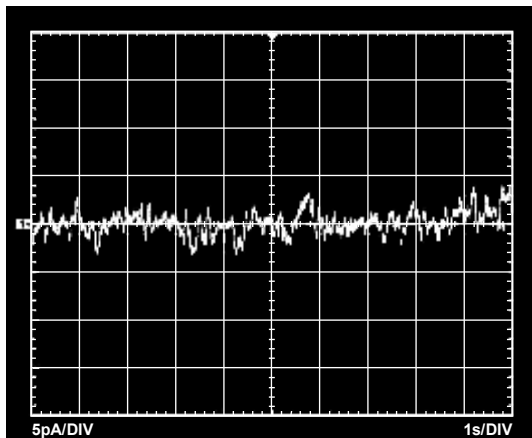


Figure 30. 0.1 Hz to 10 Hz Current Noise

13702-030

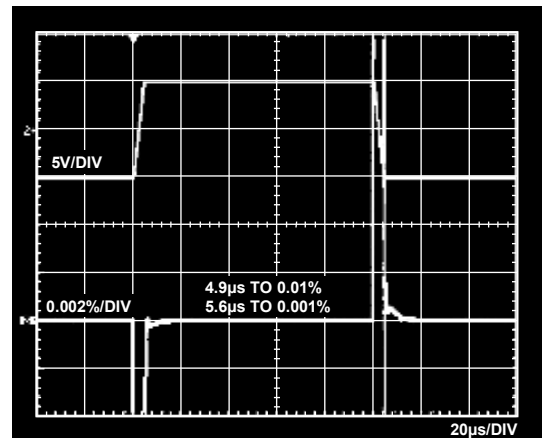
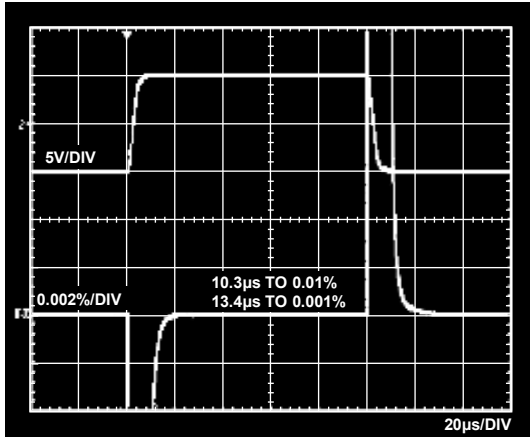


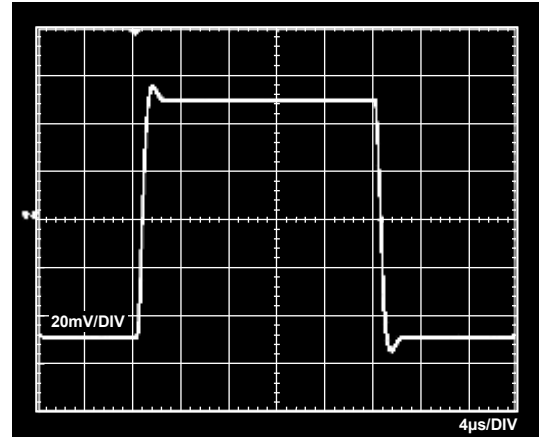
Figure 33. Large Signal Pulse Response and Settling Time ($G = 10$), 0.002%/DIV

13702-033



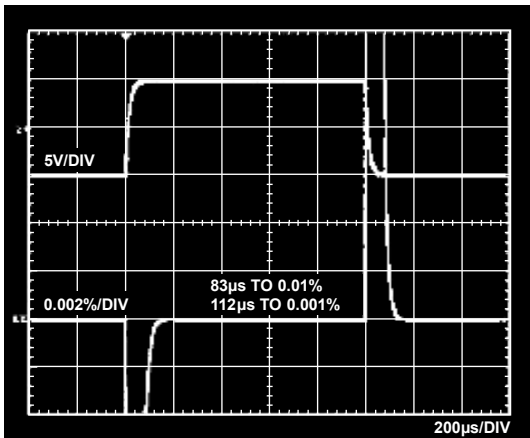
13702-004

Figure 34. Large Signal Pulse Response and Settling Time ($G = 100$), 0.002%/DIV



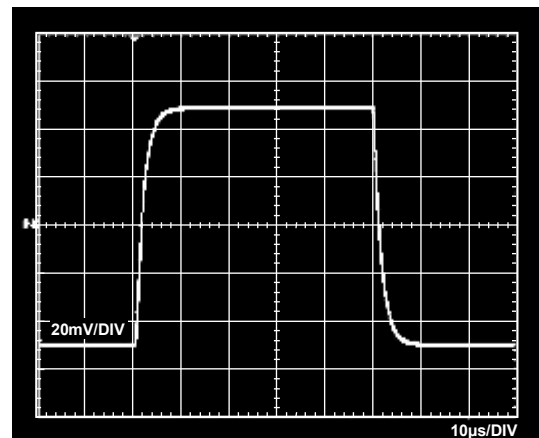
13702-007

Figure 37. Small Signal Response, $G = 10$, $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$



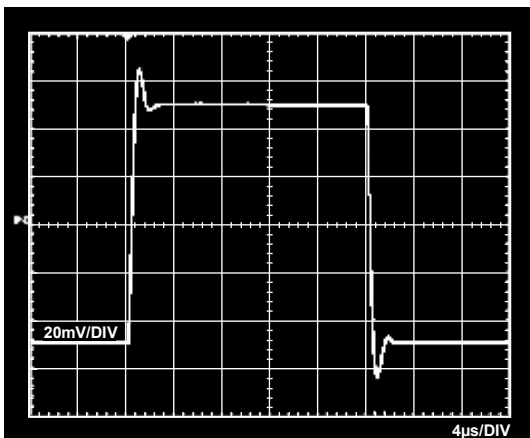
13702-035

Figure 35. Large Signal Pulse Response and Settling Time ($G = 1000$), 0.002%/DIV



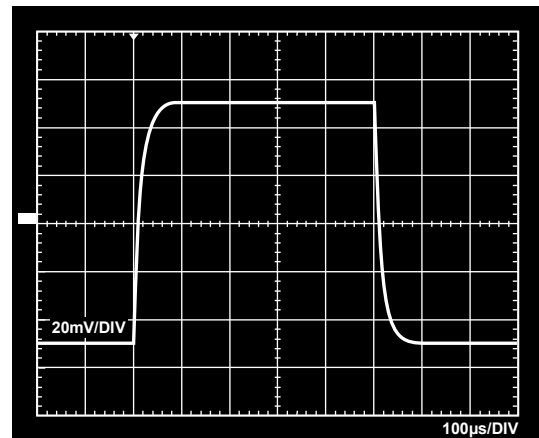
13702-038

Figure 38. Small Signal Response, $G = 100$, $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$



13702-006

Figure 36. Small Signal Response, $G = 1$, $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$



13702-039

Figure 39. Small Signal Response, $G = 1000$, $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$

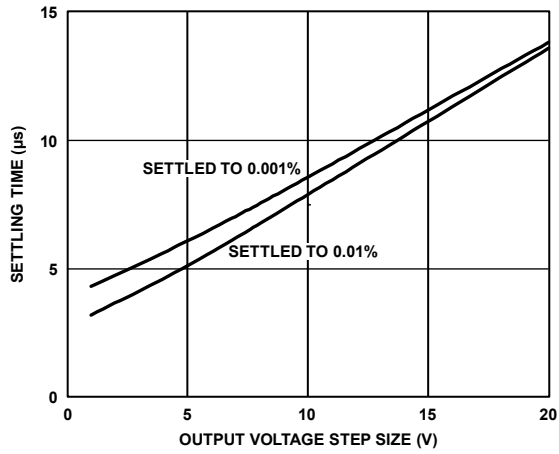


Figure 40. Settling Time vs. Output Voltage Step Size ($G = 1$)

13702-040

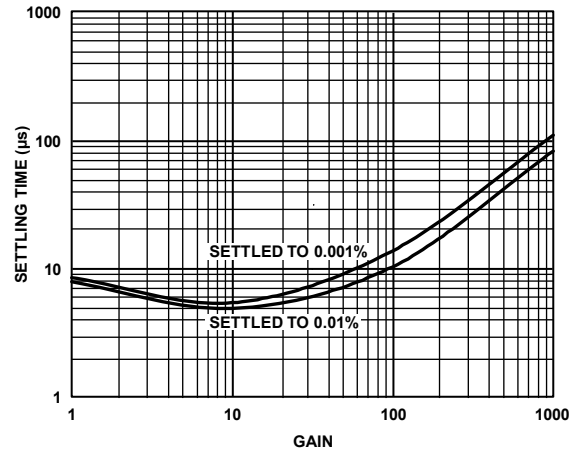
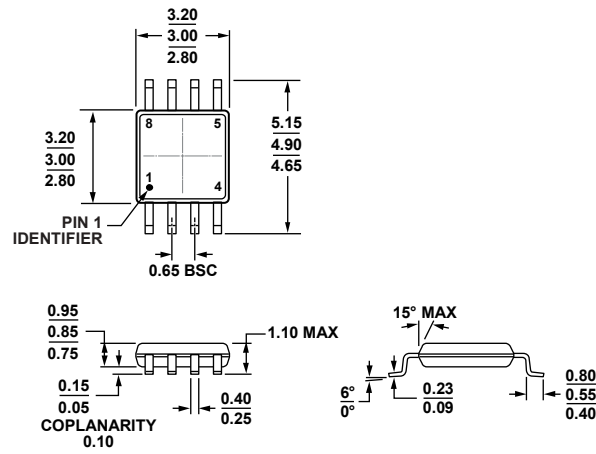


Figure 41. Settling Time vs. Gain for a 10 V Step

13702-041

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 42. 8-Lead Mini Small Outline Package [MSOP] (RM-8)

Dimensions shown in millimeters

10-07-2009 B

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option	Branding
AD8221TRMZ-EP	-55°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	Y67
AD8221TRMZ-EP-R7	-55°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	Y67

¹ Z = RoHS Compliant Part.