AS8223

FlexRay Active Star Device

1 General Description

This document is subject to change without notice.

The AS8223 is a monolithic FlexRay compliant Active Star Device that manages communication traffic among four FlexRay branches of the network, expandable to more branches through an Interstar interface.

The four branches of the AS8223 operate as a FlexRay receiver and transmitter; wherein one of the communication paths operates as a receiver while the rest operate as a transmitter.

Additionally, the AS8223 comes with a Host Controller Interface to achieve active control of the power modes and error diagnosis. An autonomous mode is entered automatically, in which the device operates without the need for a host controller. A Communication Controller interface is also built into the AS8223, to provide the standard transceiver functionality on the ECU using the AS8223.

The product is available in 44-pin MLF (9x9) package.

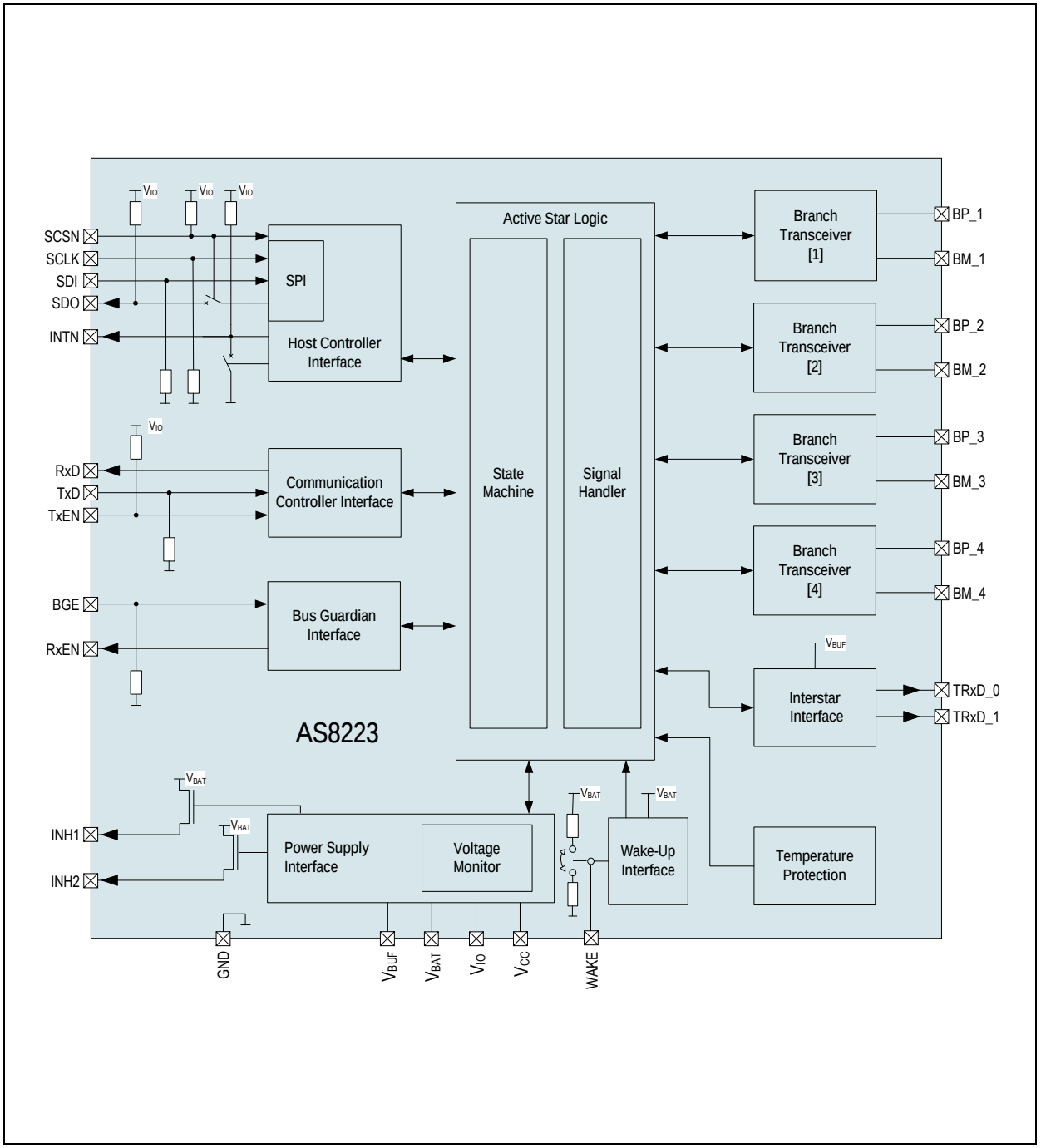
2 Key Features

- Active Star Device with four branches
- Message forwarding on six communication paths (Communication Controller Interface, four FlexRay branches, Interstar Interface)
- Data transfer up to 10Mbps
- Compliant with FlexRay Electrical Physical Layer Specification V2.1 Rev B
- Excellent EMC performance
- Low susceptibility to EMI
- Interface with optional bus guardian for bus supervision
- Automatic thermal shutdown protection
- Supports 12V and 24V systems with low sleep current
- Integrated power management system
- Two INH pins for the external voltage regulators control
- Local wake-up input
- Remote wake-up capability via FlexRay bus
- Supports Autonomous Power Mode and Host Controlled Power Mode management
- Supports 2.5V, 3V, 3.3V and 5V microcontrollers; automatically adapts to interface levels
- V_{CC} supply voltage buffer for fail-safe conditions
- Protection against damage due to short circuit conditions on the FlexRay branches (positive and negative battery voltage)
- Operating ambient temperature range -40ºC to +125ºC
- RoHs compliant
- 44-pin MLF (9x9) package

3 Applications

The AS8223 FlexRay Active Star Device is tailored for automotive gateways with embedded FlexRay Active Star functionality. Several devices can be connected to the chip's Interstar interface, thereby enabling the extension of the FlexRay branches in order to meet specific application requirements.

Figure 1. AS8223 FlexRay Active Star Device Block Diagram



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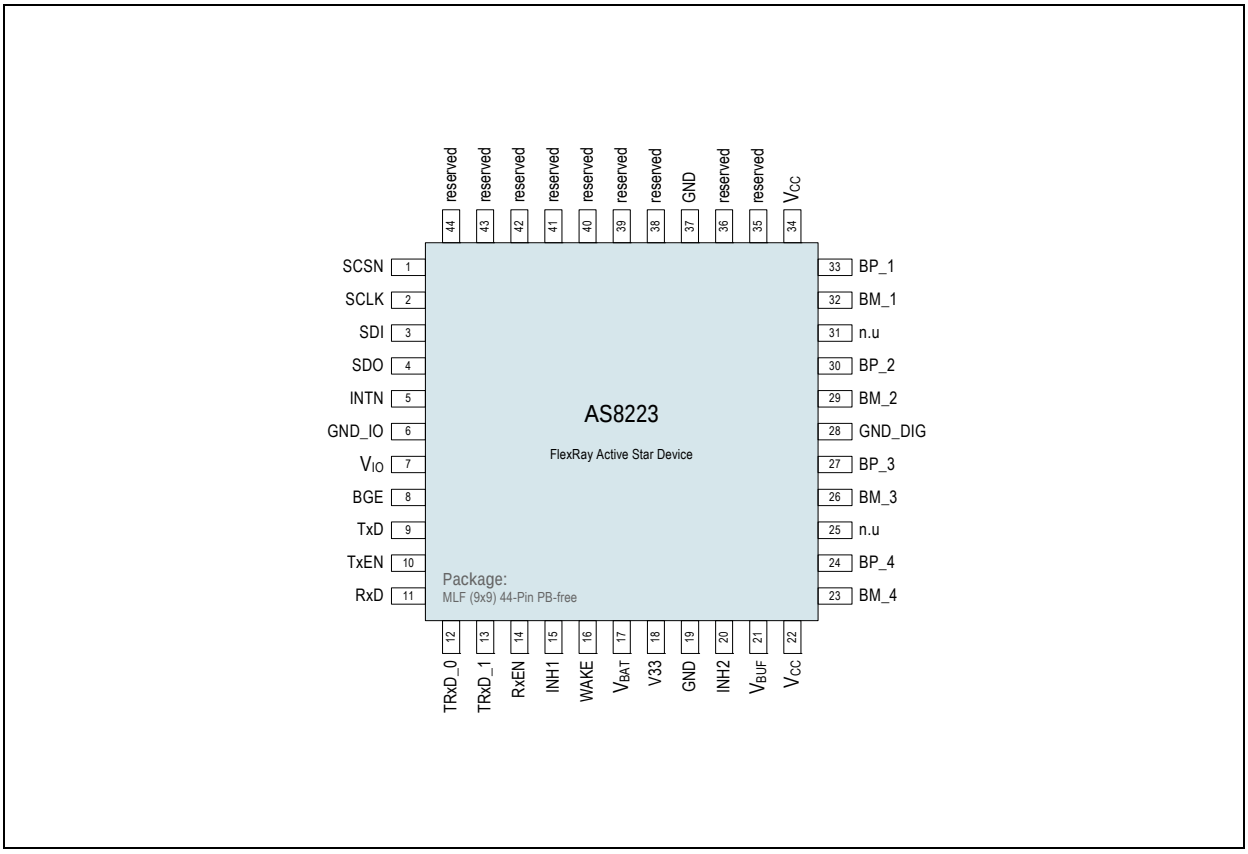
4 Pin Assignments

Figure 2. Pin Assignments (Top View)



4.1 Pin Descriptions

Table 1. Pin Descriptions

Pin Name	Pin Number	Pin Type	Description
SCSN	1	Digital input with pull-up	SPI chip select
SCLK	2	Digital input with pull-down	SPI clock
SDI	3		SPI data in
SDO	4	Digital output / tristate	SPI data out
INTN	5	Digital output open drain	Interrupt output
GNDIO	6	Supply	Ground
VIO	7		I/O supply input voltage
BGE	8	Digital input with pull-down	Bus guardian enable input
TxD	9		Transmit data input
TxEN	10	Digital input with pull-up	Transmitter enable input
RxD	11	Digital output	Receive data output
TRxD_0	12	Digital I/O	Interstar Bus line 0
TRxD_1	13		Interstar Bus line 1
RxEN	14	Digital output	Receive data enable output

Table 1. Pin Descriptions

Pin Name	Pin Number	Pin Type	Description
INH1	15	Analog I/O	Inhibit output for switching external voltage regulator
WAKE	16		Local Wake input
V_{BAT}	17	Supply	Battery supply input voltage
V33	18	Analog I/O	Internal voltage stabilizing output
GND	19	Supply	Ground
INH2	20	Analog I/O	Inhibit output for switching external voltage regulator
V_{BUF}	21		TRxD_0, TRxD_1 stabilizing output
V_{CC}	22	Supply	Supply input voltage
BM_4	23	Analog I/O	Bus line minus branch 4
BP_4	24		Bus line plus branch 4
n.u	25	-	Not used
BM_3	26	Analog I/O	Bus line minus branch 3
BP_3	27		Bus line plus branch 3
GNDD	28	Supply	Digital ground
BM_2	29	Analog I/O	Bus line minus branch 2
BP_2	30		Bus line plus branch 2
n.u	31	-	Not used
BM_1	32	Analog I/O	Bus line minus branch 1
BP_1	33		Bus line plus branch 1
V_{CC}	34	Supply	Supply voltage
Reserved	35	-	To be connected to GND
Reserved	36	-	To be connected to GND
GND	37	Supply	Ground
Reserved	38	-	To be left unconnected
Reserved	39	-	To be left unconnected
Reserved	40	-	To be connected to GND or to be left unconnected
Reserved	41	-	To be connected to GND or to be left unconnected
Reserved	42	-	To be connected to GND or to be left unconnected
Reserved	43	-	To be connected to GND or to be left unconnected
Reserved	44	-	To be connected to GND or to be left unconnected

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 9 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: All voltages are referred to pin GND.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Note
Electrical Parameters					
V_{BAT}	Battery Supply Voltage	-0.3	+40	V	
V_{CC}	Supply Voltage	-0.3	+7.0	V	
V_{IO}		-0.3	+7.0	V	$V_{IO} < V_{CC}$
V_{BUF}	Stabilizing voltage output	-0.3	+5.0	V	
V33					
	DC Voltage at INTN, TxD, RxD, TxEN, BGE, RxEN, SCSN, SCLK, SDI, SDO	-0.3	V_{IO} + 0.3	V	
V_{TRxD0}, V_{TRxD1}	DC Voltage at Interstar interface	-0.3	V_{BUF} + 0.3	V	
	DC Voltage on pin WAKE, INH1, INH2	-0.3	V_{BAT} + 0.3	V	
	DC voltage at GNDIO, GNDD	-0.3	+0.3	V	
	DC Voltage at BP_{1-4} and BM_{1-4}	-40	+40	V	
	Input current (latchup immunity)	-100	100	mA	According to AEC-Q100-004
Electrostatic Discharge					
ESD	Electrostatic discharge at bus lines V_{BAT}, WAKE	-4	+4	kV	According to AEC-Q100-002 (HBM)
	Electrostatic discharge at bus lines BP_{1-4}, BM_{1-4}	-6	+6	kV	According to AEC-Q100-002 (HBM)
	Electrostatic discharge at bus lines BP_{1-4}, BM_{1-4}, V_{BAT}, WAKE	-6	+6	kV	According to FlexRay Physical Layer EMC Measurement Specification Version 3.0
	Electrostatic discharge on all pins	-2	+2	kV	According to AEC-Q100-002 (HBM)
		-500	+500	V	According to AEC-Q100-011 (Charge Device Model)
		-100	+100	V	According to AEC-Q100-003 (Machine Model)
Damage Tests					
U_s	Transient voltage on V_{BAT}, BM and BP pins	-100		V	ISO7637-2 test pulse 1; class D (see Figure 14)
			+75	V	ISO7637-2 test pulses 2a; class D (see Figure 14)
		-150		V	ISO7637-2 test pulses 3a; class D (see Figure 14)
			+100	V	ISO7637-2 test pulses 3b; class D (see Figure 14)

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Note
Power Dissipation					
P_t	Total power dissipation (all supplies and outputs)		1	W	
Temperature Ranges and Storage Conditions					
T_{strg}	Storage temperature	-55	+150	ºC	
T_J	Junction temperature	-40	+150	ºC	
T_{BODY}	Package body temperature		+260	ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).
	Humidity non-condensing	5	85	%	
Φja	Package thermal resistance		25	ºC/W	
MSL	Moisture Sensitivity Level	3			Represents a maximum floor life time of 168h

6 Electrical Characteristics

In this specification, all the defined tolerances for external components are assured over the whole operation conditions range as well as over lifetime.

T_J=-40°C to +150°C, V_{CC}=+4.75V to +5.25V, V_{BAT}=5.5V to +40V, V_{IO}=+2.2 to V_{CC}, R_L=45Ω, C_L= 100pF, C_{RxD}= 15pF, C_{VBUF}=1µF, C_{V33}=1µF unless otherwise specified.

6.1 Supply Voltage

Table 3. Supply Voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{AMB}	Ambient temperature		-40		+125	°C
V_{CC}-V_{IO}	Difference of supplies		-0.1		+3.05	V
I_{BAT}	V_{BAT} current consumption	V_{BAT}=12V; AS_SLEEP and AS_STANDBY mode; T_J<125°C (see footnote 1)	0		150	µA
		V_{BAT}=12V; AS_SLEEP and AS_STANDBY; T_J<150°C (see footnote 1)	0		150	µA
		V_{BAT}=12V; AS_SLEEP and AS_ STANDBY mode; T_J<125°C, one remote wake-up branch active. (see footnote 1)	0		100	µA
		AS_NORMAL mode	0		1	mA
I_{CC}	V_{CC} current consumption	AS_SLEEP and AS_STANDBY mode; V_{CC} = 0V to +5.25V (see footnote 1)	-5		50	µA
		AS_NORMAL, all driver enabled	0		200	mA
		AS_NORMAL, all driver enabled; R_{BUS}=∞ Ω	0		50	mA
I_{IO}	V_{IO} current consumption	AS_SLEEP and AS_STANDBY mode; V_{IO} = 0V to +5.25V (see footnote 1)	-9		+9	µA
		AS_NORMAL mode	0		1	mA
V_{33}	V33 voltage	AS_NORMAL mode; I_{33}=10mA	3		3.6	V
		AS_SLEEP and AS_STANDBY mode; I_{33}=1mA	2.5		3.6	V
V_{BUF}	V_{BUF} voltage		1.2		1.3	V

1. SCSN, SCLK, SDI, SDO, INTN, TxD, RxD, TxEN, BGE, RxEN, WAKE, INH1, INH2, TRxD_0, TRxD_1, Pin 36, Pin 38, Pin 39, Pin 35: Unconnected.

6.2 State Transitions Active Star

Table 4. State Transitions Active Star

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{AS\_LP\_INHx\_H}$	Delay time Host Command to INHx = “high” from AS_SLEEP and AS_STANDBY mode	INHx “high” = 80% V_{BAT}			50	µs
$t_{AS\_Normal\_INHx\_L}$	Delay time Host Command to INHx = “low” from AS_NORMAL mode	INHx “low” = 20% V_{BAT}, 10kΩ external pull-down			10	µs
$t_{AS\_Standby\_INHx\_L}$	Delay time Host Command to INH1 = “low” from AS_STANDBY mode	INH1 “low” = 20% V_{BAT} 10kΩ external pull-down			50	µs
$t_{AS\_LP\_INHx\_H}$	Delay time wake-up event to INHx = “high” from AS_SLEEP and AS_STANDBY mode	INHx “high” = 80% V_{BAT}			50	µs
$t_{AS\_LP\_RxD\_H}$	Delay time wake-up event to RxD = “high” from AS_SLEEP and AS_STANDBY mode	Wake-up flag set			100	µs
$t_{AS\_LP\_RxEN\_H}$	Delay time wake-up event to RxEN = “high” from AS_SLEEP and AS_STANDBY mode	Wake-up flag set			100	µs
$t_{ASSLEEP}$	Go-to-sleep timeout (APM mode)	INH1 low = 20% V_{BAT} 10kΩ external pull-down	640		6400	ms

6.3 Branch to Branch Timing

Table 5. Branch to Branch Timing

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{BUSxy\_TSS\_length\_change}$	Frame TSS length change from BUSx to BUSy				450	ns
$t_{BUSxy\_FES1\_length\_change}$	Prolongation of last bit of a frame from BUSx to BUSy				450	ns
$t_{BUSxy\_symbol\_length\_change}$	Symbol length change		-300		450	ns
$t_{BUSxy01}$	Delay time from BUSx to BUSy positive edge				150	ns
$t_{BUSxy10}$	Delay time from BUSx to BUSy negative edge				150	ns
$t_{BUSxy\_asymmetry}$	Delay time from BUSx to BUSy data asymmetry	$t_{BUSxy01} - t_{BUSxy10}$	-8		8	ns

6.4 Communication Controller to Branch Timing

Table 6. Communication Controller to Branch Timing

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{TxD_BUS01}	Delay time from TxD to BUS positive edge	t_{TxD01} = 5ns			50	ns
t_{TxD_BUS10}	Delay time from TxD to BUS negative edge	t_{TxD10} = 5ns			50	ns
$t_{TxD\_BUS\_asymmetry}$	Delay time from TxD to BUS asymmetry	$t_{TxD\_BUS10} - t_{TxD\_BUS01}$	-4		4	ns
$t_{TxEN\_BUS\_IdleActive}$	Delay time from TxEN to BUS active				250	ns
$t_{TxEN\_BUS\_ActiveIdle}$	Delay time from TxEN to BUS idle				250	ns
$t_{TxEN\_BUS\_asymmetry}$	Delay time from TxEN to BUS active-idle asymmetry	$t_{TxEN\_BUS\_IdleActive} - t_{TxEN\_BUS\_ActiveIdle}$	-50		50	ns
$t_{BGE\_BUS\_IdleActive}$	Delay time from BGE to BUS active				250	ns
$t_{BGE\_BUS\_ActiveIdle}$	Delay time from BGE to BUS idle				250	ns

6.5 Branch to Communication Controller Timing

Table 7. Branch to Communication Controller Timing

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{BUS_RxD10}	Delay from BUS to RxD negative edge				80	ns
t_{BUS_RxD01}	Delay from BUS to RxD positive edge				80	ns
t_{bit}	Bit time		54			ns
$t_{BUS\_RxD\_asymmetry}$	Delay time from BUS to RxD asymmetry	$t_{BUS\_RxD10} - t_{BUS\_RxD01}$	-5		5	ns
t_{BUS_RxEN01}	Delay time from BUS idle to RxEN positive edge		50		400	ns
t_{BUS_RxEN10}	Delay time from BUS active to RxEN negative edge		100		450	ns

6.6 Interstar to Branch Timing

Table 8. Interstar to Branch Timing

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{IS01_BUS01}	Delay time from ISI to BUS positive edge	t_{IS01} = 5ns			70	ns
t_{IS01_BUS10}	Delay time from ISI to BUS negative edge	t_{IS10} = 5ns			70	ns
$t_{IS\_BUS\_asymmetry}$	Delay time from ISI to BUS asymmetry	$t_{IS10\_BUS10} - t_{IS01\_BUS01}$	-5		5	ns
$t_{IS\_BUS\_IdleActive}$	Delay time from ISI to BUS active				200	ns
$t_{IS\_BUS\_ActiveIdle}$	Delay time from ISI to BUS idle				200	ns

6.7 Branch to Interstar Timing

Table 9. Branch to Interstar Timing

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{BUS\_IS\_ActiveIdle}$	Delay time from BUS idle to ISI idle		50		400	ns
$t_{BUS\_IS\_IdleActive}$	Delay time from BUS active to ISI active		100		450	ns
t_{BUS_IS10}	Delay from BUS to ISI negative edge				100	ns
t_{BUS_IS01}	Delay from BUS to ISI positive edge				100	ns
t_{bit}	Bit time		54			ns
$t_{BUS\_IS\_asymmetry}$	Delay time from BUS to ISI asymmetry	$t_{BUS\_IS10} - t_{BUS\_IS01}$	-5		5	ns

6.8 Communication Controller to Interstar Timing

Table 10. Communication Controller to Interstar Timing

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{TxD01_IS01}	Delay time from TxD to ISI positive edge	t_{TxD01} = 5ns			50	ns
t_{TxD10_IS10}	Delay time from TxD to ISI negative edge	t_{TxD01} = 5ns			50	ns
$t_{TxD\_IS\_asymmetry}$	Delay time from TxD to ISI asymmetry	$t_{TxD01\_IS01} - t_{TxD10\_IS10}$	-4		4	ns
$t_{TxEN\_IS\_IdleActive}$	Delay time from TxEN to ISI active				150	ns
$t_{TxEN\_IS\_ActiveIdle}$	Delay time from TxEN to ISI idle				150	ns
$t_{BGE\_IS\_IdleActive}$	Delay time from BGE to ISI active				150	ns
$t_{BGE\_IS\_ActiveIdle}$	Delay time from BGE to ISI idle				150	ns

6.9 Interstar to Communication Controller Timing

Table 11. Interstar to Communication Controller Timing

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{IS01_RxD01}	Delay time from ISI to RxD positive edge	t_{IS01} = 5ns			50	ns
t_{IS01_RxD10}	Delay time from ISI to RxD negative edge	t_{IS10} = 5ns			50	ns
$t_{IS\_RxD\_asymmetry}$	Delay time from ISI to RxD asymmetry	$t_{IS10\_RxD10} - t_{IS01\_RxD01}$	-5		5	ns
$t_{IS\_RxEN\_01}$	Delay time from ISI to RxEN positive edge				150	ns
$t_{IS\_RxEN\_10}$	Delay time from ISI to RxEN negative edge				150	ns

6.10 Active Star General Timing

Table 12. Active Star General Timing

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{STAR_COL}	Active Star collision filter time	Guaranteed by design			50	ns
t_{exit_fail}	Idle detection time to exit branch fail silent	Programmable via SPI command		1.1	10	µs
t_{ears_shut}	Blanking time between two frames			1		µs
$t_{BranchNoiseTimeout}$	Branch noise timeout		1.5		10	ms
$t_{CCNoiseTimeout}$	Communication Controller noise timeout		1.5		10	ms
$t_{EarsShut\_Fault}$	Blanking time between two frames for faulty branches			5		µs
$t_{TxEN\_RxD\_ActiveIdle}$	Delay time from TxEN rising edge to RxD rising edge; change of bus active to bus idle (loopback)				250	ns

6.11 Transmitter

The following parameters are applicable to all the branch transmitters.

Table 13. Transmitter

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{BUS\_DIFF\_D0}$	Differential bus voltage low in BRANCH_ACTIVE mode (Data_0)	$V_{BPdata0} - V_{BMdata0}$; $40\Omega < R_L < 55\Omega$	-2		-0.6	V
$V_{BUS\_DIFF\_D1}$	Differential bus voltage high in BRANCH_ACTIVE mode (Data_1)	$V_{BPdata1} - V_{BMdata1}$; $40\Omega < R_L < 55\Omega$	0.6		2	V
ΔV_{BUS_DIFF}	Matching between Data_0 and Data_1 differential bus voltage in BRANCH_ACTIVE mode	$V_{BUS\_DIFF\_D0} - V_{BUS\_DIFF\_D1}$ $40\Omega < R_L < 55\Omega$	-200		200	mV
$V_{BUS\_COM\_D0}$	Common mode bus voltage in case of Data_0 in Branch non-low-power mode	$V_{BPdata0}/2+V_{BMdata0}/2$ $40\Omega < R_L < 55\Omega$	0.4 * Vcc		0.6 * Vcc	V
$V_{BUS\_COM\_D1}$	Common mode bus voltage in case of Data_1 in Branch non-low-power mode	$V_{BPdata1}/2+V_{BMdata1}/2$ $40\Omega < R_L < 55\Omega$	0.4 * Vcc		0.6 * Vcc	V
ΔV_{BUS_COM}	Matching between Data_0 and Data_1 common mode voltage	$V_{BUS\_COM\_D0} - V_{BUS\_COM\_D1}$ $40\Omega < R_L < 55\Omega$	-200		200	mV
$V_{BUS\_DIFF\_Idle}$	Absolute differential bus voltage in bus idle mode				30	mV
$IBP_{BMShortMax}$ $IBM_{BPShortMax}$	Absolute maximum current if BP shorted to BM	$V_{BP} = V_{BM}$			+100	mA
$IBP_{GNDShortMax}$	Absolute maximum current if BP is shorted to GND	$V_{BP} = 0V$			+100	mA
$IBM_{GNDShortMax}$	Absolute maximum current if BM is shorted to GND	$V_{BM} = 0V$			+100	mA
$IBP_{-5VShortMax}$	Absolute maximum current if BP is shorted to -5V	$V_{BP} = -5V$			+100	mA
$IBM_{-5VShortMax}$	Absolute maximum current if BM is shorted to -5V	$V_{BM} = -5V$			+100	mA
$IBP_{27VShortMax}$	Absolute maximum current if BP is shorted to 27V	$V_{BP} = 27V$			+100	mA

Table 13. Transmitter

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$IBM_{27VShortMax}$	Absolute maximum current if BM is shorted to 27V	V_{BM} = 27V			+100	mA
$IBP_{40VShortMax}$	Absolute maximum current if BP is shorted to 40V	V_{BP} = 40V			+100	mA
$IBM_{40VShortMax}$	Absolute maximum current if BM is shorted to 40V	V_{BM} = 40V			+100	mA
t_{BUS_TX10}	Fall time differential bus voltage	80% – 20% of V_{BUS}	3.75		18.75	ns
t_{BUS_TX01}	Rise time differential bus voltage	20% – 80% of V_{BUS}	3.75		18.75	ns
$t_{BUS\_IdleActive}$	Differential bus voltage transition time: idle to active				30	ns
$t_{BUS\_ActiveIdle}$	Differential bus voltage transition time: active to idle				30	ns

6.12 Receiver

The following parameters are applicable to all the branch receivers.

Table 14. Receiver

Symbol	Parameter	Conditions	Min	Typ	Max	Units
R_{BP}, R_{BM}	BP, BM input resistance	Idle mode; R_{BUS}=∞	10		40	KΩ
R_{DIFF}	BP, BM differential input resistance	Idle mode; R_{BUS}=∞	20		80	KΩ
V_{CM}	Common mode voltage at receiver	2 x (| V_{Data0} | - | V_{Data1} ||) / (| V_{Data0} | + | V_{Data1} |) x 100%, Test with (V_{BP} + V_{BM})/2 = V_{CM} = 2.5V	-10		+15	V
V_{BPidle}, V_{BMidle}	Idle voltage in Branch non-low-power modes on pin BP, BM	Branch non-low-power mode; V_{TxEN} = V_{IO} 40Ω || 100pF	0.4 * V_{CC}	0.5 * V_{CC}	0.6 * V_{CC}	V
V_{BPidle_low}, V_{BMidle_low}	Idle voltage in Branch low-power modes on pin BP, BM	Branch low-power modes 40Ω || 100pF	-0.2	0	+0.2	V
I_{BPidle}	Absolute idle output current on pin BP	-40V < V_{BP} < 40V	0		7.5	mA
I_{BMidle}	Absolute idle output current on pin BM	-40 V < V_{BM} < 40V	0		7.5	mA
I_{BPleak}, I_{BMleak}	Absolute leakage current, when not powered	V_{BP}=V_{BM}=5V, V_{CC}=0V, V_{BAT}=0V; V_{IO}=0V	0		20	µA
$V_{BUSActiveHigh}$	Activity detection differential input voltage high	Branch non-low-power modes -10V < (V_{BP}, V_{BM}) < 15V	150	225	400	mV
$V_{BUSActiveLow}$	Activity detection differential input voltage low	Branch non-low-power modes -10V < (V_{BP}, V_{BM}) < 15V	-400	-225	-150	mV
V_{Data1}	Data1 detection differential input voltage	*Pre-condition:* Activity already detected. Branch non-low-power modes. -10V < (V_{BP}, V_{BM}) < 15V	150	225	300	mV
V_{Data0}	Data0 detection differential input voltage	*Pre-condition:* Activity already detected. Branch non-low-power modes. -10V < (V_{BP}, V_{BM}) < 15V	-300	-225	-150	mV
$V_{DataErr}$	Mismatch between Data0 and Data1 differential input voltage	2 x (| V_{Data0}| - | V_{Data1} ||) / (| V_{Data0} | + | V_{Data1} |) [2]			10	%
t_{bit}	Receiving bit time	C_{RxD}=15pF	54	100		ns

Table 14. Receiver

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{ActivityDetection}$	Activity detection time		100		300	ns
$t_{IdleDetection}$	Idle detection time		50		250	ns

6.13 Bus Wake-up Detector

The following parameters are applicable to all the branch wake-up detectors.

Table 15. Bus Wake-up Detector

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{BAT_WU}	V_{BAT} supply to detect wake-up		7			V
t_{BWU0}	Data_0 detection time in remote wake-up pattern	-10V<(V_{BP}, V_{BM})<15V; V_{BAT}>7V	1		4	µs
$t_{BWUIdle}$	Idle or Data_1 detection time in remote wake-up pattern	-10V<(V_{BP}, V_{BM})<15V; V_{BAT}>7V	1		4	µs
$t_{BWUDetect}$	Total remote wake-up detection time	-10V<(V_{BP}, V_{BM})<15V; V_{BAT}>7V	48		140	us
V_{BWUTH}	Wake-up detector threshold	-10V<(V_{BP}, V_{BM})<15V; V_{BAT}>7V	-300		-150	mV

6.14 Local Wake-up Detector

Table 16. Local Wake-up Detector

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LWUL}	Low level input current on WAKE pin	V_{BAT}=12V; V_{WAKE}=2V for t<$t_{LWUFilter}$; V_{BAT}>7V	-20		-5	µA
I_{LWUH}	High level input current on WAKE pin	V_{BAT}=12V; V_{WAKE}=4V for t<$t_{LWUFilter}$; V_{BAT}>7V	5		20	µA
$t_{LWUFilter}$	Local wake filter time	V_{BAT}>7V	1		40	µs
V_{LWUTH}	Local Wake-up detection threshold voltage		2		4	V

6.15 Supply Voltage Monitor

Table 17. Supply Voltage Monitor

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{BAT_{THH}}$	V_{BAT} undervoltage recovery threshold		3.5		4.5	V
$V_{BAT_{THL}}$	V_{BAT} undervoltage detection threshold		3		4	V
$V_{CC_{THH}}$	V_{CC} undervoltage recovery threshold		3.5		4.5	V
$V_{CC_{THL}}$	V_{CC} undervoltage detection threshold		3		4	V
$V_{IO_{THH}}$	V_{IO} undervoltage recovery threshold		1.25		2.0	V
$V_{IO_{THL}}$	V_{IO} undervoltage detection threshold		0.75		1.5	V
$t_{UV\_REACTION}$	Undervoltage reaction time for V_{CC}		30		700	µs
$t_{UV\_DETECTION}$	Undervoltage detection time for V_{BAT}, V_{CC}, V_{IO}		100		700	ms
$t_{UV\_RECOVERY}$	Undervoltage recovery detection time for V_{BAT}, V_{CC}, V_{IO}		0.7		5	ms
$t_{UV\_DEBOUNCING}$	Undervoltage debouncing time for V_{BAT}, V_{CC}, V_{IO}		8		64	µs

6.16 Bus Error Detection

The following parameters are applicable to all the branch error detectors.

Table 18. Bus Error Detection

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{THL}	Absolute bus current for low current detection	BRANCH_ACTIVE mode, Transmitter enabled		5		mA
I_{THH}	Absolute bus current for high current detection	BRANCH_ACTIVE mode, Transmitter enabled		40		mA
V_{SHORT}	Differential voltage on BP and BM for detecting short circuit between bus lines	BRANCH_ACTIVE mode, Transmitter enabled		225		mV
t_{BUS_ERROR}	Bus error detection time	BRANCH_ACTIVE mode, Transmitter enabled			500	ns

6.17 Over Temperature

Table 19. Over Temperature

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OT_{TH}	Over temperature threshold		150		180	°C
OT_{TL}	Over temperature hysteresis		10		20	°C

6.18 Power Supply Interface

Table 20. Power Supply Interface

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ΔV_{OINH}	High level voltage drop on INH1, INH2	I_{INH}=0.2mA; V_{BAT}=5.5V	0		0.8	V
$\lvert I_{IL} \rvert$	Leakage current	Sleep mode, V_{INH}=0V			5	µA

6.19 Communication Controller Interface

Table 21. Communication Controller Interface

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{TxDIH}	Threshold for detecting TxD as on logical high				0.7 * V_{IO}	V
V_{TxDIL}	Threshold for detecting TxD as on logical low		0.3 * V_{IO}			V
I_{TxDIH}	TxD high level input current		30		100	µA
I_{TxDIL}	TxD low level input current		-5		5	µA
V_{TxENIH}	Threshold for detecting TxEN as on logical high				0.7 * V_{IO}	V
V_{TxENIL}	Threshold for detecting TxEN as on logical low		0.3 * V_{IO}			V
I_{TxENIH}	TxEN high level input current		-5		5	µA
I_{TxENIL}	TxEN low level input current		-100		-30	µA
V_{RxDOH}	RxD high level output voltage	I_{RxD}=-4mA, V_{IO}=5V	0.8 * V_{IO}		1.0 * V_{IO}	V
V_{RxDOL}	RxD low level output voltage	I_{RxD}=4mA, V_{IO}=5V	0		0.2 * V_{IO}	V
$t_{RxDfall}$	Fall time RxD voltage	80% – 20% of V_{RxDL}; C_{RxD}=15pF			5	ns
$t_{RxDrise}$	Rise time RxD voltage	20% – 80% of V_{RxDL}; C_{RxD}=15pF			5	ns
$t_{RxD\_mismatch}$	Mismatch of rise and fall time of RxD	$\lvert t_{RxDrise} \rvert$ - $\lvert t_{RxDfall} \rvert$	-2		+2	ns

6.20 Host Controller Interface

Table 22. Host Controller Interface

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{SDI_IH}	Threshold for detecting SDI as on logical high				0.7 * VIO	V
V_{SDI_IL}	Threshold for detecting SDI as on logical low		0.3 * VIO			V
I_{SDI_IH}	SDI high level input current		30		100	µA
I_{SDI_IL}	SDI low level input current		-5		5	µA
V_{SDO_OH}	SDO high level output voltage	I_{SDO}=-4mA, VIO=5V	0.8 * VIO		1.0 * VIO	V
V_{SDO_OL}	SDO low level output voltage	I_{SDO}=4mA, VIO=5V	0		0.2 * VIO	V
V_{SCLK_IH}	Threshold for detecting SCLK as on logical high				0.7 * VIO	V
V_{SCLK_IL}	Threshold for detecting SCLK as on logical low		0.3 * VIO			V
I_{SCLK_IH}	SCLK high level input current		30		100	µA
I_{SCLK_IL}	SCLK low level input current		-5		5	µA
V_{SCSN_IH}	Threshold for detecting SCSN as on logical high				0.7 * VIO	V
V_{SCSN_IL}	Threshold for detecting SCSN as on logical low		0.3 * VIO			V
I_{SCSN_IH}	SCSN high level input current		30		100	µA
I_{SCSN_IL}	SCSN low level input current		-5		5	µA
V_{INTN_OH}	INTN high level output voltage	I_{NTN}=-4mA, VIO=5V	0.8 * VIO		1.0 * VIO	V
V_{INTN_OL}	INTN low level output voltage	I_{INTN}=4mA, VIO=5V	0		0.2 * VIO	V
BR_{SPI}	Bit rate		10 kbps		1 Mbps	
t_{SCLK_High}	Clock high time		500			ns
t_{SCLK_High}	Clock low time		500			ns
t_{DI_Setup}	Data in setup time		20			ns
t_{DI_Setup}	Data in hold time		10			ns
t_{SCSN_Hold}	SCSN in hold time		100			ns
t_{DO_Delay}	Data out delay				150	ns
t_{DOS}	Data out setup time		130			ns
t_{DOH}	Data out hold time		130			ns
t_{DO_HZ}	Data out to high impedance delay	Time for the SPI to release the SDO bus with respect to CS rising edge			150	ns
t_{CP_Setup}	Clock setup time	Setup time of SCLK with respect to CS falling edge	100			ns
t_{CP_Hold}	Clock hold time	Hold time of SCLK with respect to CS falling edge	100			ns
I_{SDO_PU}	SDO pull-up current		30		100	µA
I_{INTN_PU}	INTN pull-up current		30		100	µA

6.21 Bus Guardian Interface

Table 23. Bus Guardian Interface

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{BGEIH}	Threshold for detecting BGE as on logical high				0.7 * V_{IO}	V
V_{BGEIL}	Threshold for detecting BGE as on logical low		0.3 * V_{IO}			V
I_{BGEIH}	BGE high level input current		30		100	µA
I_{BGEIL}	BGE low level input current		-5		5	µA
V_{RxENOH}	RxEN high level output voltage	I_{RxEN}=-4mA, V_{IO}=5V	0.8 * V_{IO}		1.0 * V_{IO}	V
V_{RxENOL}	RxEN low level output voltage	I_{RxEN}=4mA, V_{IO}=5V	0		0.2 * V_{IO}	V

6.22 Interstar Interface

Table 24. Interstar Interface

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{TRxDOH}	TRxD high level output voltage		1	1.25	1.5	V
V_{TRxDOL}	TRxD low level output voltage		0	0	0.3	V
V_{TRxD_IH}	Threshold for detecting TRxD as logical high				0.7 * V_{BUF}	V
V_{TRxD_IL}	Threshold for detecting TRxD as logical low		0.3 * V_{BUF}			V
R_{TRxD_PU}	TRxD Internal pull-up resistance		60	100	180	KΩ
t_{TRxD01}	TRxD rise time	20% – 80% of V_{BUF}; C_{TRxD}=60pF		5		ns
t_{TRxD10}	TRxD fall time	80% – 20% of V_{BUF}; C_{TRxD}=60pF		5		ns
$t_{ISActiveDetection}$	Activity detection time			10		ns
$t_{ISIdleDetection}$	Idle detection time			10		ns
$t_{ISCollision}$	Collision detection time			10		ns

7 Detailed Description

The AS8223 FlexRay Active Star Device consists of six communication paths. During normal operation one of the communication paths is switched as receiver and the other paths as transmitter. Each of the four Branch Transceivers can be connected to different FlexRay bus lines to provide bi-directional communication of the extended FlexRay network.

Every message stream received at one communication path is converted into a digital signal and then forwarded to the transmitting communication paths.

The device supports different low power states which can be controlled by the host controller. Every Branch Transceiver supports several states for controlling the communication on the respective path.

7.1 Routing Functionality of the Active Star

7.1.1 Branch Transceivers

The basic function of the Branch Transceiver (BT) is to convert the FlexRay bus signal into a digital signal and vice-versa according to the FlexRay Specification. Each BT includes a transmitter, a receiver, a wake-up detector and a failure detector. The receiver of each branch transceiver has got a digital interface to the central logic consisting of an RxD and a RxEN signal. Activity is detected on the FlexRay bus when the differential voltage between the lines BP and BM is lower than $V_{BUSActiveLow}$ or higher than $V_{BUSActiveHigh}$ for a time longer than $t_{ActivityDetection}$. Idle is detected on the bus when the differential signal between BP and BM is higher than $V_{BUSActiveLow}$ or lower than $V_{BUSActiveHigh}$ for a time longer than $t_{IdleDetection}$. The RxEN signal of the corresponding BT is active low and it gets active when activity on the FlexRay bus is detected. The RxEN signal of the corresponding BT is at logic high when Idle is detected on the bus (Idle, Idle_LP, Idle_HZ). The RxD signal is the translated frame from the incoming FlexRay signal to be received by the Active Star. RxD is logical low when the differential signal between BP and BM is lower than V_{Data0}. RxD is logical high when the differential signal is higher than V_{Data1}. The transmitter of the branch transceiver has got a digital interface to the central logic consisting of a TxD and a TxEN signal. The TxEN signal is an active low signal used by the Active Star Device to activate the transmitter. The TxD signal is the frame signal coming from the Active Star Device to be transmitted by the BT into the FlexRay bus. If the TxEN signal is driven low, the transmitter outputs $V_{BUSx\_DIFF\_D0}$ in case TxD is in logical low, and outputs $V_{BUSx\_DIFF\_D1}$ in case TxD signal is in logical high. The transmitter signals $V_{BUS\_DIFF\_Idle}$ in case TxEN is high.

7.1.2 Communication Controller Interface

The AS8223 has a Communication Controller Interface (CC) to connect a FlexRay Communication Controller directly with the central logic of the Active Star Device (ASD). The CC interface includes one receive data signal RxD, one transmit data signal TxD and one transmit enable signal TxEN. When sending a data stream, the central logic outputs the digital frame at the RxD signal of the CC interface. The ASD detects idle at the CC when the voltage level at the TxEN pin is higher than V_{TxENIH}. The ASD detects activity at the CC when the voltage level at the TxEN pin is lower than V_{TxENIL}. The TxD signal is the frame signal coming from the CC to be transmitted to the central logic. When the TxEN signal is driven low, the central logic receives Data0 when TxD voltage is lower than V_{TxDIL}; the central logic receives Data1 when TxD voltage is higher than V_{TxDIH}.

7.1.3 Interstar Interface

The AS8223 has also an Interstar Interface (ISI) to connect two or more of the AS8223 and build a larger FlexRay Active Star (EAS: Extended Active Star). The signal on the ISI bus is a complementary digital signal transmitted and received by the Active Star on two bus lines TRxD_1 and TRxD_0. TRxD_1 and TRxD_0 are interpreted as logic high if the voltage at the pins is higher than V_{TRxD_IH} and are interpreted as logic low if the voltage is lower than V_{TRxD_IL}.

Table 25. Logic Table ISI Receiver

TRxD_0	TRxD_1	State
0	0	ISI Collision
0	1	Data_0
1	0	Data_1
1	1	Idle

Activity is detected if either Data_0 or Data_1 is detected on the ISI after the activity detection time $t_{ISActiveDetection}$ if the previous state was Idle. Idle is detected if TRxD_1 and TRxD_0 are logic high after the idle detection time $t_{ISIdleDetection}$ if the previous state was Activity. In case the ISI is switched to transmit, the logic table is shown in Table 26.

Table 26. Logic Table

TRxD_0	TRxD_1	State
0	1	Data_0
1	0	Data_1
1	1	Idle

The Interstar Interface has a built-in load regulator, therefore it does not require any additional components like resistors or capacitors when connecting several AS8223 devices.

7.1.4 Message Forwarding Function of the Active Star

The message forwarding includes all six communication paths (Branch 1 to 4, Communication Controller Interface and Interstar Interface). The message forwarding of FlexRay data streams is only performed in AS_NORMAL mode. On detecting activity on a communication path, the data stream is forwarded to all other communication paths. Activity on other communication paths will only be detected after the t_{ears_shut} time has expired. This is to avoid the unwanted transmission of echoes on the bus lines. As a safety measure a longer $t_{ears\_shut\_f}$ is used for branches that have detected electrical errors during the last transmission (open line, short to V_{CC} and GND, bus short). Collisions among the communication paths are described in Collisions on page 22. The data stream is passed to the central logic based on the specific communication path that is configured as the input data source. From the central logic the data stream is transmitted to all the communication paths, except for the communication path that is configured as the receiver.

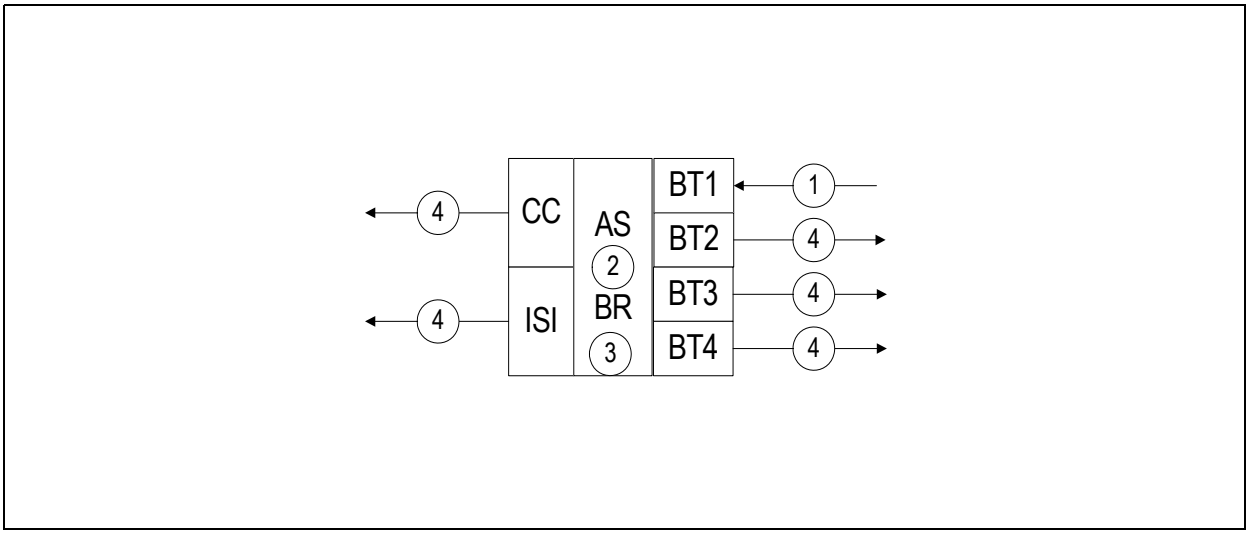
7.2 Routing Paths

There are three main routing configurations of the Active Star in AS_NORMAL mode.

7.2.1 Routing Path 1

- The incoming signal is received from one of the AS8223 bus lines (e.g. BT1).
- BT1 detects activity and indicates this on BT2, BT3, BT4, on the ISI and on the CC.
- The data stream is forwarded to BT2, BT3, BT4, to ISI and to CC.
- If BT1 detects idle on the bus, accordingly idle is indicated to BT2, BT3, BT4, to ISI and to CC.
- Now any other communication path can become the input data source.

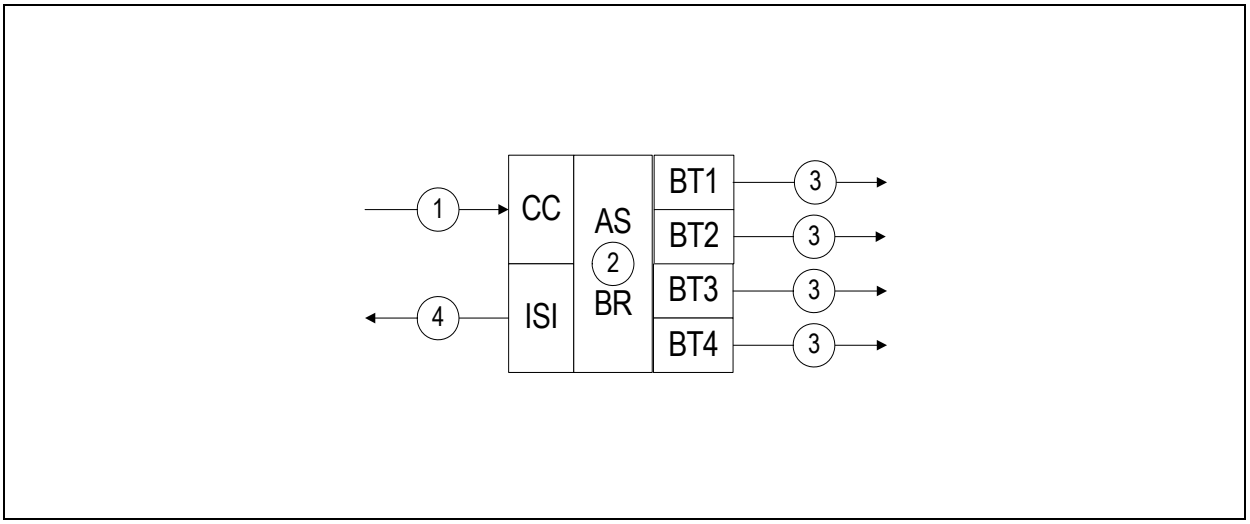
Figure 3. Routing Path 1



7.2.2 Routing Path 2

- The CC connected to the AS8223 is the input data stream source.
- First the Active Star detects activity on the CC and indicates activity on all BT and ISI.
- The data stream is then forwarded to all BT, to ISI and to CC.
- When idle on the CC is detected, accordingly idle is indicated to all BT, to ISI and to CC.
- Now any other communication path can become the input data source.

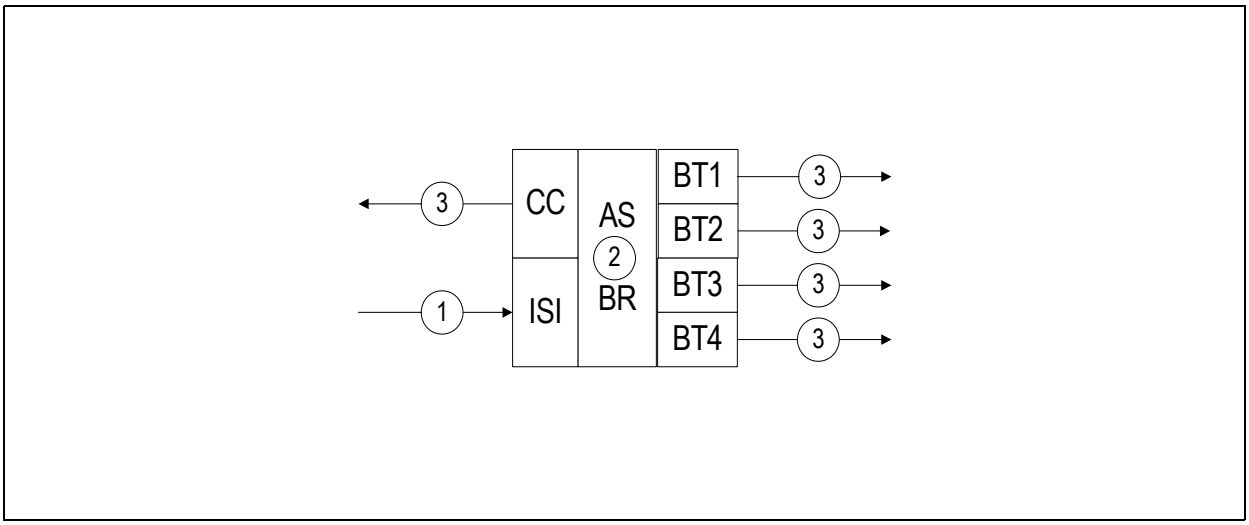
Figure 4. Routing Path 2



7.2.3 Routing Path 3

- A data stream from another AS8223 using the ISI is submitted.
- First the Active Star detects activity on the ISI and indicates activity on all BT and the CC.
- The data stream is forwarded to all BT and to CC.
- When idle on the ISI is detected, accordingly idle is indicated to all BT and to CC.
- Now any other communication path can become the input data source.

Figure 5. Routing Path 3



7.3 Collisions

7.3.1 Extended Active Star (EAS) Collision

Collision is detected on the Interstar Interface if TRxD_0 and TRxD_1 are lower than V_{TRxDIL} for a time longer than $t_{ISCollision}$ (ISI collision is possible only if two AS transmit different data on ISI).

7.3.2 Active Star Device Collision

Collision is detected if two or more elements: BT, CC or ISI are receiving an activity within a time t_{STAR_COL} or if one path: BT or CC are receiving an activity and EAS collision is detected or if only EAS collision is detected.

7.3.3 Active Star Collision Sequence

1. AS collision is detected.
2. DATA0 is forced on all communication paths except the colliding communication paths.
3. The colliding communication paths are detecting idle or they are in BT_FAILSILENT mode.
4. The CCI detects idle or timeout during collision.
5. The ISI is released to idle.
6. Idle or timeout is detected at the ISI.
7. Not colliding CCI and BT are released to idle.
8. End of AS collision.

7.4 Operation Mode of the Active Star Device

The AS8223 provides the following operating modes:

- AS_NORMAL: Non low power mode
- AS_STANDBY: Low power mode
- AS_SLEEP: Low power mode

7.4.1 APM (Autonomous Power Mode)

In Autonomous Power mode the AS8223 operates without host controller interaction. The APM flag indicates if the Autonomous Power mode is active or deactivated.

Autonomous Power mode is exited in case of

- A host command forcing the device to change the operation mode
- The APM flag is reset through a host command

The Autonomous Power mode is active

- After Power-on
- After a Wake-up event
- During undervoltage of V_{IO}
- The APM flag is reset via a host command

7.4.2 AS_NORMAL Mode

- The message forwarding is active (see Message Forwarding Function of the Active Star on page 20).
- If no activity is detected on the communication paths, BT is BRANCH_IDLE, ISI is idle and CCI is idle.
- If bus activity is detected at one BT, all BTs enter BRANCH_ACTIVE.
- If an undervoltage V_{CC} is detected, the device enters AS_STANDBY mode.
- If all communication paths stay inactive for longer than $t_{ASSLEEP}$ and the APM mode is set, the device enters AS_SLEEP mode.

7.4.3 AS_STANDBY Mode

- All branches are forced to BRANCH_LOWPOWER mode. The current consumption is significantly reduced compared to AS_NORMAL mode.
- Local and remote wake-up detector is active.
- If a wake-up event is detected, the device enters AS_NORMAL mode.
- If the undervoltage at V_{CC} recovers and the APM mode is set, the device enters AS_NORMAL mode.
- If all communication paths stay inactive for longer than $t_{ASSLEEP}$ and the APM flag is set, the device enters AS_SLEEP mode.
- If the undervoltage condition at V_{CC} persists for longer than $t_{UV\_DETECTION}$, the APM flag is set and power-on flag is set, the device enters AS_SLEEP mode.

7.4.4 AS_SLEEP Mode

- All branches are forced to BRANCH_LOWPOWER mode. The current consumption is reduced compared to AS_NORMAL and AS_STANDBY mode.
- Local and remote wake-up detector is active.
- If a wake-up event is detected, the device enters AS_NORMAL mode.

7.5 Non Operating Modes of the Active Star

The AS8223 provides the following non-operating mode:

7.5.1 AS_POWEROFF

- In this mode the device is not operable.
- INH1 and INH2 are floating.
- Branches are in idle_HZ.
- Local and remote wake-up detector is active.
- RxD and RxEN are set to high.

7.6 Mode Transitions of the Active Star

Starting from every operation mode the device enters AS_POWEROFF in case a power off event occurs regardless of wake-up events and host commands.

Starting from the AS_POWEROFF mode the device enters AS_STANDBY only in case a power on event occurs.

Starting from the AS_STANDBY mode the device enters AS_NORMAL if a wake-up event occurs regardless of any of the undervoltage flags and host commands.

Starting from the AS_NORMAL mode the device enters AS_STANDBY in case V_{CC} undervoltage reaction flag is set regardless of wake-up events and host commands.

Starting from the AS_NORMAL mode the device will stay in AS_NORMAL even if V_{BAT} undervoltage flag is set.

Starting from the AS_NORMAL mode the device will stay in AS_NORMAL even if V_{IO} undervoltage flag is set.

Starting from the AS_SLEEP mode the device enters AS_NORMAL if a wake-up event occurs regardless of any of the undervoltage flags and host commands.

Figure 6. State Machine

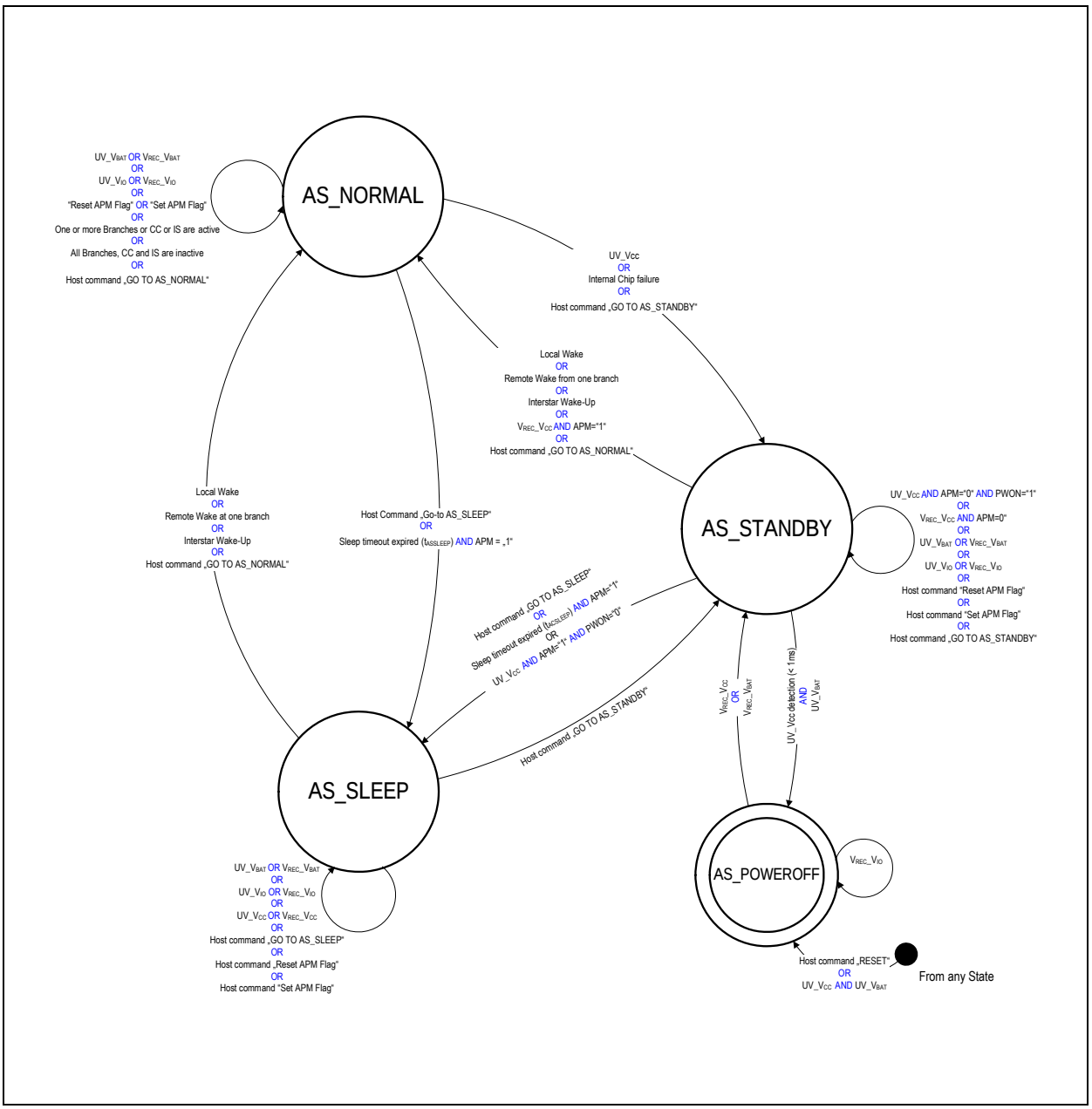


Table 27. Active Star Mode Transition

Initial Mode	Resulting Mode	Condition	Priority
AS_NORMAL	AS_POWEROFF	Undervoltage VCC detection (<1ms) AND undervoltage VBAT event	1
	AS_STANDBY	Undervoltage VCC detection (<1ms)	2
	AS_STANDBY	Internal chip failure	3
	AS_STANDBY	Host command “go to AS_STANDBY mode”	4
	AS_SLEEP	Host command “go to AS_SLEEP mode”	4
	AS_SLEEP	Sleep timeout expired ($t_{ASSLEEP}$) AND APM flag set	5
	AS_NORMAL	Undervoltage VBAT event	6
	AS_NORMAL	Undervoltage recovery VBAT event	6
	AS_NORMAL	Undervoltage VIO event	6
	AS_NORMAL	Undervoltage recovery VIO event	6
	AS_NORMAL	Host command “reset APM flag”	6
	AS_NORMAL	Host command “set APM flag”	6
	AS_NORMAL	All branches, CC and ISI are inactive	6
	AS_NORMAL	One or more branches or CC or ISI are active	6
	AS_NORMAL	Host command “go to AS_NORMAL mode”	6
AS_STANDBY	AS_POWEROFF	Undervoltage VCC reaction (<1ms) AND undervoltage VBAT event	1
	AS_NORMAL	Local Wake event	2
	AS_NORMAL	Remote Wake event from branch_1	2
	AS_NORMAL	Remote Wake event from branch_2	2
	AS_NORMAL	Remote Wake event from branch_3	2
	AS_NORMAL	Remote Wake event from branch_4	2
	AS_NORMAL	Wake on Interstar Interface detected	2
	AS_NORMAL	Undervoltage recovery VCC event AND APM flag is set	3
	AS_NORMAL	Host command “go to AS_NORMAL mode”	4
	AS_SLEEP	Host command “go to AS_SLEEP mode”	4
	AS_SLEEP	Sleep timeout expired ($t_{ASSLEEP}$) AND APM flag set	5
	AS_SLEEP	Undervoltage VCC event and APM flag is set and PWON=0	6
	AS_STANDBY	Undervoltage VCC event and (APM flag is not set or PWON=1)	7
	AS_STANDBY	Undervoltage recovery VCC event AND APM flag is not set	7
	AS_STANDBY	Undervoltage VBAT event	7
	AS_STANDBY	Undervoltage recovery VBAT event	7
	AS_STANDBY	Undervoltage VIO event	7
	AS_STANDBY	Undervoltage recovery VIO event	7
	AS_STANDBY	Host command “reset APM flag”	7
	AS_STANDBY	Host command “set APM flag”	7
	AS_STANDBY	Host command “go to AS_STANDBY mode”	7

Table 27. Active Star Mode Transition

Initial Mode	Resulting Mode	Condition	Priority
AS_SLEEP	AS_POWEROFF	Undervoltage VCC reaction (<1ms) AND undervoltage VBAT event	1
	AS_NORMAL	Local Wake event	2
	AS_NORMAL	Remote Wake event from branch_1	2
	AS_NORMAL	Remote Wake event from branch_2	2
	AS_NORMAL	Remote Wake event from branch_3	2
	AS_NORMAL	Remote Wake event from branch_4	2
	AS_NORMAL	Wake on Interstar Interface detected	2
	AS_NORMAL	Host command “go to AS_NORMAL mode”	3
	AS_STANDBY	Host command “go to AS_STANDBY mode”	3
	AS_SLEEP	Undervoltage VBAT event	4
	AS_SLEEP	Undervoltage recovery VBAT event	4
	AS_SLEEP	Undervoltage VIO event	4
	AS_SLEEP	Undervoltage recovery VIO event	4
	AS_SLEEP	Undervoltage VCC event APM flag is not set	4
	AS_SLEEP	Undervoltage VCC event APM flag is set	4
	AS_SLEEP	Undervoltage recovery VCC event	4
	AS_SLEEP	Host command “go to AS_SLEEP mode”	4
	AS_SLEEP	Host command “reset APM flag”	4
	AS_SLEEP	Host command “set APM flag”	4
AS_POWEROFF	AS_STANDBY	Undervoltage recovery VCC event	1
	AS_STANDBY	Undervoltage recovery VBAT event	1
	AS_POWEROFF	Undervoltage recovery VIO event	2

Table 28. Pin Signalling and Operating Modes

Operating Mode	Outputs	
	RxD	RxEN
AS_NORMAL	L Bus = Data_0	L Bus = Active
	H Bus = Idle or Data_1	H Bus = Idle
AS_STANDBY	not (Wake-up flag)	not (Wake-up flag)
AS_SLEEP	not (Wake-up flag)	not (Wake-up flag)

7.7 BRANCH Operating Modes

Each branch of an Active Star has the following operating modes:

- BRANCH_LOWPOWER: Low power mode
- BRANCH_IDLE: Non low power mode
- BRANCH_ACTIVE: Non low power mode
- BRANCH_DISABLED: Low power mode
- BRANCH_FAILSILENT: Non low power mode

7.7.1 BRANCH_LOWPOWER Mode

- Receiver and transmitter are deactivated.
- The branch signals Idle_LP on the bus.
- The wake-up detector is activated.
- If a wake-up is detected the branch forces the Active Star into AS_NORMAL mode.
- In case the Active Star statemachine enters AS_NORMAL mode the branch enters BRANCH_IDLE.

7.7.2 BRANCH_IDLE Mode

- Receiver and transmitter are deactivated.
- Activity detection is active.
- The wake-up detector is deactivated.
- The branch signals Idle on the bus.
- The branch enters BRANCH_ACTIVE if activity is detected on this branch (and the ears_shut timer has expired), or on another branch activity is detected.
- The branch enters BRANCH_DISABLED upon host command.
- The branch enters BRANCH_LOWPOWER if the Active Star statemachine leaves AS_NORMAL mode.

7.7.3 BRANCH_ACTIVE Mode

- Receiver and transmitter are activated.
- The wake-up detector is deactivated.
- If BRANCH_ACTIVE is entered upon detection of activity on the bus, the received data stream is passed to the central logic.
- If BRANCH_ACTIVE is entered upon request of the Active Star statemachine, the data stream coming from the central logic is transmitted by this branch to the bus.
- In case Idle is detected on the branch and no transmission is requested by internal logic then BRANCH_IDLE is entered.
- After receiving a data stream on a branch for longer than $t_{BranchNoiseTimeout}$ the branch is excluded from communication and enters BRANCH_FAILSILENT.
- The branch enters BRANCH_DISABLED upon host command.
- The branch enters BRANCH_LOWPOWER if the Active Star statemachine leaves AS_NORMAL mode.

7.7.4 BRANCH_DISABLED Mode

- This state is only entered upon host command.
- Receiver and transmitter are deactivated.
- The wake-up detector is deactivated.
- The branch signals Idle_LP on the bus.
- If in BRANCH_DISABLED, the branch is forced into BRANCH_LOWPOWER if the Active Star statemachine leaves AS_NORMAL mode.
- The branch enters BRANCH_IDLE upon host command.

7.7.5 BRANCH_FAILSILENT Mode

- Receiver and transmitter are deactivated.
- The branch signals Idle on the bus.
- The wake-up detector is deactivated.
- In case Idle is detected at a branch for at least t_{exit_fail}, then BRANCH_IDLE is entered.
- The branch enters BRANCH_DISABLED upon host command.
- The branch enters BRANCH_LOWPOWER if the Active Star statemachine leaves AS_NORMAL mode.

7.8 Non Operating Modes of BRANCH Logic

The AS8223 provides the following non-operating mode:

7.8.1 BRANCH_POWEROFF Mode

- This state is entered if the Active Star enters AS_POWEROFF.
- Activity detection and wake-up detection are deactivated in this state.
- The bus wires are not terminated to GND (bus state: Idle_HZ).
- In case the Active Star statemachine enters AS_STANDBY the branch enters BRANCH_LOWPOWER.

7.9 Branch Transitions

Figure 7. Branch State Machine

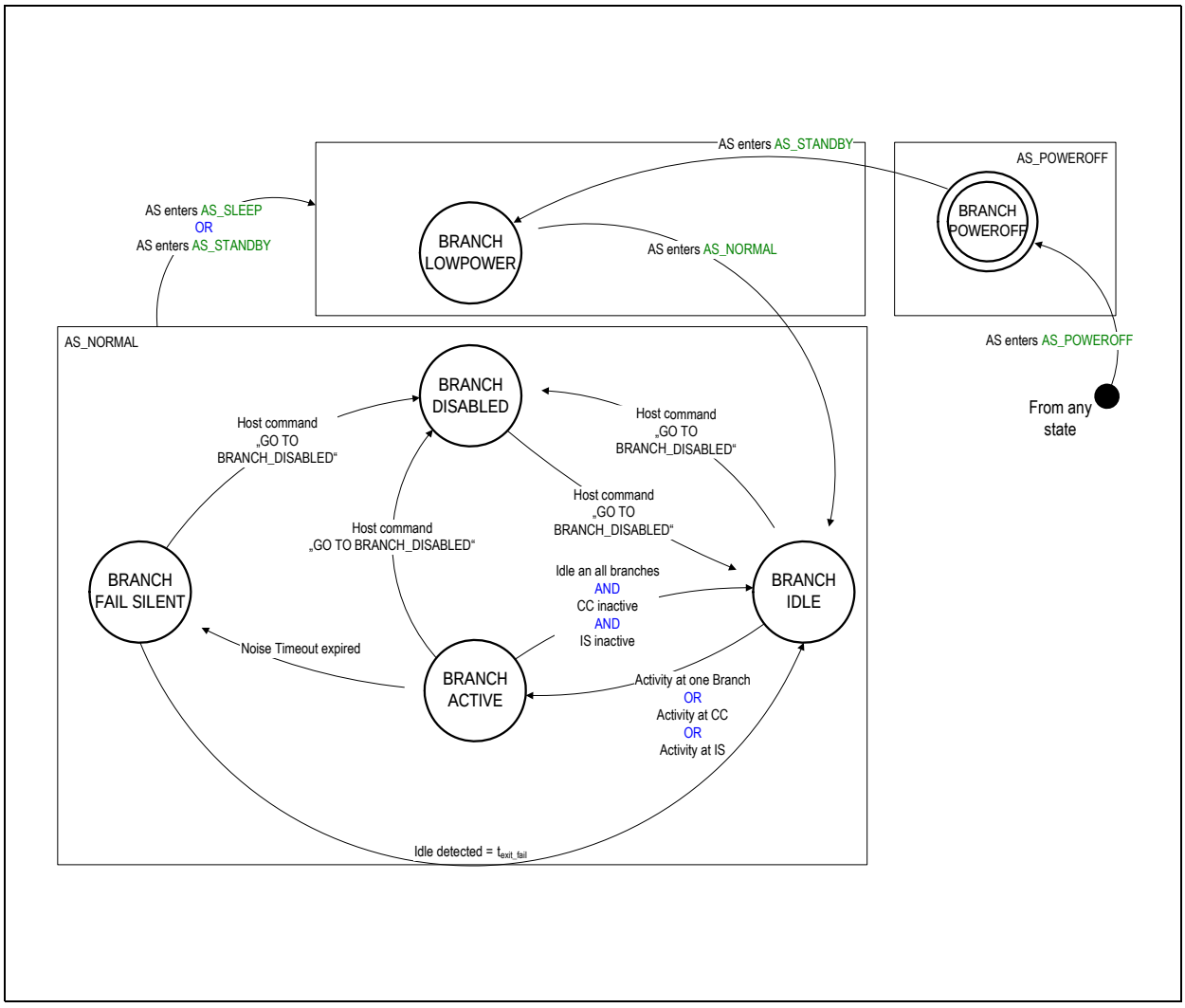


Table 29. Branch Transition

Initial Mode	Resulting Mode	Condition	Priority
BRANCH _ACTIVE	BRANCH_POWEROFF	Active Star enters AS_POWEROFF	1
	BRANCH_LOWPOWER	Active Star enters AS_SLEEP	2
	BRANCH_LOWPOWER	Active Star enters AS_STANDBY	2
	BRANCH_DISABLED	Host command “go to BRANCH_DISABLED mode”	3
	BRANCH_FAILSILENT	Noise timeout expired	4
	BRANCH_FAILSILENT	Bus error detected	5
	BRANCH_IDLE	Idle on all branches AND CC inactive AND ISI inactive	6
BRANCH_IDLE	BRANCH_POWEROFF	Active Star enters AS_POWEROFF	1
	BRANCH_LOWPOWER	Active Star enters AS_SLEEP	2
	BRANCH_LOWPOWER	Active Star enters AS_STANDBY	2
	BRANCH_DISABLED	Host command “go to BRANCH_DISABLED mode”	3
	BRANCH_ACTIVE	Bus Activity detected on this branch	4
	BRANCH_ACTIVE	Bus Activity detected on other branch	4
	BRANCH_ACTIVE	Activity detected on CC	4
	BRANCH_ACTIVE	Activity detected on ISI	4
BRANCH_LOWPOWER	BRANCH_POWEROFF	Active Star enters AS_POWEROFF	1
	BRANCH_LOWPOWER	Active Star enters AS_SLEEP	2
	BRANCH_LOWPOWER	Active Star enters AS_STANDBY	2
	BRANCH_IDLE	Active Star enters AS_NORMAL	3
BRANCH_DISABLED	BRANCH_POWEROFF	Active Star enters AS_POWEROFF	1
	BRANCH_LOWPOWER	Active Star enters AS_SLEEP	2
	BRANCH_LOWPOWER	Active Star enters AS_STANDBY	2
	BRANCH_IDLE	Host command “go to BRANCH_IDLE mode”	3
BRANCH_FAILSILENT	BRANCH_POWEROFF	Active Star enters AS_POWEROFF	1
	BRANCH_LOWPOWER	Active Star enters AS_SLEEP	2
	BRANCH_LOWPOWER	Active Star enters AS_STANDBY	2
	BRANCH_DISABLED	Host command “go to BRANCH_DISABLED mode”	3
	BRANCH_IDLE	Idle detected for at least t_{exit_fail}	4
BRANCH_POWEROFF	BRANCH_LOWPOWER	Active Star enters AS_STANDBY	1

7.10 Undervoltage Events

7.10.1 Undervoltage VCC Reaction Event

An undervoltage V_{CC} event is detected if the V_{CC} voltage falls below V_{CCTHL} for a time longer than $t_{UV\_REACTION}$.

7.10.2 Undervoltage VCC Detection Event

An undervoltage V_{CC} event is detected if the V_{CC} voltage falls below V_{CCTHL} for a time longer than $t_{UV\_DETECTION}$.

7.10.3 Undervoltage Recovery VCC Event

An undervoltage recovery at VCC is detected if the VCC voltage exceeds the voltage threshold V_{CCTHH} for a time longer than $t_{UV\_RECOVERY}$.

7.10.4 Undervoltage VBAT Event

An undervoltage VBAT event is detected if the VBAT voltage falls below V_{BATTHL} for a time longer than $t_{UV\_REACTION}$.

7.10.5 Undervoltage Recovery VBAT Event

An undervoltage recovery at VBAT is detected if VBAT exceeds the voltage threshold V_{BATTHH} for a time longer than $t_{UV\_RECOVERY}$.

7.10.6 Undervoltage VIO Event

An undervoltage VIO event is detected if the VIO voltage falls below V_{IOTHL} for a time longer than $t_{UV\_REACTION}$.

7.10.7 Undervoltage Recovery VIO Event

An undervoltage recovery of VIO is detected if VIO exceeds the voltage threshold V_{IOTHH} for a time longer than $t_{UV\_RECOVERY}$.

7.10.8 Power On/Off Events

- Starting from AS_POWEROFF mode a power-on (PWON) event occurs if either VBAT or VCC undervoltage flag is reset.
- A power off event in any operation mode is detected in case VBAT and VCC undervoltage flags are set.

7.11 Wake-up Events

A wake-up event can be detected only in low power modes of the Active Star (AS_STANDBY and AS_SLEEP) if one of the following events occur:

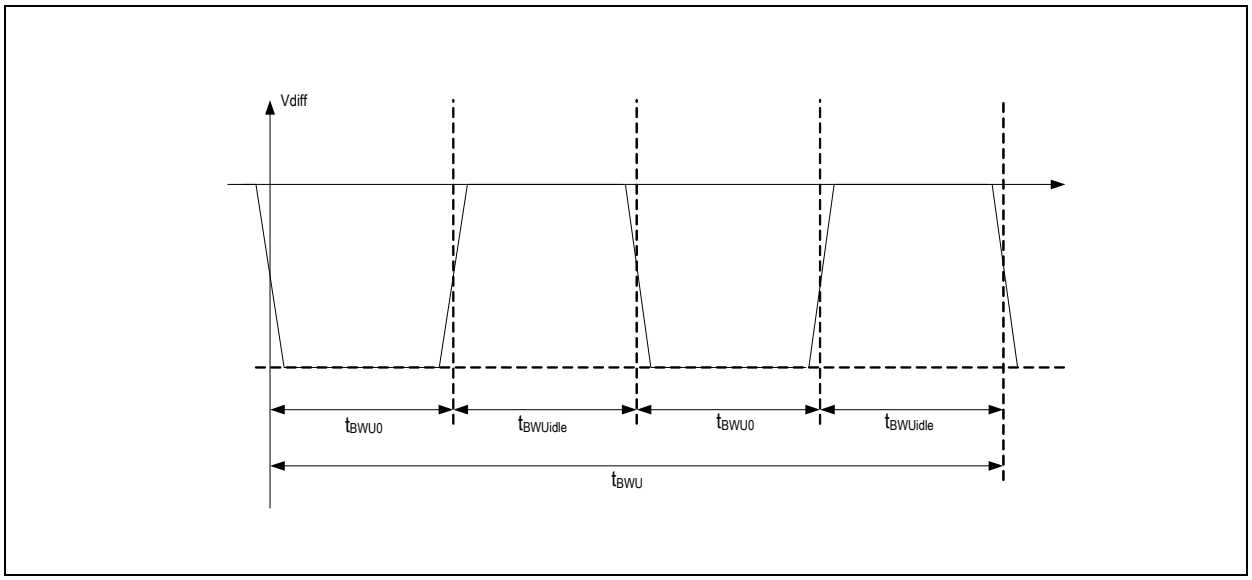
- Remote wake event on one or more branches
- Local wake-up event
- ISI wake-up event

7.11.1 Remote Wake-up Event

A remote wake-up event is detected after the reception of at least two consecutive wake-up symbols within t_{BWU} in BRANCH_LOWPOWER. The wake-up symbol is defined as Data_0 longer than t_{BWU0} followed by Idle or Data_1 longer than $t_{BWUidle}$ Every branch has a remote wake-up detector with its corresponding remote wake-up flag implemented. A remote wake-up flag is set if a remote wake-up event occurs.

It is possible to disable the remote wake-up sensitivity on selected branches by setting the corresponding bits in the Remote Wakeup Disable register (see page 40). A disabled branch will reduce power consumption during AS_STANDBY mode. Upon wake-up, the branch transceiver will be enabled only if VCC is higher than V_{CCTHH} for longer than $t_{UV\_DEBOUNCING}$.

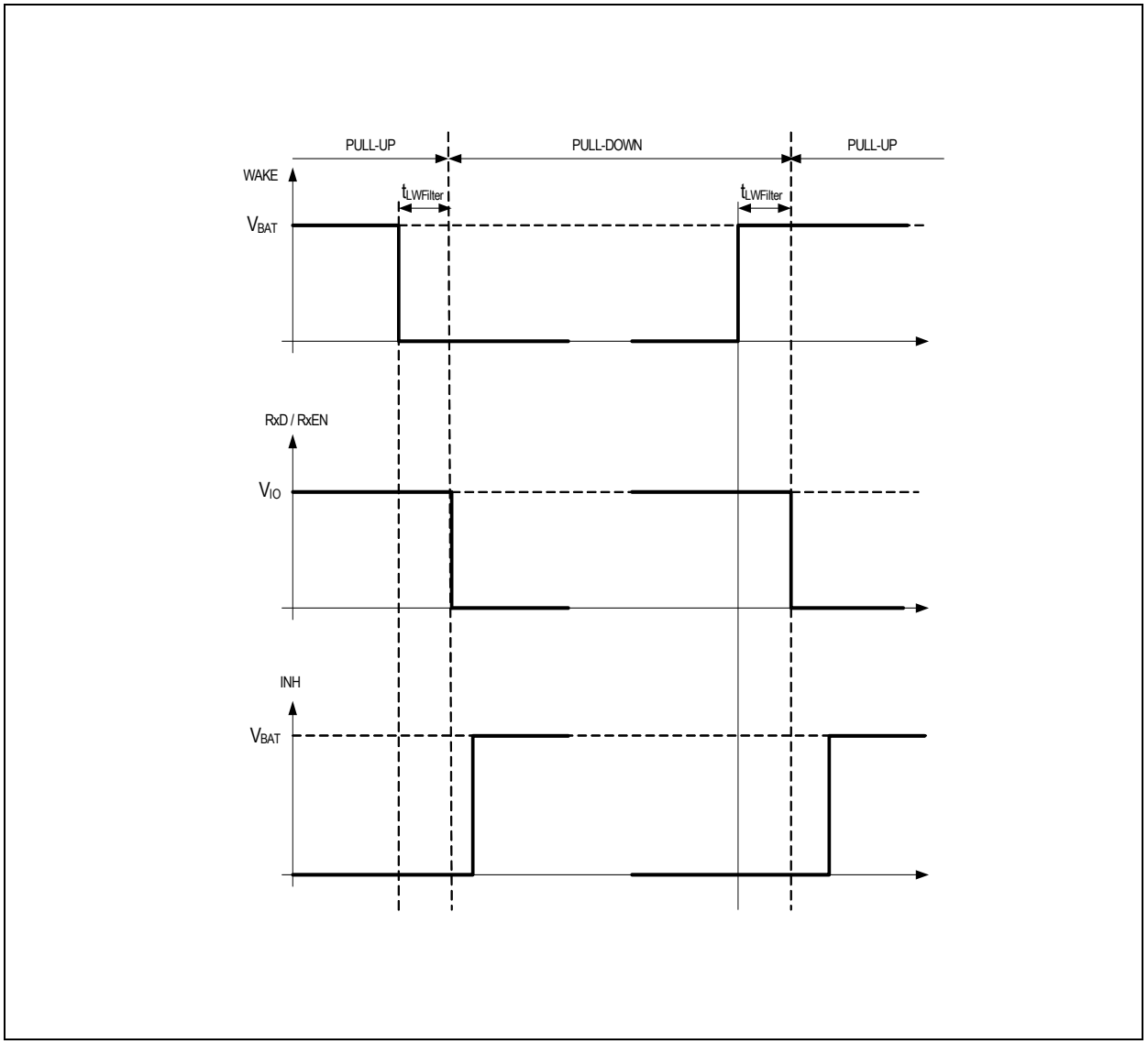
Figure 8. Signal for Wake-up Pattern Recognition



7.11.2 Local Wake-up Event

In all low power modes of the Active Star, if the voltage on the WAKE pin falls below V_{LWUTH} for longer than $t_{LWFilter}$, a local wake-up event is detected. At the same time the biasing of the pin is switched to pull-down. If the voltage on the WAKE pin rises above V_{LWUTH} for longer than $t_{LWFilter}$, a local wake-up event is detected. At the same time the biasing of the pin is switched to pull-up. The pull-up and down mechanism of the local wake pin is active in all operation modes of the ASD.

Figure 9. WAKE Input Pin Behavior



7.11.3 Interstar Wake-up Event

In all low power modes of the Active Star (AS_SLEEP, AS_STANDBY), an activity on the ISI generates an ISI wake-up event.

7.12 Host Interface Events

An host interface event is detected if one of the host commands “go to AS_NORMAL mode”, “go to AS_SLEEP mode”, “go to AS_STANDBY mode”, “set APM flag” or “reset APM flag” is received via the SPI interface (rising edge on the CSN pin).

7.13 Sleep Timer Events

7.13.1 Enable Condition

Starting from AS_NORMAL mode or AS_STANDBY mode the sleep timer is enabled when APM flag is set and no activity on BT, ISI and CC is detected.

7.13.2 Reset Condition

The sleep timer is reset and it starts again whenever a host command (set/reset APM, go to command, set/reset FIN) or activity at one of the communication elements is detected or a higher priority event causes a transition between the Active Star states.

7.13.3 Timeout Condition

Starting from AS_NORMAL mode or AS_STANDBY mode, sleep timer event occurs if the sleep timer expired after $t_{ASSLEEP}$.

7.14 Loss of Ground

In case the ground of the device is disconnected and the host pins are open the bus lines are switched to Idle_HZ.

7.15 Error and Status Flags

The Active Star device has a general error/status register and four branch error/status registers.

7.15.1 General Active Star Error Flags

Undervoltage V_{BAT} Flag UVVBAT_det. The UVVBAT_det flag is set if an undervoltage V_{BAT} event is detected. The flag is reset if an undervoltage recovery V_{BAT} event is detected and if a wake-up event is detected.

Undervoltage VIO Flag UVVIO_det. The UVVIO_det flag is set if an undervoltage V_{IO} event is detected. The flag is reset if an undervoltage recovery V_{IO} event is detected, when the Active Star enters AS_POWEROFF and if a wake-up event is detected.

Undervoltage VCC Flag UVVCC_det. The UVVCC_det flag is set if an undervoltage V_{CC} event is detected. The flag is reset when an undervoltage recovery V_{CC} event is detected and if a wake-up event is detected.

Over-temperature Flag OT. This flag can only be set/reset in the AS_NORMAL. The flag is set if the junction temperature exceeds OTTH and it is reset if the junction temperature falls below OTTL. The bus drivers are disabled when this flag is set.

Communication Controller Timeout Flag TxEN_Timeout. If in AS_NORMAL the Communication Controller keeps the TxEN signal asserted low and the BGE asserted high for a time longer than $t_{ActiveTimeout}$ the CC Noise Timeout will be set, the Active Star will ignore the signal coming from TxD at the CC Interface and behave as if TxEN would be high. The flag is reset after t_{exit_fail} since the TxEN signal is driven high or BGE is driven low and in AS_POWEROFF.

Interstar Noise Timeout Flag IS_TIMEOUT. When at the Interstar interface for longer than $t_{ISNoiseTimeout}$ activity is detected, the Interstar Noise Timeout flag will be set, the Active Star will ignore the data signal coming from the Interstar interface. The flag is reset after t_{exit_fail} since Idle is detected and when entering AS_POWEROFF.

7.15.2 General Active Status Flags

Power-On Flag PWON. The power-on flag is set in the AS_POWEROFF state and it is reset entering AS_NORMAL.

Undervoltage VCC Reaction Flag UVVCCREA_det. The UVVCCREA_det flag is set when an undervoltage V_{CC} reaction event is detected. The flag is reset when an undervoltage recovery V_{CC} event is detected, when a wake-up event is detected.

Autonomous Powering Mode Flag APM. When the Active Star is in its autonomous powering mode, the APM flag is set. When the Active Star leaves the Autonomous Powering mode the APM flag is reset.

Local Wake Flag LWAKE. The local wake-up flag is set if a local wake-up event occurs. The local wake-up flag is reset entering a low power mode from AS_NORMAL, when an undervoltage event occurs and entering AS_POWEROFF.

Interstar Wake Flag ISWAKE. The ISI wake-up flag is set if an ISI wake-up event occurs. The ISI wake-up flag is reset entering a low power mode from AS_NORMAL, when an undervoltage event occurs and entering AS_POWEROFF.

Global Wake Flag WAKE. The flag is the logical “OR” between LWAKE, ISWAKE and the RWAKE flags of all branches.

Communication Controller Collision Flag CC_COL. This flag is set when CC and ISI or BT are receiving an activity within a time t_{STAR_COL}. The flag is reset when all the paths signal no activity to the central logic and in AS_POWEROFF.

ISI Collision Flag ISI_COL. This flag is set when ISI and BT or CC are receiving an activity within a time t_{STAR_COL}. The flag is reset when all the paths signal no activity to the central logic and in AS_POWEROFF.

EAS Collision Flag EAS_COL. This flag is set when an EAS collision is detected. The flag is reset when EAS collision is not present and in AS_POWEROFF.

General Collision Flag COLLISION. This flag is the logical “OR” of all collision flags.

AS Operation Mode Flag AS1:AS0. The current operating mode of the Active Star is coded with two flags on the status register.

Table 30. State Coding of Active Star

AS1:AS0	Active Star State
00	AS_POWEROFF
01	AS_STANDBY
10	AS_NORMAL
11	AS_SLEEP

7.15.3 Branch Error Flags

Flags related to branch errors can be read on the branch status flag registers (at address 0x02, 0x03, 0x04, 0x05).

Bus Error. The bus error flag is set when 2 consecutive rising edges on the TxD pin without any rising edge on the RxD pin are detected or if 2 consecutive falling edges on the TxD pin without any falling edge on the RxD pin are detected.

This flag can be set only in BRANCH_ACTIVE mode of the branch operation states if the transmitter is enabled. The flag is reset after readout and in AS_SLEEP or AS_STANDBY mode.

Low and High Current Internal Flag. These flags can be set in BRANCH_ACTIVE if the driver is enabled and during the transmission of Data1 or Data0 for at least t_{BUS_ERROR}.

The flags are reset after readout or if the branch enters the BRANCH_LOWPOWER state.

Table 31. Low Current and High Current Internal Flags

Flag	Set Condition on Data	Set Condition on Pin Current
Low current BP high side driver	Data1	$\|I_{BP}\| < I_{THL}$ for more than t_{BUS_ERROR}
Low current BP low side driver	Data0	$\|I_{BP}\| < I_{THL}$ for more than t_{BUS_ERROR}
Low current BM high side driver	Data0	$\|I_{BM}\| < I_{THL}$ for more than t_{BUS_ERROR}
Low current BM low side driver	Data1	$\|I_{BM}\| < I_{THL}$ for more than t_{BUS_ERROR}
High current BP high side driver	Data1	$\|I_{BP}\| > I_{THH}$ for more than t_{BUS_ERROR}
High current BP low side driver	Data0	$\|I_{BP}\| > I_{THH}$ for more than t_{BUS_ERROR}
High current BM high side driver	Data0	$\|I_{BM}\| > I_{THH}$ for more than t_{BUS_ERROR}
High current BM low side driver	Data1	$\|I_{BM}\| > I_{THH}$ for more than t_{BUS_ERROR}

Note: Detection of the fault conditions depends on the FlexRay network design.

BP Open Line. This flag is the logical “OR” between “low current on BP high side” and “low current on BP low side”.

BM Open Line. This flag is the logical “OR” between “low current on BM high side” and “low current on BM low side”.

BP Short Circuit to VCC. This flag is set if “high current on BP low side” flag is set.

BP Short Circuit to GND. This flag is set if “high current on BP high side” flag is set.

BM Short Circuit to VCC. This flag is set if “high current on BM low side” flag is set.

BM Short Circuit to GND. This flag is set if “high current on BM high side” flag is set.

Short Circuit Between BP and BM. This flag can only be set in BRANCH_ACTIVE mode in case the driver is enabled. The bus activity signal (RxEN) is low during transmission, otherwise the flag is set. The flag is reset after readout and if the branch enters BRANCH_LOWPOWER.

Note: The flag is meaningful only if no other short circuit flag is set.

Branch Noise Timeout BRANCH_timeout. Starting from BRANCH_ACTIVE after receiving activity for longer than $t_{BranchNoiseTimeout}$ the noise timeout flag of this branch will be set, the branch is then excluded from communication and enters BRANCH_FAILSILENT. The flag is reset after t_{exit_fail} since Idle is detected and if the branch enters BRANCH_LOWPOWER.

7.15.4 Branch Status Flags

Bus Activity Flag BUSACTIVE. Starting from a non low power mode if activity is detected on the bus the BUSACTIVE flag is set. The flag is reset if the bus becomes idle or enters BRANCH_LOWPOWER.

Branch Collision Flag BT_COL. This flag is set if BT and ISI or CC are receiving an activity within a time t_{STAR_COL}. The flag is reset after readout and in AS_SLEEP or AS_STANDBY mode.

Remote Wake Flag RWAKE. The remote wake-up flag is set if a remote wake-up event is detected. The remote wake-up flag is reset entering a low power mode from AS_NORMAL, if an undervoltage event occurs and entering AS_POWEROFF.

Branch Operating Mode Flags BS2:BS1:BS0.

Table 32. BS2:BS1:BS0

BS2:BS1:BS0	
000	BRANCH_POWEROFF
001	BRANCH_LOWPOWER
010	BRANCH_IDLE
011	BRANCH_ACTIVE
100	BRANCH_DISABLED
101	BRANCH_FAILSILENT
110	BRANCH_TXONLY

Branch Logical Idle Flag BRANCH_IDLE. This flag is reset in BRANCH_ACTIVE and it is set in all the other branch modes.

7.16 INTN

Starting from every operating mode INTN is forced to digital low in case one error flag or a collision flag is changing its value. Starting from AS_SLEEP or AS_STANDBY the INTN pin is forced low also in case a wake-up event is detected. INTN is released to digital high in case of SPI reading command to address 0x00. The pin is low at AS_POWEROFF.

7.17 SPI Interface

The SPI interface is for reading operations of the status flags and for accepting commands from the host controller. The SPI access is only possible if UVVIO flag is not set and at least one of the UVVCC or UVVBAT flags is reset. In case the SCSN is high, the SDO pin is switched to high impedance.

The status flags of the Active Star device are organized in 6 status registers, one for the Active Star, one for the Controller/Interstar Interface and four registers for the status and error flags for the branches. These registers are read only (every write access is ignored).

There are 8 command registers. With the command registers state transitions of the Active Star or branch transitions are initiated, as well the APM and FIN flag is set and reset or the INTN is forced to low. The command register can be read.

7.17.1 SPI Frame

Within one SCSN cycle (SCSN on logical low) 16 clock periods (SCLK) are expected. Any deviation in the number of clock periods is recognized as an error and the access is ignored. Any bit sampling is performed with the falling clock edge and the data is shifted with the rising clock edge (starting from MSB).

A frame is done by a first byte for command (write or read) and address and a following byte that can be the data to write or an undefined sequence of bits when the command is read. Command is coded on the first bit, while address is given on 7 bits.

Table 33. First SPI Frame Byte

Command							
CMD	A6	A5	A4	A3	A2	A1	A0

Table 34. Second SPI Frame Byte

Command							
D7	D6	D5	D4	D3	D2	D1	D0

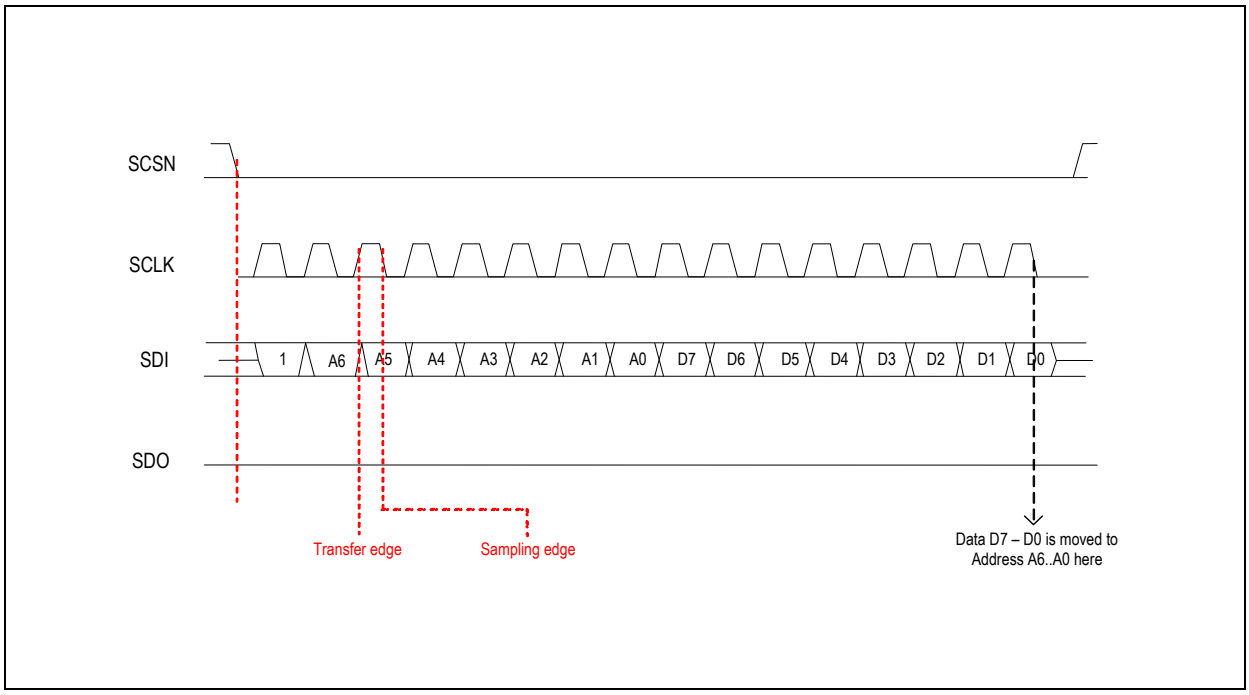
Table 35. SPI Command Code

CMD	Command	<A6:A0>	Description
1	WRITE	ADDRESS	Writes data byte on the given address
0	READ	ADDRESS	Reads data byte from the given address

In case of read command the value of the addressed register is loaded on the 16th SCLK falling edge, if another SCLK falling edge is received before SCSN rising edge this data is discharged. If the read SPI frame is valid, on the 1st SCLK rising edge of the next frame (write or read frame) the SPI starts shifting out the previous loaded value, starting with the MSB. On the 16th falling edge of SCLK the read out sequence stops, the SPI can be released by returning the level of SCSN to High. As soon as SCSN is high the SDO output goes low. If the previous frame was not valid or it was a write command the SDO output remains low.

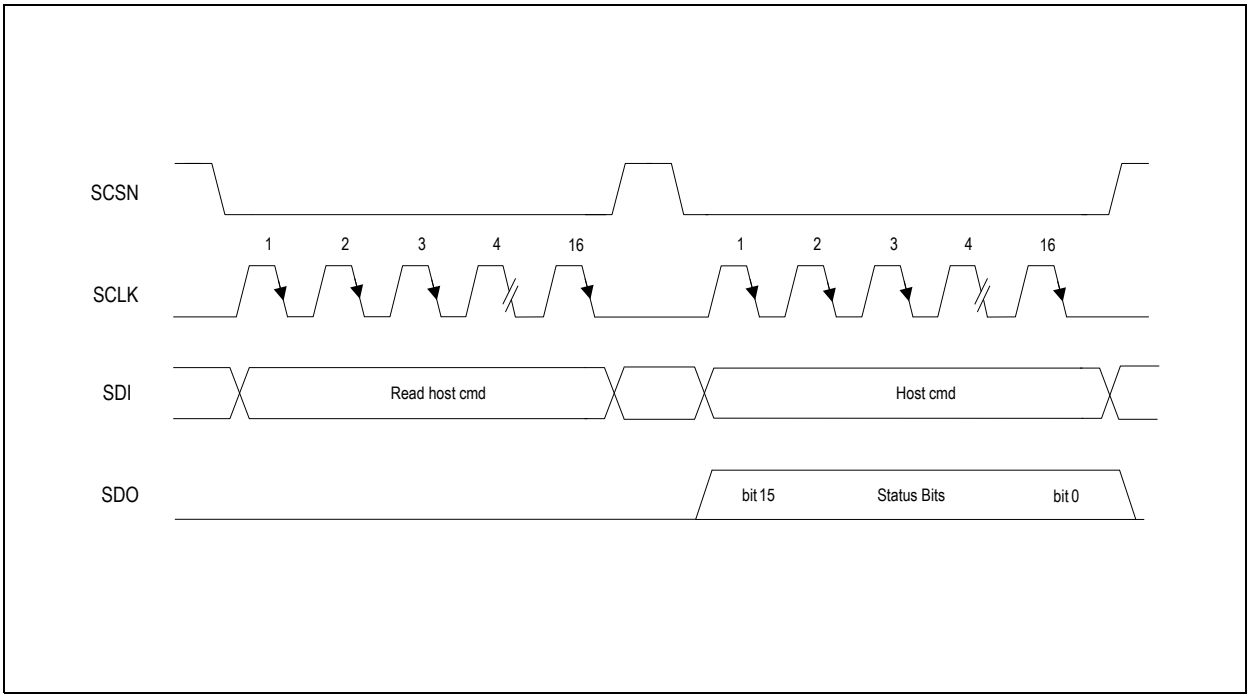
7.17.2 Write Access (no previous valid read access)

Figure 10. SPI Write Access (in case no previous valid read command is received SDO stays low)



7.17.3 Read Access

Figure 11. SPI Read Access (second host command can be a write or a read command)



7.17.4 Register Settings

Table 36. Register Settings

Register	Address	Type	Reset Value
AS status flag register	0x00	read-only	0x0067
CC/ISI status flag register	0x01	read-only	0x0000
Branch 1 status flag register	0x02	read-only	0x8000
Branch 2 status flag register	0x03	read-only	0x8000
Branch 3 status flag register	0x04	read-only	0x8000
Branch 4 status flag register	0x05	read-only	0x8000
APM flag command register	0x06	read/write	0x0001
AS Host command register	0x07	read/write	0x0000
Branch 1 command register	0x08	read/write	0x0000
Branch 2 command register	0x09	read/write	0x0000
Branch 3 command register	0x0A	read/write	0x0000
Branch 4 command register	0x0B	read/write	0x0000
Reserved	0x0C	-	-
Reserved	0x0D	-	-
Noise Timeout register	0x0E	read/write	0x00BB
Texit_fail register	0x0F	read/write	0x0057
Tears_shut register	0x10	read/write	0x000A
POR register	0x11	read/write	0x0000
Tears_shut_faulty register	0x12	read/write	0x0031
Remote wake-up disable register	0x13	read/write	0x0000
VCCUV_filter register	0x14	read/write	0x000F

AS Status Flag Register (address 0x00, read-only).

Table 37. Status Register Bits of Active Star

Bit	AS Status Flags	Symbol
Bit 0	Undervoltage V_{BAT}	UVVBAT_det
Bit 1	Undervoltage V_{IO}	UVVIO_stored[1]
Bit 2	Undervoltage V_{CC}	UVVCC_det
Bit 3	Over temperature	OT
Bit 4	Global Wake	WAKE
Bit 5	Autonomous Power Mode active	APM
Bit 6	Power on	PWON
Bit 7	Local Wake	LWAKE
Bit 8	Internal frequency	FIN
Bit 9	Error or Wake-up in CC/ISI status	ERRWAKE0
Bit 10	Error or Wake-up in BR1 status	ERRWAKE1
Bit 11	Error or Wake-up in BR2 status	ERRWAKE2

Table 37. Status Register Bits of Active Star

Bit	AS Status Flags	Symbol
Bit 12	Error or Wake-up in BR3 status	ERRWAKE3
Bit 13	Error or Wake-up in BR4 status	ERRWAKE4
Bit [14:15]	Active Star State	AS1:AS0

1. UVVIO_stored is set if UVVIO_det is set and it is reset after an SPI access.

CC / ISI Status Flag Register (address 0x01, read-only).

Table 38. Status Register Bits of Controller / ISI

Bit	CC / ISI Status Flags	Symbol
Bit 0	TxEN Timeout	TxEN_timeout
Bit 1	CC Collision	CC_COL
Bit [2:7]	Reserved	
Bit 8	Interstar Wake flag	ISWAKE
Bit 9	Electrical Collision	EAS_COL
Bit 10	Interstar Collision	IS_COL
Bit 11	Interstar Timeout	IS_TIMEOUT
Bit [12:15]	Reserved	

Branch Status Flag Registers (addresses 0x02, 0x03, 0x04, 0x05, read-only).

Table 39. Status Register Bits for One Branch – example for Branch_x

Bit	BRANCH STATUS FLAGS to Host Controller Interface	Symbol
Bit 0	Bus Error (input / output comparison)	BUSERRx
Bit 1	Bus Activity flag (1 bus active / 0 bus idle)	BUSACTIVEx
Bit 2	Branch Collision flag	BRANCHx_COL
Bit 3	BP open line	BPx_OL
Bit 4	BP short circuit to V_{CC}	BPx_VCC
Bit 5	BP short circuit to GND	BPx_GND
Bit 6	BM open line	BMx_OL
Bit 7	BM short circuit to V_{CC}	BMx_VCC
Bit 8	BM short circuit to GND	BMx_GND
Bit 9	Short circuit between BP and BM	BPx_BMx
Bit 10	Remote Wake flag	RWAKEx
Bit 11	Branch Activity Timeout	BRANCHx_TO
Bit [12:14]	Branch State	BRANCHx_BSx
Bit 15	Logic Idle flag	BRANCHx_IDLE

APM Flag Command Register (address 0x06, read / write).

Table 40. APM Command Register Bit

Bit[0]	APM FLAGS from Host Controller Interface	Symbol
0	Reset APM flag command	RESET_APM
1	Set APM flag command	SET_APM

AS Host Command Register (address 0x07, read / write).

Table 41. AS Host Command Register Bit

Bit1:[0]	AS State from Host Controller Interface	Symbol
01	Go to AS_STANDBY	GOTOSTANDBY
10	Go to AS_NORMAL	GOTONORM
11	Go to AS_SLEEP	GOTOSLEEP
00	Reserved	

BRANCH Command Registers (addresses 0x08, 0x09, 0x0A and 0x0B, read / write).

Table 42. Host Command Register Bits

Bit [1:0]	BRx State from Host Controller Interface	Symbol
01	Go to BranchX_Disabled	BRx_DIS
10	Go to BranchX_Idle	BRx_IDLE
Others	Reserved	

NoiseTimeout Register (address 0x0E, read / write).

Table 43. NoiseTimeout Register

Bit	$T_{noise\_timeout}$	Symbol
Bit[0:7]	$T_{noise\_timeout}$ = (SPI value*16+ 1) * T_{step} (T_{step} is between 0.5µs and 2µs)	NOISE_LSB

Note: $T_{BranchNoiseTimeout} = T_{CCNoiseTimeout} = T_{noise\_timeout}$

$T_{ISNoiseTimeout} = 2*T_{noise\_timeout}$

Texit_fail Register (address 0x0F, read / write).

Table 44. Texit_fail Register

Bit	Texit Fail	Symbol
7	1: Exit fail silent when idle is detected on all elements. 0: Exit fail silent when idle is detected on the branch.	EXIT_COND
[6:0]	t_{exit_fail} = (SPI value+ 1) * T_{step} (T_{step} is between 12.5ns and 20ns)	EXIT_FAIL

Tears_shut Register (address 0x10, read / write).

Table 45. Tears_shut Register

Bit	Tears Shut	Symbol
[5:0]	t_{ears_shut} = SPI value*8*T_{step} (T_{step} is between 12.5ns and 20ns)	EARS_SHUT

POR Register (address 0x11, read / write).

Table 46. Reset Command Register Bit

Bit	Reset from Host Controller Interface	Symbol
0	Force reset (will be reset to 0 as soon as RESET is generated)	RESET

Tears_shut_faulty Register (address 0x12, read / write).

Table 47. Tears_shut_faulty Register

Bit	Tears Shut_f	Symbol
[5:0]	$t_{ears\_shu\_f}$ = SPI value*8*T_{step} (T_{step} is between 12.5ns and 20ns)	EARS_SHUT_F

Remote wake-up Disable Register (address 0x13, read / write).

Table 48. Disable Remote Wake-up Register

Bit	Disable Remote wake-up Receiver	Symbol
0	Disable Branch 1 remote wake-up receiver	WAKE0_MASK
1	Disable Branch 1 remote wake-up receiver	WAKE1_MASK
2	Disable Branch 1 remote wake-up receiver	WAKE2_MASK
3	Disable Branch 1 remote wake-up receiver	WAKE3_MASK

VCCUV Filter Register (address 0x14, read / write).

Table 49. VCCUV Filter Register

Bit	VCCUV Debouncing Time	Symbol
[5:0]	$t_{VCCUV\_DEBOUNCING}$ = (SPI value + 1) * T_{step} (T_{step} is between 0.5µs and 2µs)	VCC_UV_DEB

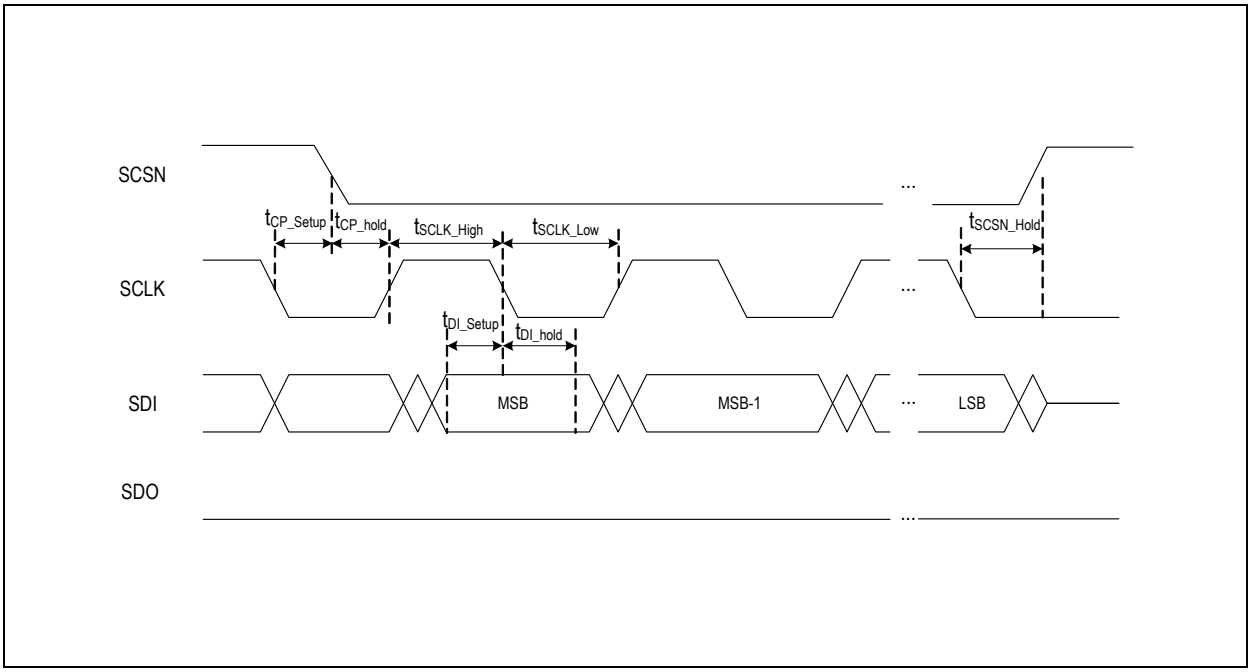
Note: This parameter is used only for VCCUV debouncing; $t_{UV\_DEBOUNCING}$ is not affected.

7.18 Timings

In the following paragraphs timing waveforms and parameters are exposed.

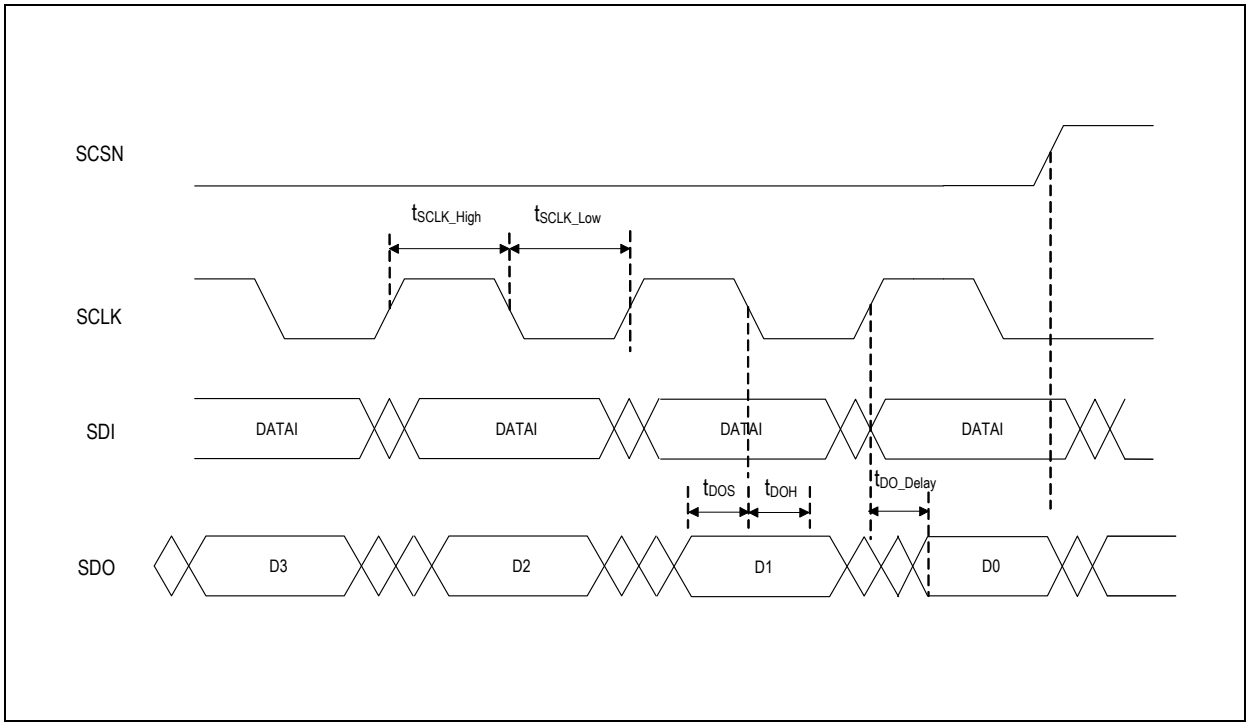
7.18.1 Write

Figure 12. Write Access Timing



7.18.2 Read

Figure 13. Read Access Timing



7.19 Inhibit Pins

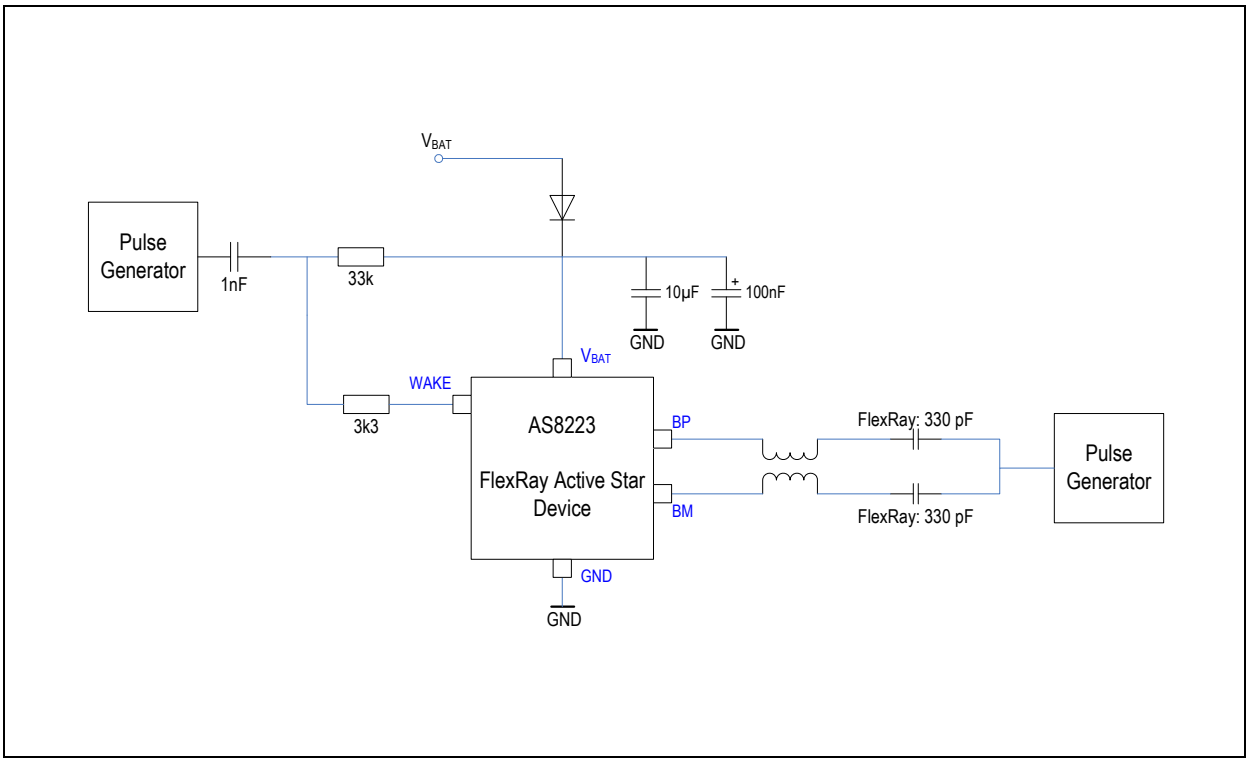
INH1 and INH2 are output pins of the AS8223. They can be used to control an external power supply. INH1 is floating if the device is in AS_SLEEP or AS_POWEROFF and it is driven to VBAT level if the Active Star is in one of the other modes. INH2 is floating if the device is in AS_SLEEP or AS_STANDBY or AS_POWEROFF and it is driven to VBAT level if the Active Star is in one of the other modes. A pull-down resistor should be used to force the floating outputs to ground.

Table 50. Function Table of Inhibit Pins

AS_State	INH1	INH2
AS_NORMAL	Driven to VBAT	Driven to VBAT
AS_STANDBY	Driven to VBAT	Floating
AS_SLEEP	Floating	Floating
AS_POWEROFF	Floating	Floating

7.20 Damage Tests (Class D)

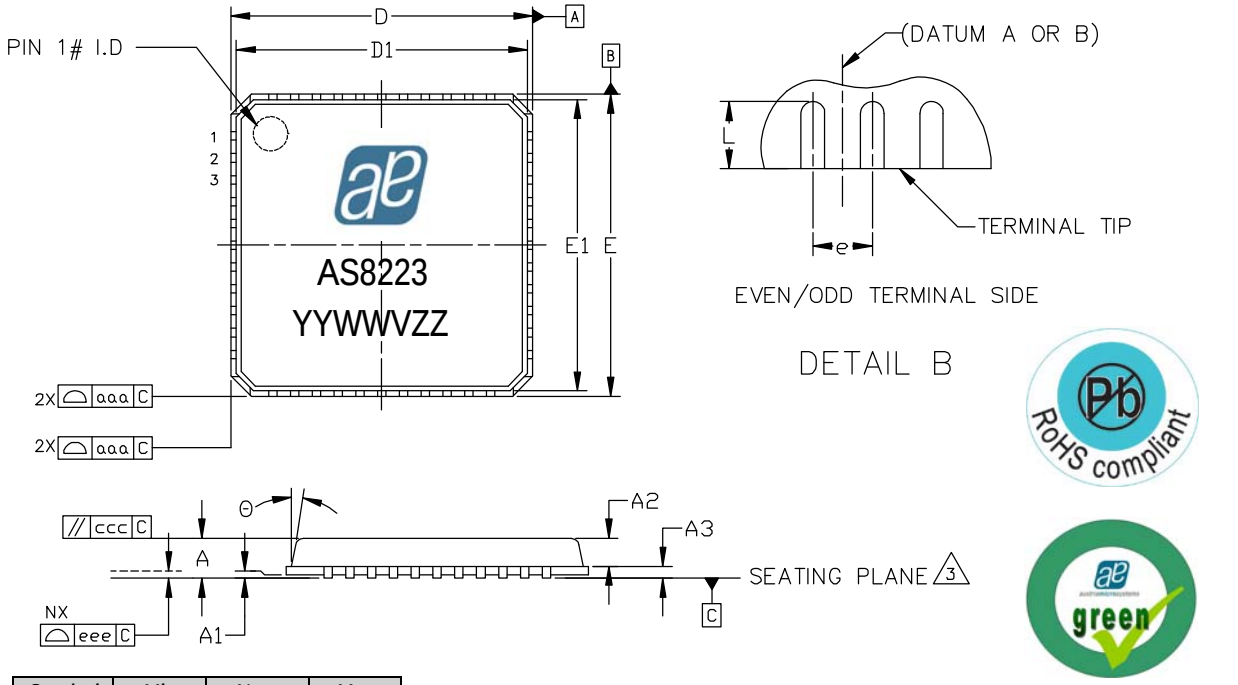
Figure 14. Damage Tests



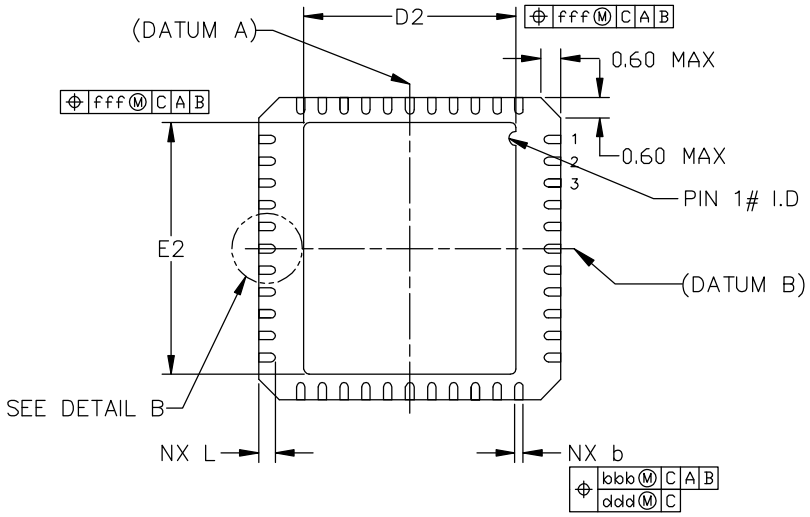
8 Package Drawings and Markings

The product is available in a 44-pin MLF (9x9) package.

Figure 15. Drawings and Dimensions



Symbol	Min	Nom	Max
A	0.80	0.90	1.00
A1	0	0.02	0.05
A2	-	0.65	1.00
A3		0.20 REF	
L	0.30	0.40	0.50
Θ	0°	-	14°
b	0.23	0.28	0.35
D		9.00 BSC	
E		9.00 BSC	
e		0.65 BSC	
D1		8.75 BSC	
E1		8.75 BSC	
D2	6.20	6.30	6.40
E2	7.40	7.50	7.60
aaa	-	0.15	-
bbb	-	0.10	-
ccc	-	0.10	-
ddd	-	0.05	-
eee	-	0.08	-
fff	-	0.10	-
N		44	



Notes:

1. Dimensions & tolerancing conform to *ASME Y14.5M-1994*.
2. All dimensions are in millimeters. Angles are in degrees.
3. Bilateral coplanarity zone applies to the exposed pad as well as the terminal.
4. Radius on terminal is optional.
5. N is the total number of terminals.

Marking: YYWWVZZ.

YY	WW	V	ZZ
Year (i.e. 10 for 2010)	Manufacturing Week	Assembly plant identifier	Assembly traceability code

Revision History

Revision	Date	Owner	Description
1.0	21 Apr, 2011	hgl	Initial version

Note: Typos may not be explicitly mentioned under revision history.

Related Documents

FlexRay Communication System Electrical Physical Layer Specification	V2.1 Rev B / November 2006
FlexRay Communication System Physical Layer EMC Measurement Specification	V3.0
Hardware requirements for LIN, CAN and FlexRay interfaces for Automotive applications	Rev. 1.1 / 02.12.2009

9 Ordering Information

Table 51. Ordering Information

Ordering Code	Marking	Description	Delivery Form	Package
AS8223-AMFP	AS8223	AS8223 FlexRay Active Star Device	Tape & Reel in Dry Pack	44-pin MLF (9x9)

Note: All products are RoHS compliant and austriamicrosystems green.
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