ACFL-6211U, ACFL-6212U

Bi-directional High Speed, Low Power Digital Optocoupler with R^{2}Coupler^{TM} Isolation in a Stretched 12-Pin Surface Mount Plastic Package

Data Sheet

Description

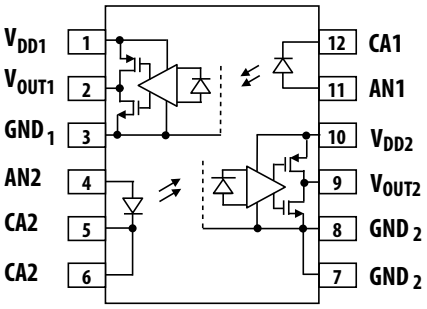
The ACFL-6211U and ACFL-6212U are dual channel, bi-directional, high speed digital CMOS optocouplers. The stretched SO-12 stretched package outline is designed to be compatible with standard surface mount processes and occupies the same land area as their single channel stretched SO8 package.

This digital optocoupler uses an insulating layer between the light emitting diode and an integrated photo detector to provide electrical insulation between input and output.

Each channel of the digital optocoupler has a CMOS detector IC with an integrated photodiode, a high speed trans-impedance amplifier, and a voltage comparator with an output driver. Each channel is also isolated from the other.

Avago R2Coupler technology provides reinforced insulation and reliability that delivers safe signal isolation critical in high temperature industrial applications.

Functional Diagram



Truth Table

LED	VO
ON	LOW
OFF	HIGH

NOTE The connection of a 1 µF bypass capacitor between pins 1 and 3 and pins 8 and 10 is recommended.

Features

- Wide temperature range: –40 °C to +125 °C
- 5 V CMOS compatibility
- 40 kV/µs common-mode rejection at V_{CM}=1000V (typ)
- Low propagation delay:
  - ACFL-6211U: 25 ns at I_F = 10 mA (typ)
  - ACFL-6212U: 60 ns at I_F = 4 mA (typ)
- Compact, auto-insertable stretched SO12 packages
- Worldwide safety approval:
  - UL 1577 recognized, 5kV_{RMS}/1 min.
  - CSA Approved
  - IEC/EN/DIN EN 60747-5-5

Applications

- CANBus and SPI communications interface
- High temperature digital/analog signal isolation
- Power transistor isolation

CAUTION It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD. The components featured in this data sheet are not to be used in military or aerospace applications or environments.

Pin Description

Pin No.	Pin Name	Description	Pin No.	Pin Name	Description
1	V_{DD1}	Primary Side Power Supply	7	GND2	Secondary Side Ground
2	V_{OUT1}	Output 1	8	GND2	Secondary Side Ground
3	GND1	Primary Side Ground	9	V_{OUT2}	Output 2
4	AN2	Anode 2	10	V_{DD2}	Secondary Side Power Supply
5	CA2	Cathode 2	11	AN1	Anode 1
6	CA2	Cathode 2	12	CA1	Cathode 1

Ordering Information

Part Number	Option (Ro HS Compliant)	Package	Surface Mount	Tape & Reel	UL 5000 Vrms/ 1 Minute Rating	IEC/EN/DIN EN 60747-5-5	Quantity
ACFL-6211U	-000E	Stretched SO-12	X		X		80 per tube
	-060E		X		X	X	80 per tube
	-500E		X	X	X		1000 per reel
	-560E		X	X	X	X	1000 per reel
ACFL-6212U	-000E	Stretched SO-12	X		X		80 per tube
	-060E		X		X	X	80 per tube
	-500E		X	X	X		1000 per reel
	-560E		X	X	X	X	1000 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

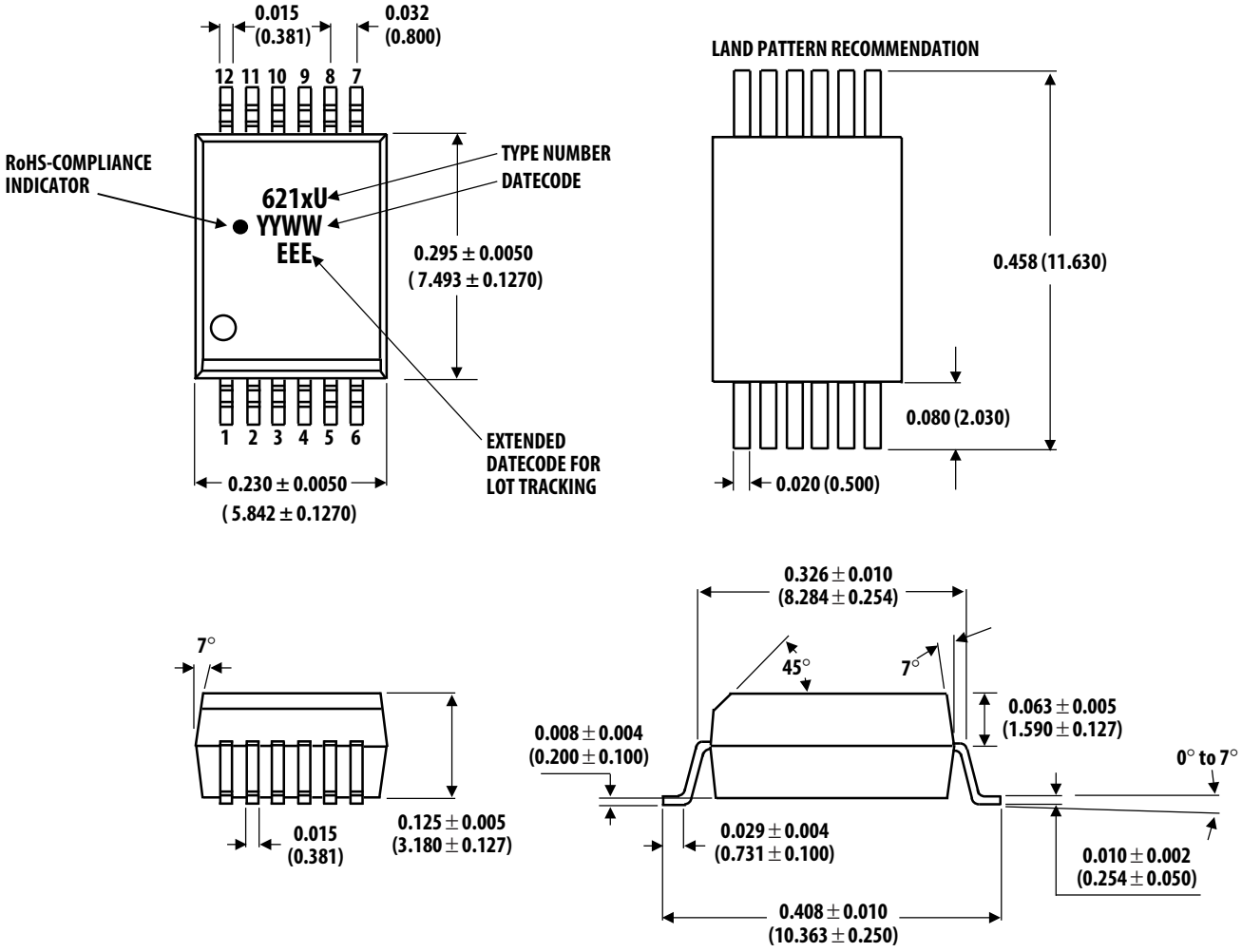
Example 1:

ACFL-6212U-560E to order product of SSO-12 Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Package Outline Drawing

12-Lead Surface Mount



Dimensions in inches (millimeters)

Lead coplanarity = 0.004 inches (0.1 mm)

Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision).

NOTE Non-halide flux should be used.

Regulatory Information

The ACFL-6211U and ACFL-6212U are approved by the following organizations:

UL	UL 1577, component recognition program up to VISO = 5kVRMS
CSA	Approved under CSA Component Acceptance Notice #5
IEC/EN/DIN EN 60747-5-5	Approved under IEC/EN/DIN EN 60747-5-5

Insulation and Safety Related Specifications

Parameter	Symbol	ACFL-6211U / ACFL-6212U	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	8.3	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	8.5	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group (DIN VDE0109)		IIIa		Material Group (DIN VDE 0109)

IEC/EN/DIN EN 60747-5-5 Insulation Related Characteristic (Option 060E and 560E)

Description	Symbol	Characteristic	Units
Installation classification per DIN VDE 0110/1.89, Table 1 for rated mains voltage ≤ 600 V rms for rated mains voltage < 1000 V rms		 I-III I-III	
Climatic Classification		40/125/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	1140	V_{PEAK}
Input to Output Test Voltage, Method b V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	2137	V_{PEAK}
Input to Output Test Voltage, Method a V_{IORM} x 1.6 = V_{PR}, Type and sample test, t_m = 10 sec, Partial Discharge < 5 pC	V_{PR}	1824	V_{PEAK}
Highest Allowable Overvoltage (Transient Overvoltage, t_{ini}= 60 sec)	V_{IOTM}	6000	V_{PEAK}
Safety Limiting Values (Maximum values allowed in the event of a failure) Case Temperature Input Current Output Power	 T_S $I_{S,INPUT}$ $P_{S,OUTPUT}$	 175 230 600	 °C mA mW
Insulation Resistance at T_S, VIO = 500 V	RS	10^9	Ω

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Condition
Storage Temperature	T_S	–55	+150	°C	
Ambient Operating Temperature	T_A	–40	+125	°C	
Junction Temperature	T_J		+150	°C	
Supply Voltages	V_{DD}	0	6.5	V	
Output Voltage	V_O	–0.5	V_{DD} +0.5	V	
Average Forward Input Current	I_F	-	20.0	mA	
Peak Transient Input Current (I_F at 1 µs pulse width, <10% duty cycle)	$I_{F(\ TRAN)}$		1 80	A mA	≤1 µs Pulse Width, 300pps ≤1 µs Pulse Width, <10% Duty Cycle
Reverse Input Voltage	V_r	-	5	V	
Input Power Dissipation	P_I		40	mW	
Average Output Current	Io		10	mA	
Output Power Dissipation	Po		30	mW	
Lead Solder Temperature	260 °C for 10 sec., 1.6 mm below seating plane				
Solder Reflow Temperature Profile	See Solder Reflow Temperature Profile section				

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Note
Supply Voltage	V_{DD}	3.0	5.5	V	
Operating Temperature	T_A	–40	125	°C	
Forward Input Current	$I_{F(ON)}$	4.0	15	mA	
Forward Off State Voltage	$V_{F(OFF)}$		0.8	V	
Input Threshold Current	I_{TH}		3.5	mA	

Electrical Specifications

Over recommended operating conditions. All typical specifications are at T_A=25 °C, V_{DD}= 5V.

Parameter	Symbol	Min.	Typ.	Max	Units	Test Conditions	Fig
LED Forward Voltage	V_F	1.45	1.5	1.75	V	I_F = 10 mA, T_A = 25 °C	
		1.25	1.5	1.85	V	I_F = 10 mA	
VF Temperature Coefficient			–1.5		mV/°C		
Input Threshold Current	I_{TH}		1.3	3.5	mA		2
Input Capacitance	C_{IN}		90		pF		
Input Reverse Breakdown Voltage	BV_R	5.0			V	I_R = 10 µA	
Logic High Output Voltage	V_{OH}	V_{DD} – 0.6			V	I_{OH} = –3.2 mA	4
Logic Low Output Voltage	V_{OL}			0.6	V	I_{OL} = 4 mA	3
Logic Low Output Supply Current (per channel)	I_{DDL}		0.9	1.5	mA		
Logic High Output Supply Current (per channel)	I_{DDH}		0.9	1.5	mA		

ACFL-6211U High Speed Mode Switching Specifications

Over recommended operating conditions: T_A = –40 °C to +125 °C, 4.5 V ≤ V_{DD} ≤. 5.5 V. All typical specifications are at T_A=25 °C, V_{DD} = 5V.

Parameter	Symbol	Min.	Typ,	Max.	Units	Test Conditions	Fig	Note
Propagation Delay Time to Logic Low Output	t_{PHL}		25	35	ns	V_{in} = 4.5V–5.5V, R_{in} = 390Ω ±5%, C_{in} = 100pF, CL = 15pF Output low threshold = 0.8V Output high threshold = 80% of Vdd	5, 9, 11	a, b, c
Propagation Delay Time to Logic High Output	t_{PLH}		25	35	ns			
Pulse Width Distortion	PWD		0	12	ns			
Propagation Delay Skew	t_{PSK}			15	ns			
Output Rise Time (10% – 90%)	t_R		10		ns			
Output Fall Time (90% –10%)	t_F		10		ns			
Common Mode Transient Immunity at Logic High Output	$\lvert CM_H \rvert$	15	25		kV/µs	V_{in} = 0V, R_{in} = 390Ω ± 5%, C_{in} = 100pF, V_{cm} = 1000V, T_A = 25°C		d
Common Mode Transient Immunity at Logic Low Output	$\lvert CM_L \rvert$	15	25		kV/µs	V_{in} = 4.5V –5.5V, R_{in} = 390Ω ±5%, C_{in} = 100pF, V_{cm} = 1000V, T_A = 25 °C		e

a. t_{PHL} propagation delay is measured from the 50% (V_{IN} or I_F) on the rising edge of the input pulse to the 0.8V of V_{DD} of the falling edge of the V_O signal. t_{PLH} propagation delay is measured from the 50% (V_{IN} or I_F) on the falling edge of the input pulse to the 80% level of the rising edge of the V_O signal.

b. PWD is defined as $|t_{PHL} - t_{PLH}|$.

c. t_{PSK} is equal to the magnitude of the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature within the recommended operating conditions.

d. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state.

e. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state.

ACFL-6212U Low Power Mode Switching Specifications

Over recommended operating conditions: T_A = –40 °C to +125 °C, 3.0 V ≤ V_{DD} ≤ 5.5 V. All typical specifications at 25 °C and V_{DD} = 5V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig	Note
Propagation Delay Time to Logic Low Output	t_{PHL}		60	100	ns	IF = 4mA, CL= 15pF	7, 12	a, b, c
Propagation Delay Time to Logic High Output	t_{PLH}		35	100	ns			
Pulse Width Distortion	PWD		25	50	ns			
Propagation Delay Skew	t_{PSK}			60	ns			
Output Rise Time (10% –90%)	t_R		10		ns			
Output Fall Time (90% - 10%)	t_F		10		ns			
Common Mode Transient Immunity at Logic High Output	$\lvert CM_H \rvert$	25	40		kV/µs	Using Avago LED Driving Circuit, V_{IN} = 0 V, R1 = 330 Ω ± 5%, R2 = 330 Ω ±5 %, V_{CM} = 1000 V, T_A = 25 °C		d
Common Mode Transient Immunity at Logic Low Output	$\lvert CM_L \rvert$	25	40		kV/µs	Using Avago LED Driving Circuit, V_{IN}=4.5 – 5.5V, R1 = 330 Ω ± 5%, R2 = 330 Ω ± 5%, V_{CM} = 1000V , T_A = 25 °C		e

a. t_{PHL} propagation delay is measured from the 50% (V_{IN} or I_F) on the rising edge of the input pulse to the 0.8V of V_{DD} of the falling edge of the V_O signal. t_{PLH} propagation delay is measured from the 50% (V_{IN} or I_F) on the falling edge of the input pulse to the 80% level of the rising edge of the V_O signal.

b. PWD is defined as $|t_{PHL} - t_{PLH}|$.

c. t_{PSK} is equal to the magnitude of the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature within the recommended operating conditions.

d. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state.

e. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state.

Package Characteristics

All Typical at T_A = 25 °C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Notes
Input-Output Momentary Withstand Voltage	V_{ISO}	5000			Vrms	RH ≤ 50%, t = 1 min, T_A = 25 °C	a, b
Input-Output Resistance	R_{I-O}		10^{14}		Ω	V_{I-O} = 500 V dc	a
Input-Output Capacitance	C_{I-O}		0.6		pF	f = 1 MHz, T_A = 25°C	a

a. Device considered a two terminal device: pins 1 to 6 shorted together, and pins 7 to 12 shorted together.

b. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage > 6000V_{RMS} for 1 second.

Figure 1 Typical Diode Input Forward Current Characteristic

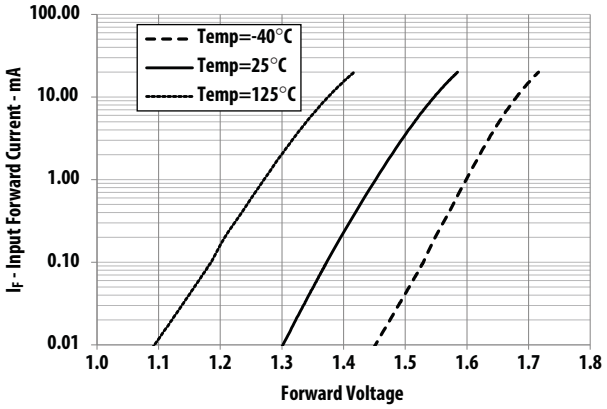


Figure 2 Typical Output Voltage vs Input Forward Current

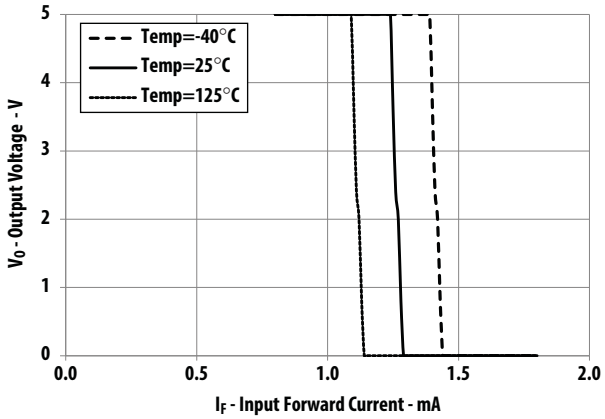


Figure 3 Typical Logic Low Output Voltage vs Logic Low Output Current

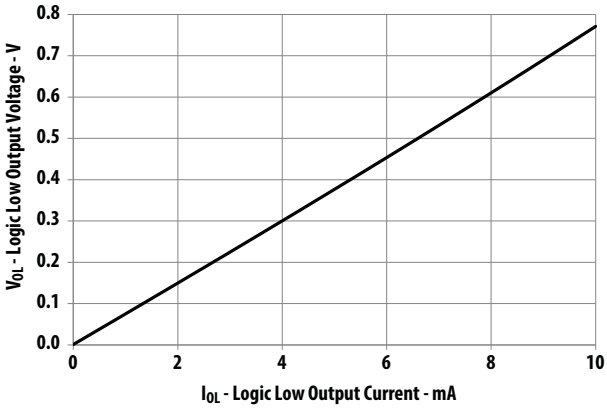


Figure 4 Typical Logic High Output Voltage vs Logic High Output Current

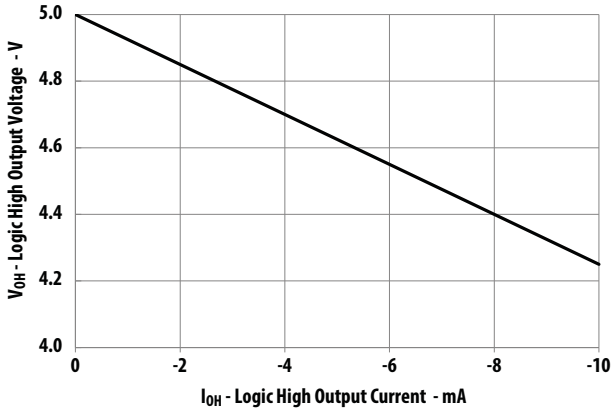


Figure 5 ACFL-6211U (High Speed) Typical Propagation Delay vs Temperature, V_{IN}=4.5V, R_{IN}=390Ω, C_{IN}=100pF

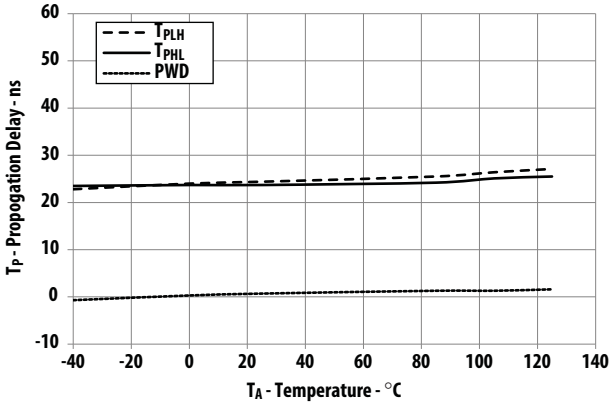


Figure 6 ACFL-6211U (High Speed) Typical Propagation Delay vs Input Forward Current, V_{IN}=4.5V, R_{IN}=390Ω, C_{IN}=100pF, T_A=25 °C

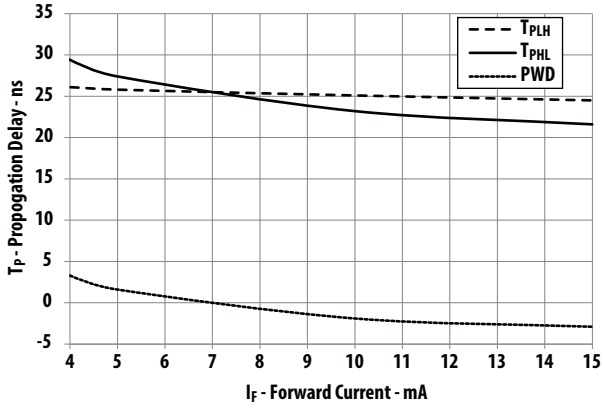


Figure 7 ACFL-6212U (5V) Typical Propagation Delay vs Temperature

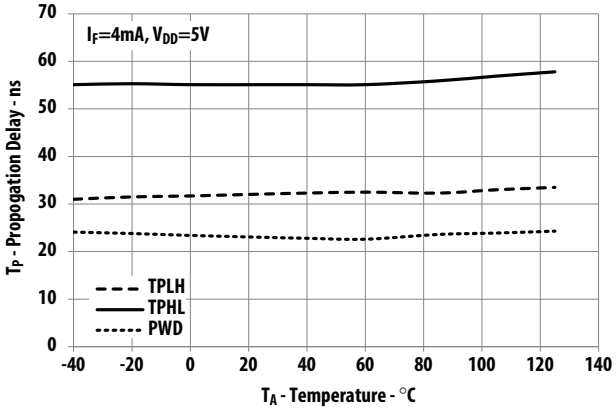


Figure 8 ACFL-6212U (5V) Typical Propagation Delay vs Input Forward Current

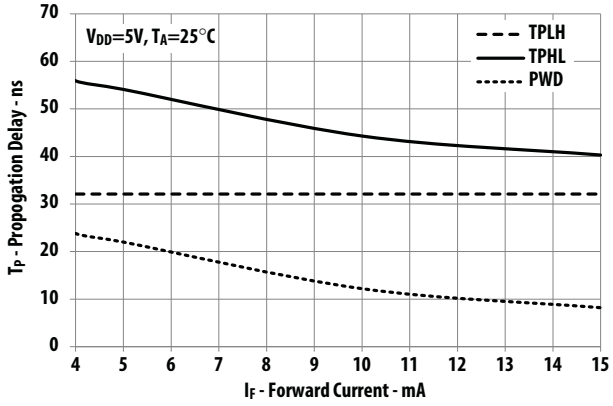


Figure 9 ACFL-6212U (3V) Typical Propagation Delay vs Temperature

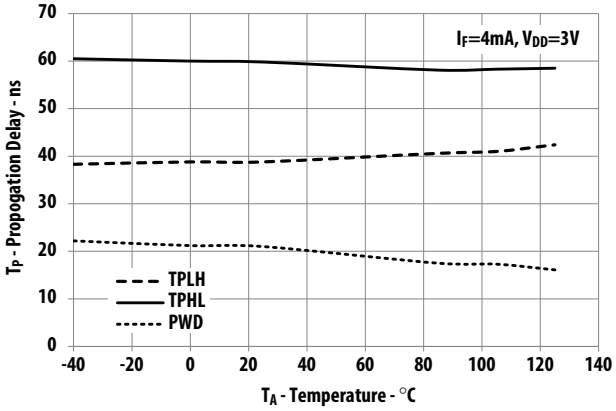


Figure 10 ACFL-6212U (3V) Typical Propagation Delay vs Input Forward Current

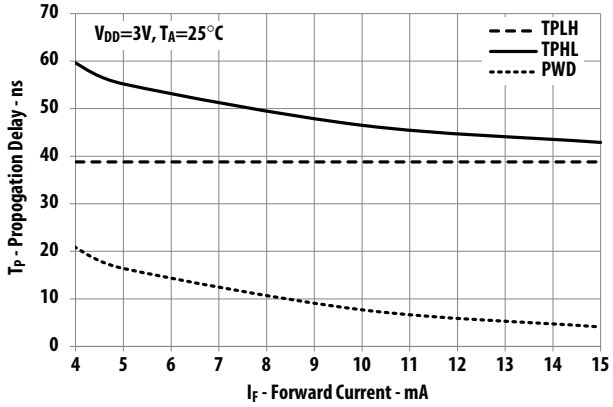
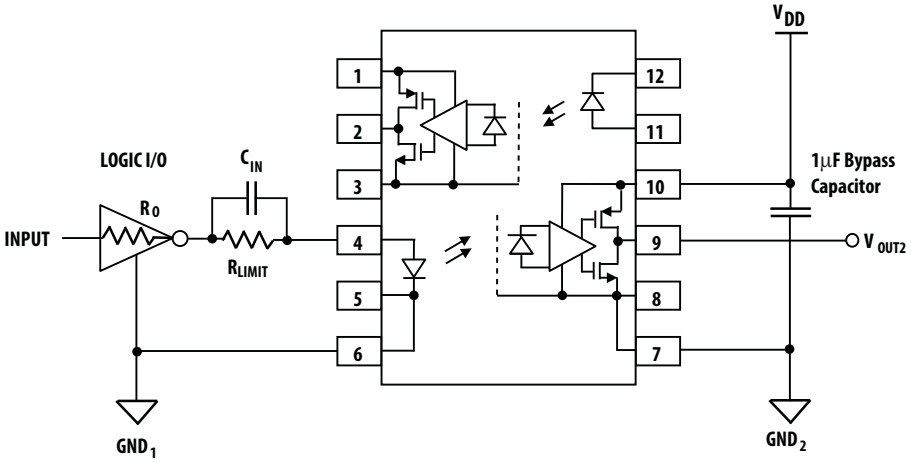


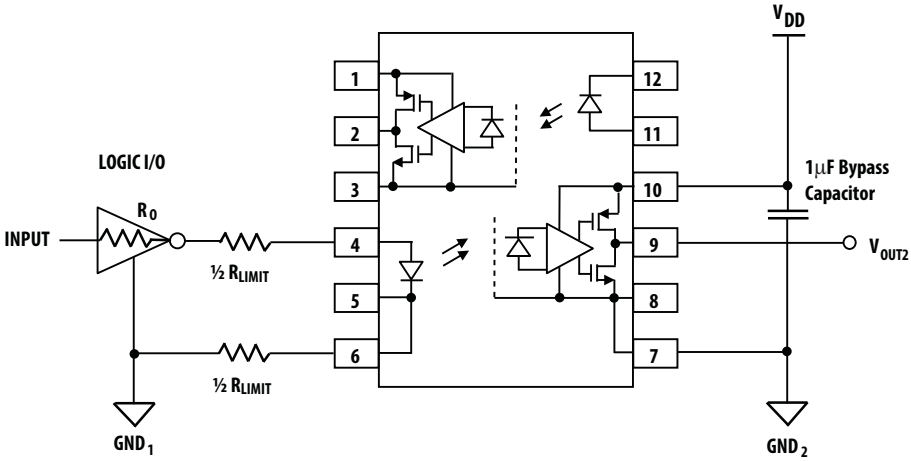
Figure 11 Recommended Application Circuit for ACFL-6211U High Speed Performance



TRUTH TABLE

INPUT	LED	OUTPUT
L	ON	L
H	OFF	H

Figure 12 Recommended Application Circuit for ACFL-6212U Low Power Performance



TRUTH TABLE

INPUT	LED	OUTPUT
L	ON	L
H	OFF	H

Test Circuits

Figure 13 Test Circuit for t_{PHL}, t_{PLH}, t_F, and t_R

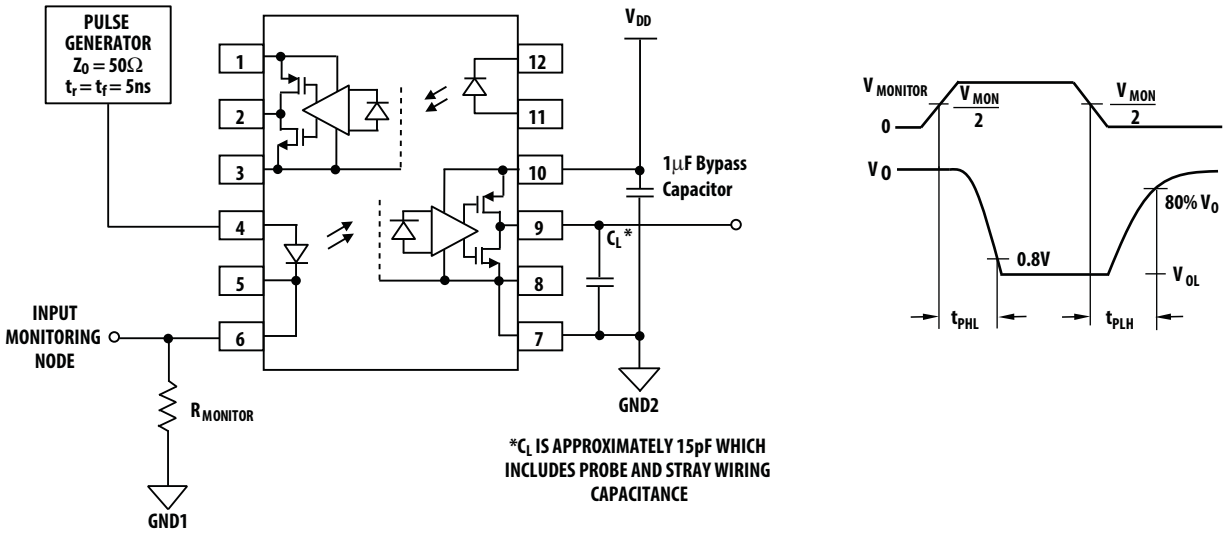
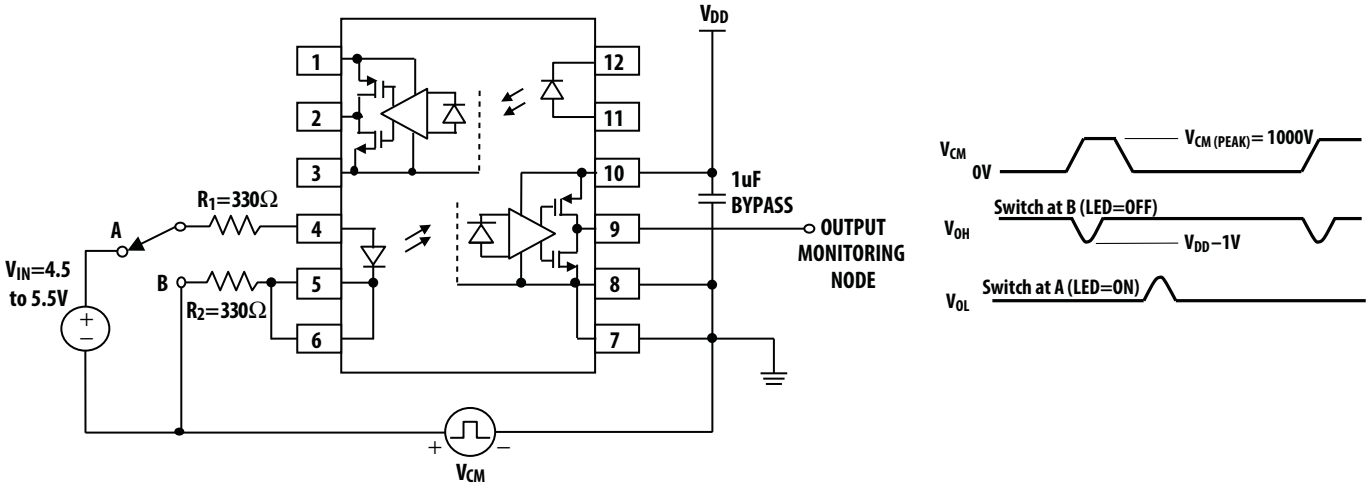


Figure 14 Test Circuit for Common Mode Transient Immunity



Thermal Resistance Measurement

The diagram of ACFL-6211U/6212U for measurement is shown in Figure 15. This is a multi-chip package with four heat sources, the effect of heating of one die due to the adjacent dice are considered by applying the theory of linear superposition. Here, one die is heated first and the temperatures of all the dice are recorded after thermal equilibrium is reached. Then, the 2nd die is heated and all the dice temperatures are recorded and so on until the 4th die is heated. With the known ambient temperature, the die junction temperature and power dissipation, the thermal resistance can be calculated. The thermal resistance calculation can be cast in matrix form. This yields a 4 by 4 matrix for our case of two heat sources.

$$\begin{vmatrix} R11 & R12 & R13 & R14 \\ R21 & R22 & R23 & R24 \\ R31 & R32 & R33 & R34 \\ R41 & R42 & R43 & R44 \end{vmatrix} \cdot \begin{vmatrix} P1 \\ P2 \\ P3 \\ P4 \end{vmatrix} = \begin{vmatrix} \Delta T1 \\ \Delta T2 \\ \Delta T3 \\ \Delta T4 \end{vmatrix}$$

R_{11}: Thermal Resistance of Die1 due to heating of Die1 (°C/W)
R_{12}: Thermal Resistance of Die1 due to heating of Die2 (°C/W)
R_{13}: Thermal Resistance of Die1 due to heating of Die3 (°C/W)
R_{14}: Thermal Resistance of Die1 due to heating of Die4 (°C/W)

R_{21}: Thermal Resistance of Die2 due to heating of Die1 (°C/W)
R_{22}: Thermal Resistance of Die2 due to heating of Die2 (°C/W)
R_{23}: Thermal Resistance of Die2 due to heating of Die3 (°C/W)
R_{24}: Thermal Resistance of Die2 due to heating of Die4 (°C/W)

R_{31}: Thermal Resistance of Die3 due to heating of Die1 (°C/W)
R_{32}: Thermal Resistance of Die3 due to heating of Die2 (°C/W)
R_{33}: Thermal Resistance of Die3 due to heating of Die3 (°C/W)
R_{34}: Thermal Resistance of Die3 due to heating of Die4 (°C/W)

R_{41}: Thermal Resistance of Die4 due to heating of Die1 (°C/W)
R_{42}: Thermal Resistance of Die4 due to heating of Die2 (°C/W)
R_{43}: Thermal Resistance of Die4 due to heating of Die3 (°C/W)
R_{44}: Thermal Resistance of Die4 due to heating of Die4 (°C/W)

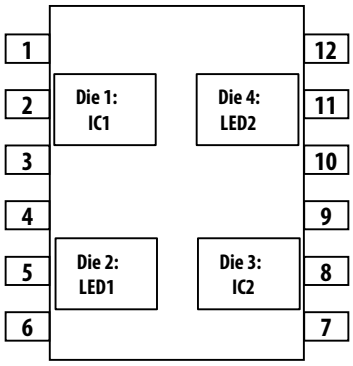
P_1: Power dissipation of Die1 (W)
P_2: Power dissipation of Die2 (W)
P_3: Power dissipation of Die3 (W)
P_4: Power dissipation of Die4 (W)

T_1: Junction temperature of Die1 due to heat from all dice (°C)
T_2: Junction temperature of Die2 due to heat from all dice (°C)
T_3: Junction temperature of Die3 due to heat from all dice (°C)
T_4: Junction temperature of Die4 due to heat from all dice (°C)

Ta: Ambient temperature.
ΔT_1: Temperature difference between Die1 junction and ambient (°C)
ΔT_2: Temperature deference between Die2 junction and ambient (°C)
ΔT_3: Temperature difference between Die3 junction and ambient (°C)
ΔT_4: Temperature deference between Die4 junction and ambient (°C)

$T_1 = (R_{11} \times P_1 + R_{12} \times P_2 + R_{13} \times P_3 + R_{14} \times P_4) + Ta$ -- (1)
$T_2 = (R_{21} \times P_1 + R_{22} \times P_2 + R_{23} \times P_3 + R24 \times P_4) + Ta$ -- (2)
$T_3 = (R_{31} \times P_1 + R_{32} \times P_2 + R_{33} \times P_3 + R34 \times P_4) + Ta$ -- (3)
$T_4 = (R_{41} \times P_1 + R_{42} \times P_2 + R_{43} \times P_3 + R_{44} \times P_4) + Ta$ -- (4)

Figure 15 Diagram of ACFL-6211U/6212U for Measurement



Measurement data on a low K (conductivity) board:

R_{11} = 181 °C/W
R_{21} = 103 °C/W
R_{31} = 82 °C/W
R_{41} = 110 °C/W
R_{12} = 91 °C/W
R_{22} = 232 °C/W
R_{32} = 97 °C/W
R_{42} = 86 °C/W
R_{13} = 85 °C/W
R_{23} = 109 °C/W
R_{33} = 180 °C/W
R_{43} = 101 °C/W
R_{14} = 112 °C/W
R_{24} = 91 °C/W
R_{34} = 91 °C/W
R_{44} = 277 °C/W

Measurement data on a high K (conductivity) board:

R_{11} = 117 °C/W
R_{21} = 37 °C/W
R_{31} = 35 °C/W
R_{41} = 47 °C/W
R_{12} = 42 °C/W
R_{22} = 161 °C/W
R_{32} = 53°C/W
R_{42} = 30 °C/W
R_{13} = 32 °C/W
R_{23} = 39 °C/W
R_{33} = 114 °C/W
R_{43} = 29 °C/W
R_{14} = 60 °C/W
R_{24} = 33 °C/W
R_{34} = 34 °C/W
R_{44} = 189 °C/W

For product information and a complete list of distributors, please go to our web site:
www.avagotech.com

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