Features

- **Hardware**
  - **Supports Programming for Atmel AT40K/AT40KAL and AT94KALSeries of SRAM-based Programmable System Level Integration (PSLI) Devices**
  - **Supports ISP (In-System Programming) for Atmel AT17 Series Configuration EEPROMs**
  - **Built-in Clock Source with GCLK/FCLK Jumper Settings**
  - **Supports Modular Docking Platform for the ATDH40D FPGA Daughter Boards**
  - **Runs Off Portable 9V DC Power Supply or External Power**
  - **Supports 5.0V or 3.3V Supply**
  - **Designed to Work with Atmel IDS 5.0 or Above**
  - **Downloading for AT40K/AT17 Devices Direct from PC Parallel Port**
  - **Can be Used to Support FPSLIC**
- **System Contents**
  - **ATDH2081**
    25-pin Parallel to 10-pin Header Adapter
  - **ATDH40Dxxx**
    Package-specific Daughterboard (Variable)
  - **ATDH40M**
    Programming Motherboard
  - **Standard Parallel Cable (PC Parallel Port DB25), 10-pin Header Cable, 9V DC/200 mA, 2.1 mm Center Positive Power Supply**

Description

The Atmel ATDH40M prototyping system allows designers to quickly and economically evaluate Atmel's family of AT40K/AT40KAL FPGA and AT94K Field Programmable System Level Integrated Circuit (FPSLIC™) devices and Atmel's AT17 FPGA configuration memory devices. The ATDH40M board connects to any x86 PC via parallel port through a 10-pin header cable to program the AT40K/AT40KAL FPGA/AT94K FPSLIC, or through a parallel port cable to program the AT17 FPGA Configuration EEPROMs. The motherboard interfaces with various daughter boards in order to program different package footprints (see Table 1).

Table 1. Daughter Board Support List

Part Number	Description
ATDH40D84	84-pin Plastic Lead Chip Carrier
ATDH40D100	100-pin Very Thin Quad Flat Pack
ATDH40D100R	100-pin Rectangular Quad Flat Pack
ATDH40D144	144-pin Thin Quad Flat Pack
ATDH40D160	160-pin Plastic Quad Flat Pack
ATDH40D208	208-pin Plastic Quad Flat Pack
ATDH40D240	240-pin Plastic Quad Flat Pack

Programmable System Level Integration Prototyping System

ATDH40M ATDH40DXXX

Rev. 1402B–06/01

The AT40K/AT40KAL FPGA devices are pin-compatible in a given package footprint across the family. See Table 2 for compatibility listings. The 208PQFP, for example, will support all AT40K family members.

FPSLIC is pin-compatible with AT40K/AT40KAL device families and is supported by the ATDH40M Prototyping System.

Table 2. Part and Package Availability Showing User I/O Counts

Package	Ordering Code	AT40K05/ AT40K05AL/ AT94K05AL	AT40K10 AT40K10AL AT94K10AL	AT40K20/ AT40K20AL	AT40K40/ AT40K40AL AT94K40AL
PC84	AJ	62	62	62	62
VQ100	AQ	78	78	-	-
RQ100	RQ	78	78	77	-
TQ144	BQ	114	114	114	114
PQ160	CQ	128	130	130	-
PQ208	DQ	128	161	161	161
BG225[1]	AG	-	192	192	192
PQ240	EQ	-	192	193	193
PQ304[1]	FQ	-	-	256	256
BG352[1]	BG	-	-	256	289
BG432[1]	CG	-	-	-	352

Note: 1. Daughtercard not available for ATDH40M.

2. Not all devices are available in all package options. Please check appropriate datasheet for a list of valid part/package combinations.

Programming Setup

Figure 1 on page 3 is the board layout of the ATDH40M motherboard. Figure 2 shows the typical daughter board. To connect the two boards together, the daughter board fits on top of the motherboard by aligning the two arrows together. The two boards will only fit one way.

Figure 1. Motherboard Layout – ATDH40M

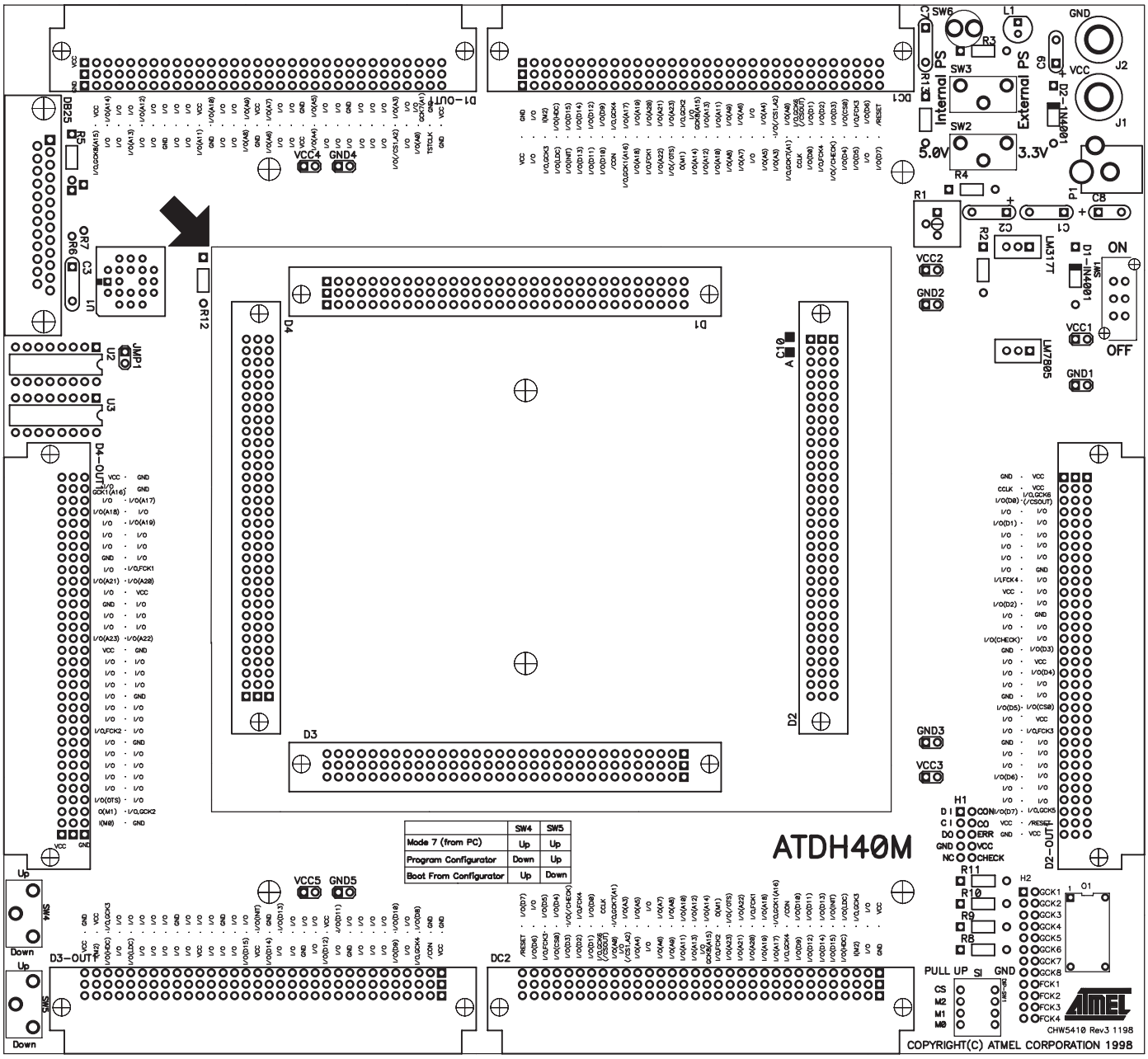
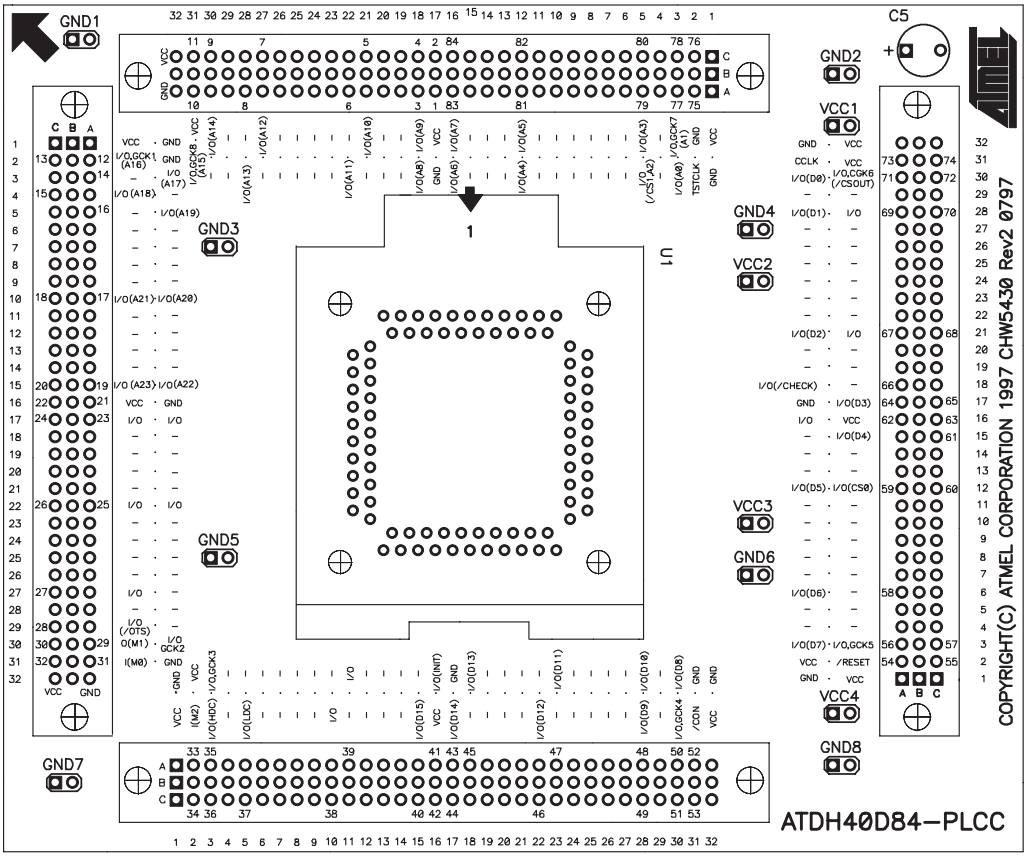


Figure 2. Daughter Board Layout Example – ATDH40D84



Power Configuration

Power for the motherboard can come from two sources. It can be supplied by either the jack inputs J1 and J2, or by a 9V power input P1. The source that will drive the motherboard is determined by switch SW3. Power supplied by the jacks uses the *external* setting. Power supplied by the 9V source uses the *internal* setting. Voltage on the motherboard for the latter setting is regulated by switch SW2. LV parts use the 3.3V setting while the rest use the 5.0V setting. The LED L1 will light up only when power is correctly supplied to VCC. Table 3 lists the possible configurations. AT40KAL and AT94KAL devices must use 3.5V power setting.

Table 3. Motherboard Power Distribution

SW1	SW2	SW3	Voltage
Off	X	X	0.0V (no power)
On	X	External	Variable
On	3.3V	Internal	3.3V for AT40KAL/AT94KAL
On	5.0V	Internal	5.0V for AT40K

Program/Boot Settings

Switches SW4 and SW5 determine the program and boot settings for the ATDH40M. They are located on the bottom left corner. Table 4 lists the switch combinations and their effects. SW4 controls the $\overline{\text{SEREN}}$ signal line of the motherboard to the 2:1 multiplexer (device U3) and the AT17 (device U1). SW% connects signal D0 from the PSLI device to either the AT17 configuration memory device only (down) or to the PC interface (up).

Table 4. Programming Modes

SW4	SW5	Effect
Up	Up	Program in Slave Serial from PC
Down	Up	Program AT17 Configuration Memory
Up	Down	Program in Master Serial from AT17

Programming the AT40K FPGA Device

When SW4 and SW5 are set to up, the PSLI device can be programmed by the PC parallel interface. The ATDH40M interfaces with the PC through the 10-pin header socket H1 located on the bottom right corner. Programming the FPGA is *not* possible by using the parallel port interface on the motherboard. Located below the header H1 are the mode-select dip-switches DIP-SW1. These control the mode settings for the PSLI device (switches M0, (M1), M2). The modes directly supported by the motherboard are only Slave Serial and Master Serial. Programming the AT40K FPGA from the PC can be achieved from the IDS desktop or by using the software *downld40.exe*. Both tools accept ASCII bitstream files generated by the IDS software (.BST).

Programming the AT17 Configuration Memory Device

When SW4 is set to down and SW5 is set to up, the AT17 FPGA configuration memory can be programmed by the parallel port interface located on the top left corner. Programming the AT17 FPGA Configuration EEPROM is *not* possible by using the 10-pin header H1. Programming the AT17 FPGA Configuration EEPROM from the PC can be achieved from the IDS desktop or by using the Configurator Programming System (CPS) software supplied by the IDS software.This software accepts the ASCII bitstream files (.BST) generated by IDS.

Programming the PSLI Device Using the AT17 Configuration Memory

When SW4 is set to up and SW5 is set to down, the AT17 Configurator can program the FPGA in Master Serial. To ensure reliable system power-up, set jumper JMP1 (located below the Configurator socket). The Configurator must be programmed prior to this setup.

Troubleshooting

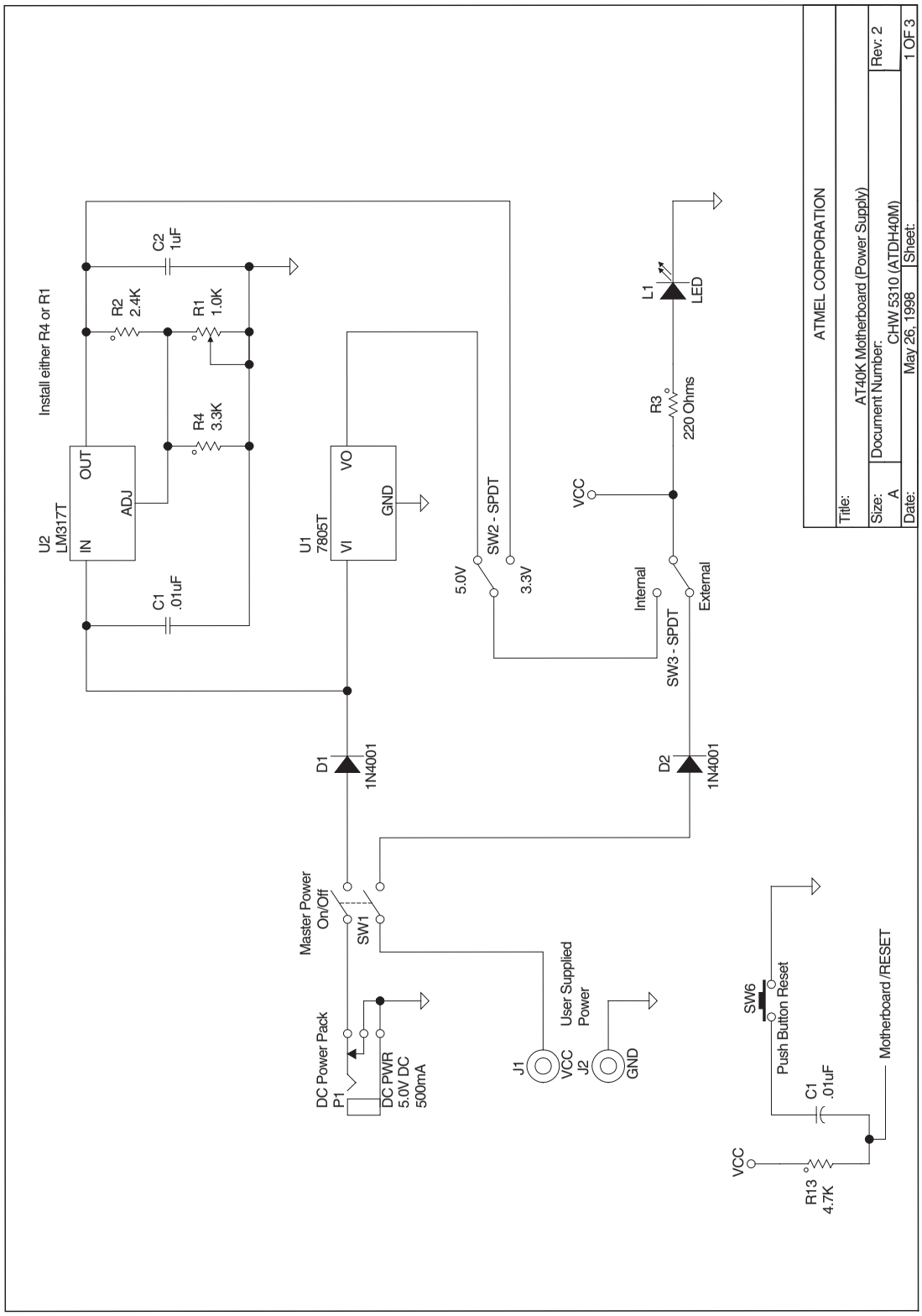
1. Check that the motherboard is connected to the PC either through the parallel port or through the 10-pin header.
2. Check that the motherboard has power (SW1) and the power configuration switches SW2 and SW3 are correct.
3. Make sure programming configuration switches SW4 and SW5 are correct.
4. Verify that the daughter card is inserted correctly and that it receives power.
5. Verify that the PSLI device and/or the PSLI. Configurator are placed in their sockets correctly.
6. Set the mode switches before downloading to the PSLI Device.
7. Set the GCLK/FCLK jumpers before verifying PSLI logic.

Technical Support

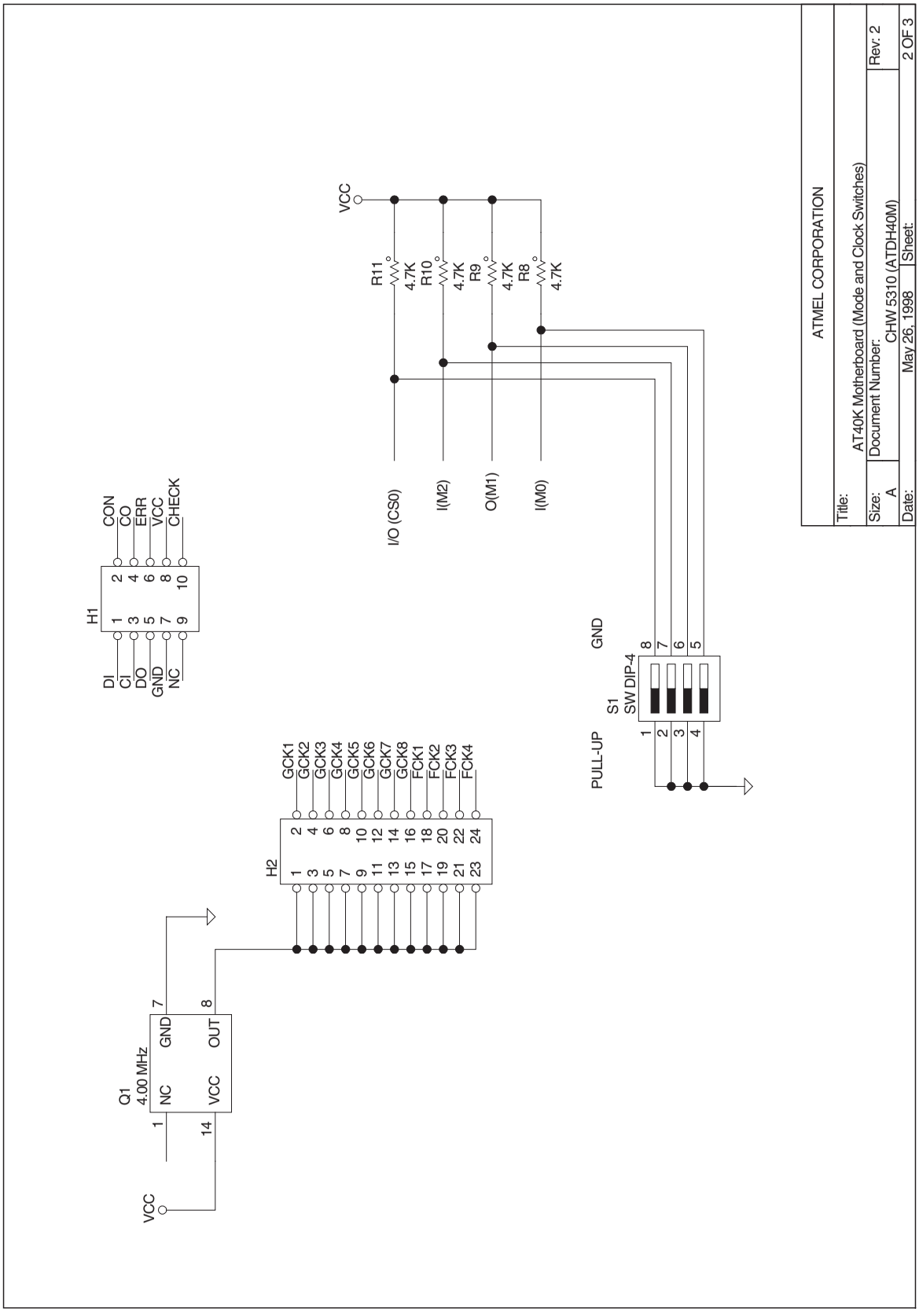
- Check each of the items listed in the troubleshooting section.
- Contact your local Atmel Representative or Distributor who provided the PSLI board for technical support.
- Contact your local Atmel FAE (available at most sales offices).
- Contact the Atmel PSLI technical support hotline at (408) 436-4119. Hours are Monday-Friday 9:00 a.m. – 6:00 p.m. PST.
- E-mail Atmel PSLI technical support at fpga@atmel.com.
- Fax inquiries to “FPGA Tech Support” at (408) 487-2637

ATDH40M Functional Schematics

Power Supply

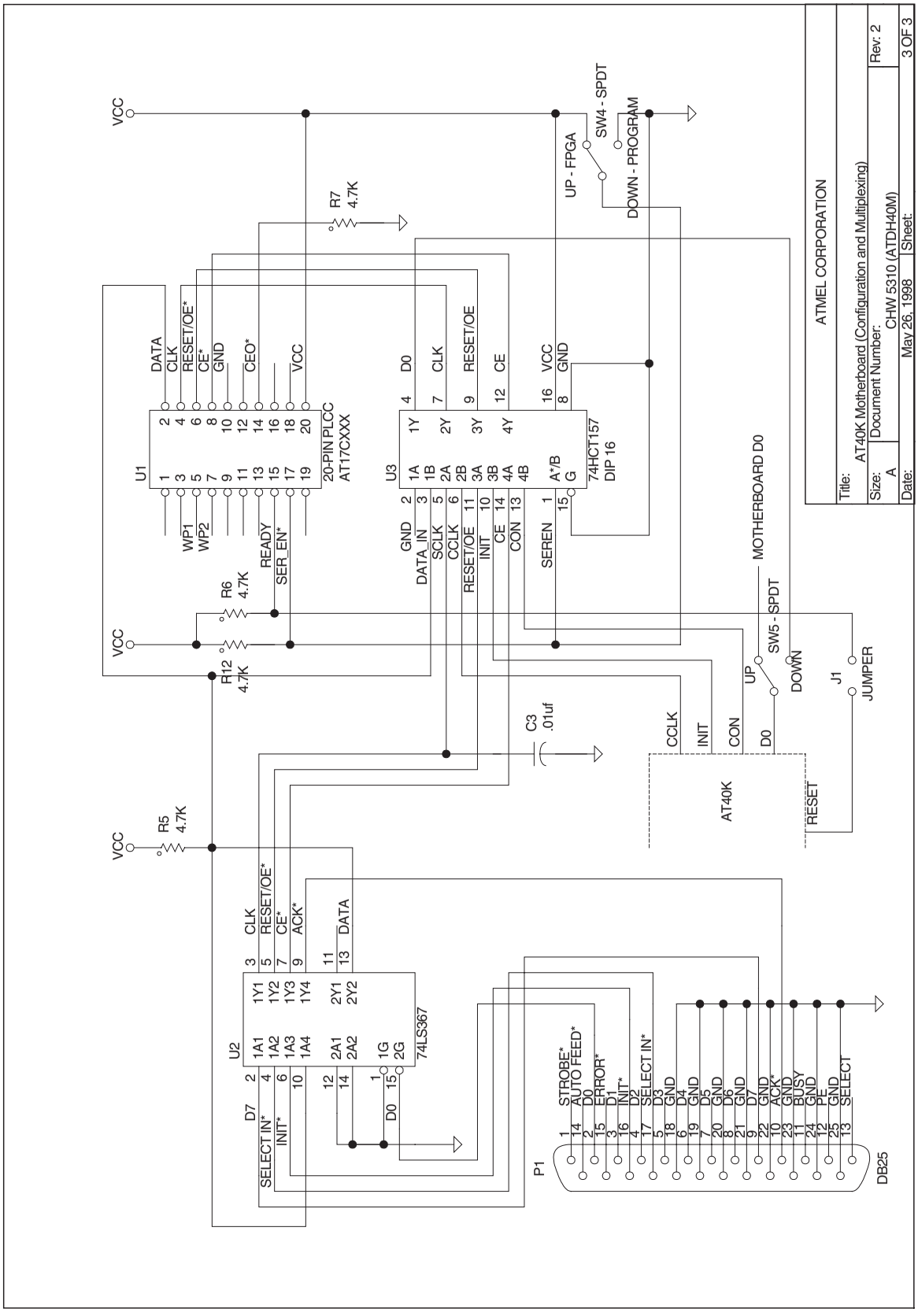


Mode and Clock Switches



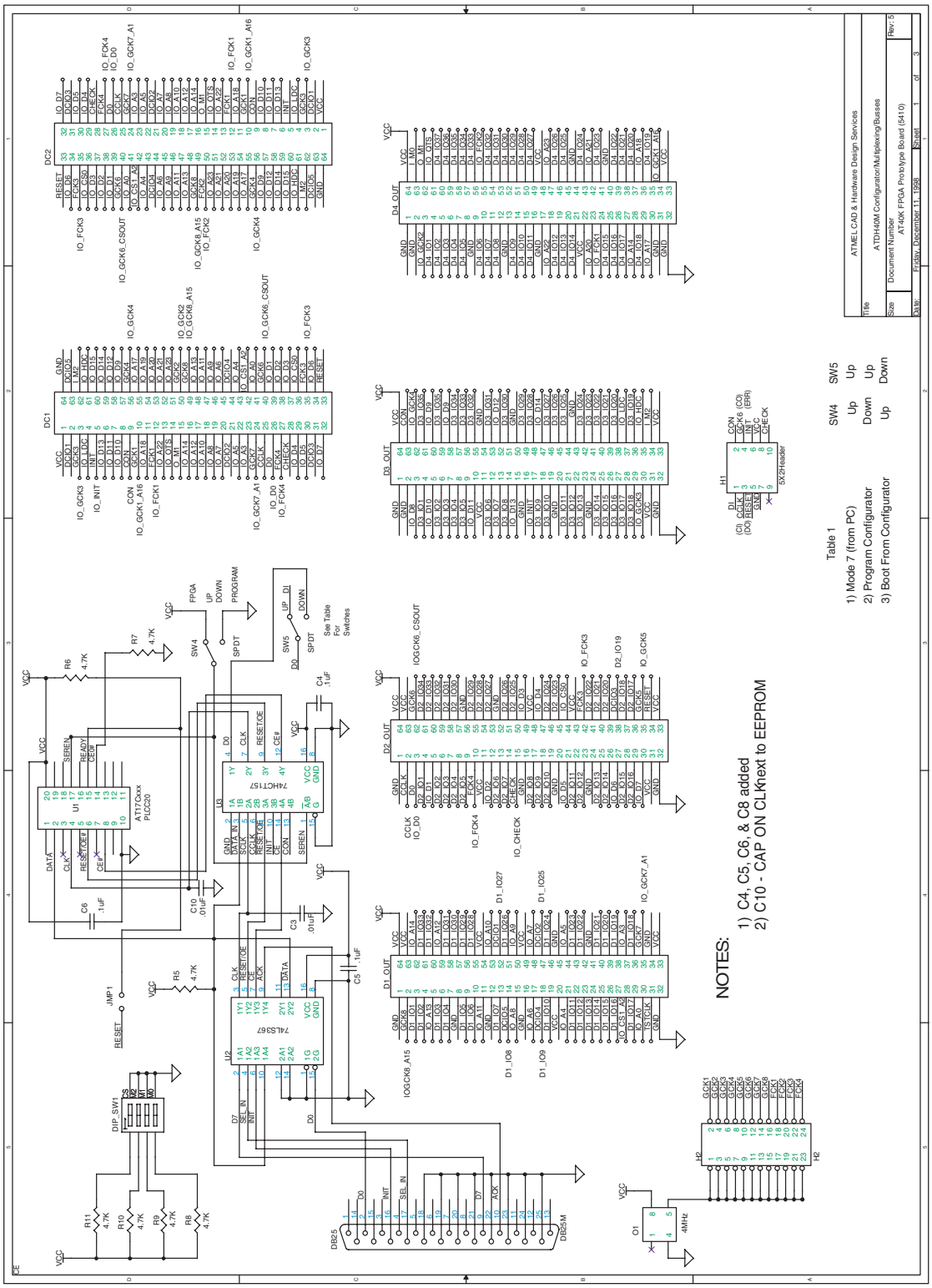
Note: The 12-pin header (H2) is used to connect the clocks with the jumpers. The DIP switch (S1) is used to set the different modes.

Configuration and Multiplexing

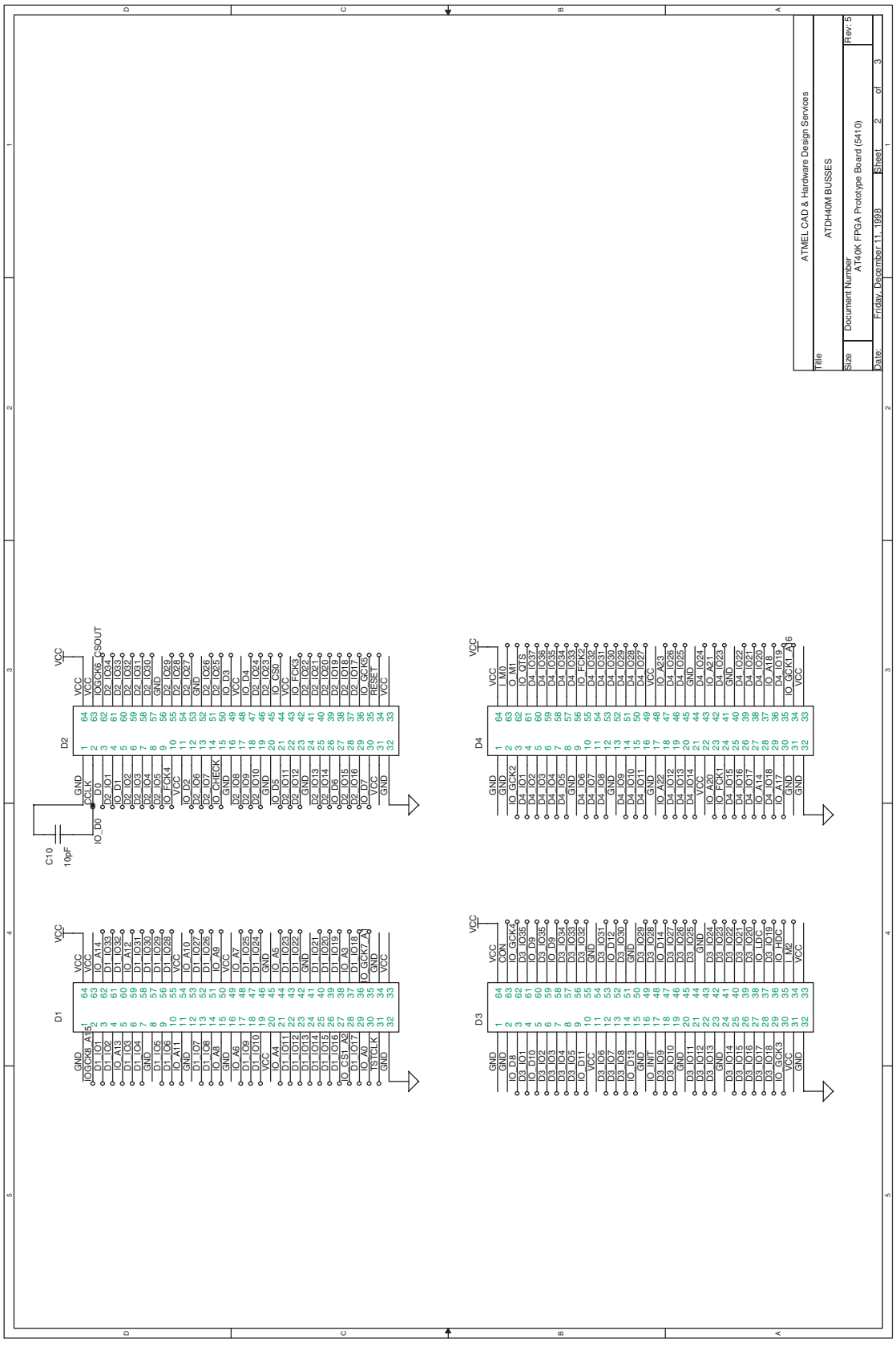


ATDH40M Layout Schematics

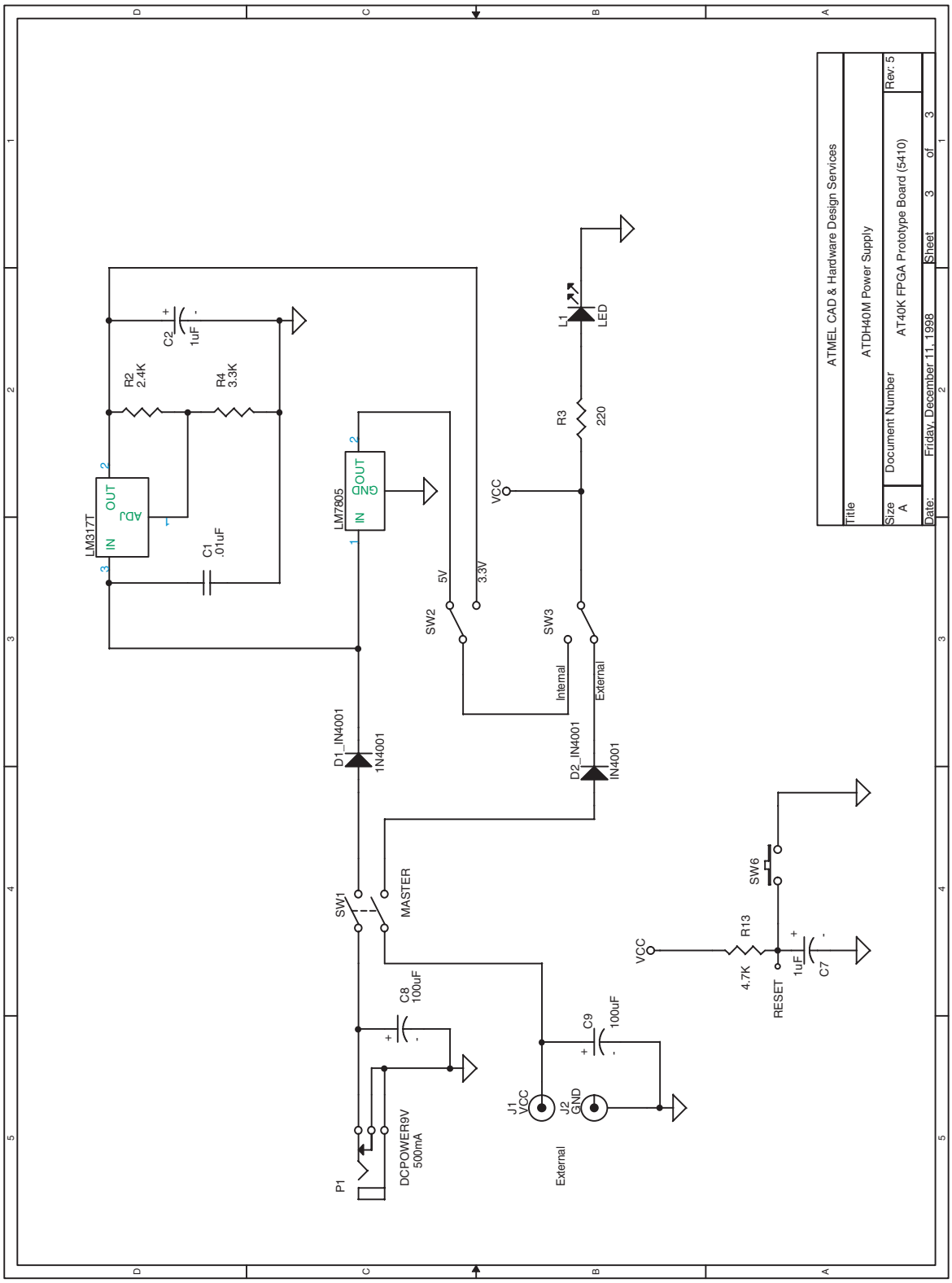
Configurator/Multiplexing/Buses



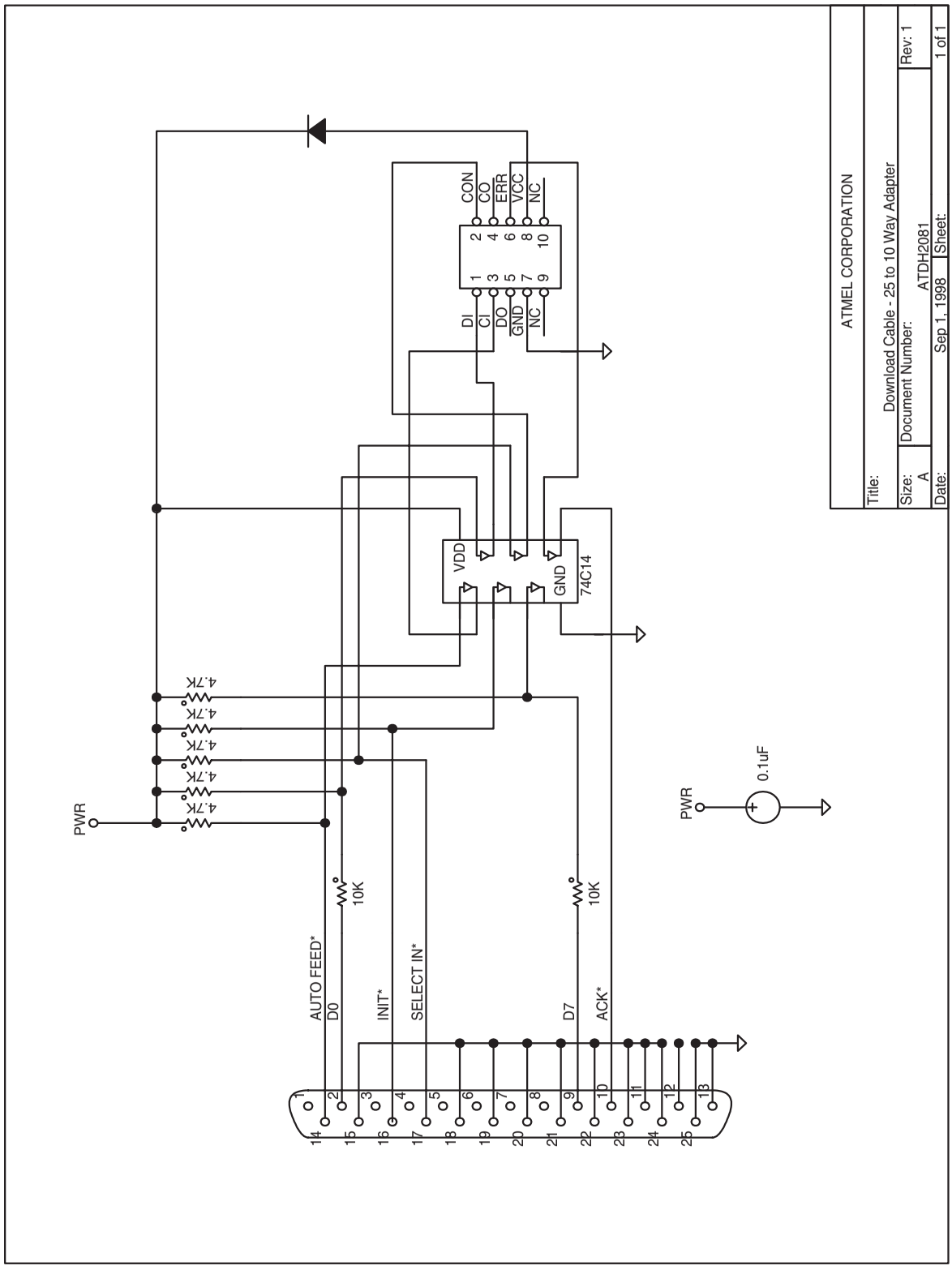
Buses


ATMEL CAD & Hardware Design Services
Title
ATDH40M BUSSES
Size
Document Number
AT40K FPGA Prototype Board (5410)
Rev: 5
Date: Friday, December 11, 1998
Sheet 2 of 3
D1
D2
D3
D4
C10
10pF
IO_D0
VCC
GND

Power Supply



ATDH2081 Download Cable (25- to 10-Way Adapter)



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