Introduction

This application note will help developers quickly implement proof-of-concept designs using the **KX021, KX022**, and **KX023** tri-axis accelerometers. Please refer to the corresponding Product Specifications document for additional implementation guidelines. Kionix strives to ensure that our accelerometers will meet design expectations by default, but it is not possible to provide default settings to work in every environment. Depending on the intended application, it is very likely that some customization will be required in order to optimize performance. The information provided here will help the developer get the most out of this tri-axis accelerometers.

Circuit Schematic

This section shows recommended wiring for this family of accelerometers, based on proven operation of the part. Specific applications may require modifications from these recommendations. Please refer to the corresponding Product Specifications documents for all pin descriptions.

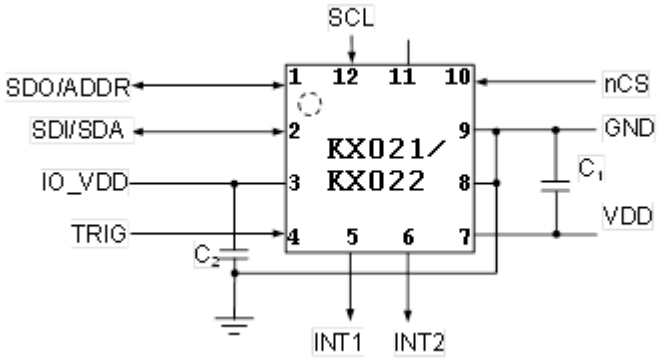

Figure 1: KX021/KX022 Application Schematic

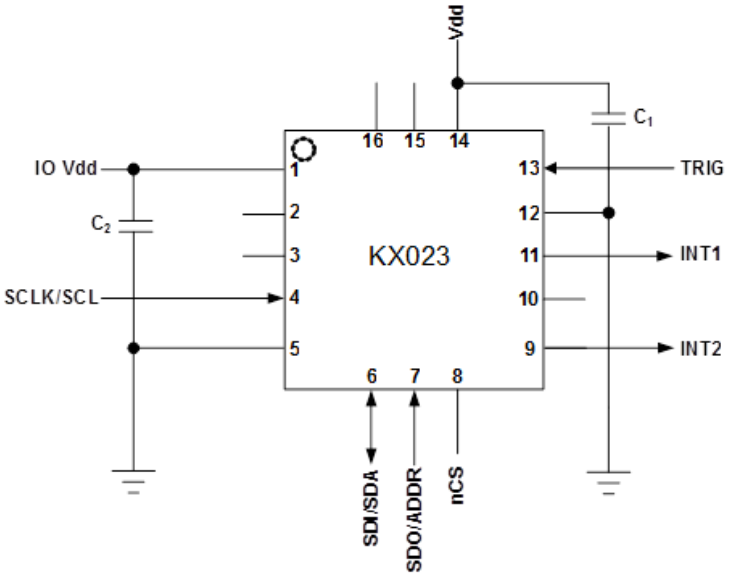

Figure 2: KX023 Application Schematic

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Quick Start Implementation

Here we present several basic ways to initialize the part. These can vary based on desired operation, but generally the initial operations a developer wants to do are: 1) read back acceleration data asynchronously, 2) read back acceleration data when next data is ready via interrupt (synchronous data reading), 3) use of the sample buffer, 4) use the Wake Up function, 5) activate the tilt position function, and 6) activate the tap/double-tap function. These cursory solutions are provided as a means for configuring the part to a known operational state. Note that these conditions just provide a starting point, and the values may vary as developers refine their application requirements.

1. Asynchronous Read Back Acceleration Data (Setting G-Range and ODR)

- Write 0x40 to Control Register 1 (CNTL1) to set the accelerometer in stand-by mode, to set the performance mode to High Resolution (full power) and G-range to ±2g.

Register Name	Address	Value
CNTL1	0x18	0x40

- Write 0x02 to Data Control Register (ODCNTL) to set the Output Data Rate (ODR) of the accelerometer to 50 Hz. (Note: This is also the default value.)

Register Name	Address	Value
ODCNTL	0x1B	0x02

- Write 0xC0 to Control Register 1 (CNTL1) to set the accelerometer into operating mode (PC1 = 1)

Register Name	Address	Value
CNTL1	0x18	0xC0

- Acceleration data can now be read from the XOUT_L, XOUT_H, YOUT_L, YOUT_H, ZOUT_L, and ZOUT_H registers in 2's complement format.

  Notes:
  a. All 6 bytes of output data can be read in one serial read transaction using the register auto-increment feature (see Product Specification for details)
  b. All sample data read operations must be completed within 1/ODR cycle. More specifically, the serial read operation must be completed before the next sample is ready. This is because the write to output data registers is blocked when these registers are being read. If old sample data read transaction is not completed in time, the new sample data won't be written to the output data register. Consider using Synchronous Data read to avoid potential timing issues (see ***Synchronous Hardware Interrupt Read Back Acceleration Data*** section of this application note for details).

2. Synchronous Hardware Interrupt Read Back Acceleration Data

- Write 0x60 to Control Register 1 (CNTL1) to set the accelerometer in stand-by mode, to set the performance mode to High Resolution (full power), G-range to ±2g, and enable the availability of new data as an interrupt.

Register Name	Address	Value
0x18	0x18	0x60

- Write 0x38 to Interrupt Control Register (INC1) to enable physical interrupt pin INT1, to set the polarity of the physical interrupt to active high and to transmit interrupt pulses with a period of 0.03 ms to 0.05 ms in pin (5).

Register Name	Address	Value
INC1	0x1C	0x38

- Write 0x10 to Interrupt Control Register 4 (INC4) to set the Data Ready interrupt to be reported on physical interrupt pin INT1.

Register Name	Address	Value
INC4	0x1F	0x10

- Write 0x02 to Data Control Register (ODCNTL) to set the Output Data Rate (ODR) of the accelerometer to 50 Hz. (Note: This is also the default value.)

Register Name	Address	Value
ODCNTL	0x1B	0x02

- Write 0xE0 to Control Register 1 (CNTL1) to set the accelerometer into operating mode (PC1 = 1)

Register Name	Address	Value
CNTL1	0x18	0xE0

- Monitor the physical interrupt INT1 of the accelerometer. The rising edge of the pulse on INT1 signal should be used to determine when new sample data is ready. Also, the interrupt would be reflected in bit 4 of INS2 register until cleared by reading the data from the XOUT_L, XOUT_H, YOUT_L, YOUT_H, ZOUT_L, and ZOUT_H registers in 2's complement format.

  Notes:
  c. All 6 bytes of output data can be read in one serial read transaction using the register auto-increment feature (see Product Specification for details)
  d. All sample data read operations must be completed within 1/ODR cycle. More specifically, the serial read operation must be completed before the next sample is ready. This is because the write to output data registers is blocked when these registers are being read. If old sample data read transaction is not completed in time, the new sample data will not be written to the output data register, and no interrupt on Data Ready will be issued (either on a physical pin or in the interrupt status register).

3. Sample Buffer-Full Interrupt via physical hardware interrupt

- Write 0x00 to Control Register 1 (CNTL1) to set the accelerometer in stand-by mode, to set the performance mode to Low Current mode, and G-range to ±2g.

Register Name	Address	Value
CNTL1	0x18	0x00

- Write 0x38 to Interrupt Control Register (INC1) to enable physical interrupt pin INT1, to set the polarity of the physical interrupt to active high and to transmit interrupt pulses with a period of 0.03 ms to 0.05 ms in pin (5).

Register Name	Address	Value
INC1	0x1C	0x38

- Write 0x40 to Interrupt Control Register 4 (INC4) to set the Buffer Full interrupt to be reported on physical interrupt pin INT1.

Register Name	Address	Value
INC4	0x1F	0x40

- Write 0x02 to Data Control Register (ODCNTL) to set the Output Data Rate (ODR) of the accelerometer to 50 Hz. (Note: This is also the default value.)

Register Name	Address	Value
ODCNTL	0x1B	0x02

- Write 0xA0 to Buffer Control Register 2 (BUF_CTL2) to activate the sample buffer, to set the resolution of the acceleration data samples collected to 8 bits, to enable report of the interrupt status in INS2, and set the operating mode of the sample buffer to FIFO.

Register Name	Address	Value
BUF_CNTL2	0x3B	0xA0

- Write 0x80 to Control Register 1 (CNTL1) to set the accelerometer into operating mode (PC1 = 1)

Register Name	Address	Value
CNTL1	0x18	0x80

- Once Buffer-Full Interrupt is issued on INT1 pin, acceleration data can then be read from the Buffer Read (BUF_READ) register at address 0x3F in 2's complement format. Since the resolution of the samples data was set to 8-bit, only the most significant 8 bits of each sample will be stored in the buffer, and recorded in the following order: X_HIGH, Y_HIGH, Z_HIGH with the oldest data point read first as it is a FIFO buffer. The full buffer contains 252 X, Y, Z elements, which corresponds to 84 unique acceleration data samples.

Buffer reading tips:

a) The acceleration data can be read from a buffer using multiple-byte read as shown in the Figure 3 below. The register auto-increment feature is disabled when data is read from the Buffer Read register.
b) If data is read using single-byte read, it should be read in increments of 3 bytes in 8-bit resolution mode and 6 bytes in 16-bit resolution mode.
c) It is very important to follow proper I2C Write-Read sequence as specified in the product specifications. More specifically, the Master should avoid sending the Stop (P) bit at the end of the I2C Write command, and should issue a Repeat Start bit (Sr) at the start of the I2C Read command as show in the Figure 3. Failure of following this sequence may result in reading the same value from the Read Buffer.

Master	S	SAD + W		RA		Sr	SAD + R			ACK		NACK	P
Slave			ACK		ACK			ACK	DATA		DATA		

Term	Definition
S	Start Condition
Sr	Repeated Start Condition
SAD	Slave Address
W	Write Bit
R	Read Bit
ACK	Acknowledge
NACK	Not Acknowledge
RA	Register Address
Data	Transmitted/Received Data
P	Stop Condition

Figure 3: Proper I2C Sequence to Receive Data from the Slave

4. Wake-Up Function via latched physical hardware interrupt

- Write 0x42 to Control Register 1 (CNTL1) to set the accelerometer in stand-by mode, to set the performance mode to High Resolution (full power), G-range to ±2g, and enable the Wake Up (motion detect) function.

Register Name	Address	Value
CNTL1	0x18	0x42

- Write 0x06 to Control Register 3 (CNTL3) to set the Output Data Rate of the Wake Up function (motion detection) (OWUF) to 50 Hz.

Register Name	Address	Value
CNTL3	0x1A	0x06

- Write 0x7F to Interrupt Control Register 2 (INC2) to define the direction of detected motion for all positive and negative directions: x positive (x+), x negative (x-), y positive (y+), y negative (y-), z positive (z+), z negative (z-) directions.

Register Name	Address	Value
INC2	0x1D	0x7F

- Write 0x05 to Interrupt Wake-Up Timer (WUFC) to set the time motion must be present before a wake-up interrupt is set to 0.1 second. The following formula is used:

WUFC (counts) = Desired Delay Time (sec) x OWUF (Hz)

WUFC (counts) = 0.1 x 50 = 5 counts

Since the desired delay time is 0.1 second and the OWUF was previously set to 50 Hz, then the Wake-Up Timer is 5 counts (0000 0101).

Register Name	Address	Value
WUFC	0x23	0x05

- Write 0x08 to Interrupt Wake-Up Threshold (ATH) to set the level to 0.5g. The following formula is used:

WAKEUP_THREHOLD (counts) = Desired Threshold (g) x 16 (counts/g)

WAKEUP_THREHOLD (counts) = 0.5 x 16 = 8 counts

Note that this threshold is differential with respect to the previous reading.

Register Name	Address	Value
ATH	0x30	0x08

- Write 0x30 to Interrupt Control Register (INC1) to output the physical interrupt of the previously defined Wake-Up detect function. This value will create an active high and latched interrupt.

Register Name	Address	Value
INC1	0x1C	0x30

- Write 0x02 to Interrupt Control Register 4 (INC4) to set the WUF interrupt to be reported on physical interrupt pin INT1.

Register Name	Address	Value
INC4	0x1F	0x02

- Write 0xC2 to Control Register 1 (CNTL1) to set the accelerometer in operating mode with the previously defined settings.

Register Name	Address	Value
CNTL1	0x18	0xC2

- Monitor the physical interrupt INT1 of the accelerometer, if the acceleration input profile satisfies the criteria previously established for the 0.5g motion detect threshold level in both positive and negative directions of the X, Y, Z axis for more than 0.1 second, then there should be positive latched interrupt present.

- Read Interrupt Release (INT_REL) register to unlatch (clear) the output interrupt created by the motion detection function.

Register Name	Address	Value
INT_REL	0x17	n/a

- Monitor the physical interrupt INT1 of the accelerometer, the positive latched interrupt should not be present. Repeat the last two steps of moving the accelerometer and clearing the interrupt as needed to test this motion detect functionality based on the previous settings.

5. Activate Tilt Position Function

- Write 0x41 to Control Register 1 (CNTL1) to set the accelerometer in stand-by mode, to set the performance mode to High Resolution (full power), G-range to ±2g, and enable the Tilt Position function.

Register Name	Address	Value
CNTL1	0x18	0x41

- Write 0x3F to Control 2 register (CNTL2) to enable Tilt detection from positive and negative directions of all three axes (+x, -x, +y, -y, +z, -z). This step is optional as this is also a default setting.

Register Name	Address	Value
CNTL2	0x19	0x3F

- Write 0x98 to Control 3 register (CNTL3) to set the output data rate for the Tilt Position function to 12.5Hz. This step is optional as this is also a default setting.

Register Name	Address	Value
CNTL3	0x1A	0x98

- Write 0x01 to TILT_TIMER register. Here we assume an 80 msec timer will be sufficient. Note that each count value written to this register is calculated as 1/(Tilt Position ODR) = 1/12.5Hz = 80 msec.

Register Name	Address	Value
TILT_TIMER	0x22	0x01

- Write 0x0C to Tilt Angle Low Limit (TILT_ANGLE_LL) register to set the low threshold to 22º from Horizontal. The value is calculated using the following equations: TILT_ANGLE_LL (counts) = sin θ * (32 (counts/g)). This step is optional as this is also a default setting.

Register Name	Address	Value
TILT_ANGLE_LL	0x32	0x0C

- Write 0x2A to Tilt Angle High Limit (TILT_ANGLE_HL) register to set the High threshold. This step is optional as this is also a default setting.

Register Name	Address	Value
TILT_ANGLE_HL	0x33	0x2A

- Write 0x14 to HYST_SET register to set the hysteresis that is placed between the screen rotation states to ±15º. This step is optional as this is also a default setting

Register Name	Address	Value
HYST_SET	0x34	0x14

- Write 0x30 to Interrupt Control Register (INC1) to output the physical interrupt of the previously defined Tap/Double-Tap function. This value will create an active high and latched interrupt.

Register Name	Address	Value
INC1	0x1C	0x30

- Write 0x01 to Interrupt Control Register 4 (INC4) to set the Tilt Position interrupt (TPI1) to be reported on physical interrupt pin INT1.

Register Name	Address	Value
INC4	0x1F	0x01

- Write 0xC1 to Control Register 1 (CNTL1) to set the accelerometer in operating mode with the previously defined settings.

Register Name	Address	Value
CNTL1	0x18	0xC1

- Monitor the physical interrupt INT1 of the accelerometer. If changes in the tilt position satisfies the criteria previously established, then there should be a positive latched interrupt present. Also, the interrupt would be reflected in bit 4 of STATUS_REG (INT bit), bit 0 of INS2 (TPS bit), and Current Tilt Position register TSCP as well as Previous Tilt Position register TSPP

- Read Interrupt Release (INT_REL) register to unlatch (clear) the output interrupt created by the Tilt Position function. The read value is dummy.

Register Name	Address	Value
INT_REL	0x17	N/A

6. Activate Tap/Double Tap Function

- Write 0x44 to Control Register 1 (CNTL1) to set the accelerometer in stand-by mode, to set the performance mode to High Resolution (full power), G-range to ±2g, and enable the Directional Tap function.

Register Name	Address	Value
CNTL1	0x18	0x44

- Write 0x3F to Interrupt Control 3 register (INC3) to enable tap/double tap from positive and negative directions of all three axes (+x, -x, +y, -y, +z, -z). This step is optional as this is also a default setting.

Register Name	Address	Value
INC3	0x1E	0x3F

- Write 0x98 to Control 3 register (CNTL3) to set the output data rate for the Directional Tap function to 400Hz. This step is optional as this is also a default setting.

Register Name	Address	Value
CNTL3	0x1A	0x98

- Write 0x03 to Tap / Double-Tap Register Control register (TDTRC) to enable interrupt on single tap and double tap. This step is optional as this is also a default setting. This setting can be adjusted as needed.

Register Name	Address	Value
TDTRC	0x24	0x03

- Write 0x78 to Tap / Double-Tap Counter register (TDTC) to set the counter to 0.3 sec. The TDTC counts starts at the beginning of the fist tap and it represents the minimum time separation between the first tap and the second tap in a double tap event. More specifically, the second tap event must end outside of the TDTC. This step is optional as this is also a default setting. This setting can be adjusted as needed.

Register Name	Address	Value
TDTC	0x25	0x78

- Write 0xCB (203d) to Tap Threshold High register (TTH). This register represents the 8-bit jerk high threshold to determine if a tap is detected. Though this is an 8-bit register, the register value is internally multiplied by two in order to set the high threshold. This multiplication results in a range of 0d to 510d with a resolution of two counts. The Performance Index (PI) is the jerk signal that is expected to be less than this threshold, but greater than the TTL threshold during single and double tap events. This step is optional as this is also a default setting. This setting can be adjusted as needed.

Register Name	Address	Value
TTH	0x26	0xCB

- Write 0x1A (26d) to Tap Threshold Low register (TTL). This register represents the 8-bit (0d–255d) jerk low threshold to determine if a tap is detected. The Performance Index (PI) is the jerk signal that is expected to be greater than this threshold and less than the TTH threshold during single and double tap events. This step is optional as this is also a default setting. This setting can be adjusted as needed.

Register Name	Address	Value
TTL	0x27	0x1A

- Write 0xA2 (162d) to set the FTD counter register to 0.005 seconds. This register contains counter information for the detection of *any* tap event. A tap event must be above the performance index threshold for at least the low limit (FTDL0 – FTDL2) and no more than the high limit (FTDH0 – FTDH4). This step is optional as this is also a default setting. This setting can be adjusted as needed.

Register Name	Address	Value
FTD	0x28	0xA2

- Write 0x24 (36d) to set the STD counter register to 0.09 seconds. This register contains counter information for the detection of a *double* tap event. This register sets the total amount of time that the two taps in a double tap event can be above the PI threshold (TTL). This step is optional as this is also a default setting. This setting can be adjusted as needed.

Register Name	Address	Value
STD	0x29	0x24

- Write 0x28 (40d) to set the TLT counter register to 0.1 seconds. This register contains counter information for the detection of a tap event. This register sets the total amount of time that the tap algorithm will count samples that are above the PI threshold (TTL) during a potential tap event. It is used during both single and double tap events. However, reporting of single taps on the physical interrupt pin INT1 or INT2 will occur at the end of the TWS. This step is optional as this is also a default setting. This setting can be adjusted as needed.

Register Name	Address	Value
TLT	0x2A	0x28

- Write 0xA0 (160d) to set the TWS counter register to 0.4 seconds. This register contains counter information for the detection of single and double taps. This counter defines the time window for the entire tap event, single or double, to occur. Reporting of single taps on the physical interrupt pin INT1 or INT2 will occur at the end of this tap window. This step is optional as this is also a default setting. This setting can be adjusted as needed.

Register Name	Address	Value
TWS	0x2B	0xA0

- Write 0x30 to Interrupt Control Register (INC1) to output the physical interrupt of the previously defined Tap/Double-Tap function. This value will create an active high and latched interrupt.

Register Name	Address	Value
INC1	0x1C	0x30

- Write 0x04 to Interrupt Control Register 4 (INC4) to set the Tap/Double-Tap interrupt (TDTI) to be reported on physical interrupt pin INT1.

Register Name	Address	Value
INC4	0x1F	0x04

- Write 0xC4 to Control Register 1 (CNTL1) to set the accelerometer in operating mode with the previously defined settings.

Register Name	Address	Value
CNTL1	0x18	0xC4

- Monitor the physical interrupt INT1 of the accelerometer, if the acceleration input profile satisfies the criteria previously established for Tap/Double-Tap, then there should be a positive latched interrupt present. Also, the interrupt would be reflected in bit 4 of STATUS_REG (INT bit), and bit 3 and bit 2 of INS2 registers. To distinguish between a single and double-tap events, monitor INS2 register bits <TDTS1:TDTS0>. TDTS1 bit3 would be set for Double-tap event, and TDTS0 bit2 for Single-tap event. Also, INS1 register can be monitored to identify the direction the tap came from.

- Read Interrupt Release (INT_REL) register to unlatch (clear) the output interrupt created by the Tap/Double-Tap detection function. The read value is dummy.

Register Name	Address	Value
INT_REL	0x17	N/A

Timing Requirements

There are several timing requirements that developers should keep in mind when working with the KX023 and KX022.

I²C Clock - The I²C Clock can support Fast Mode up to **400 KHz** and High Speed mode up to **3.4 MHz**.

SPI Clock - The SPI Clock can support up to **10MHz**.

Enable to Valid Outputs - After the part is enabled (PC1 bit in Control Register 1 is asserted), it takes from **3.4 ms** to **80 ms** depending on the ODR before the acceleration outputs are valid. (See KX021/KX022/KX023 Product Specification for details)

Power-Up Time (Time from VDD and IO_VDD valid to device boot completion) - After a Power-up, the part takes between **10 ms** to **50 ms** before it is ready for communication.

Software Reset Delay - After a Software Reset, the part takes **2 ms** before it is ready for I²C communication.

Standby to Operation Delay - Please allow 1.5/ODR delay time when transitioning from stand-by PC1 = 0 to operating mode PC1 = 1 to allow new settings to load.

Interrupt Configuration

The physical interrupt has 6 possible configurations, based on two states for each of the three customizable variables located in Interrupt Control Register 1:

Latched/Pulsed (IEL – bit 3 – 0x08)

0 – Latched mode – When an interrupt is triggered, it will remain active on the pin until cleared.

1 – Pulse mode – When an interrupt is triggered, it will cause a short (~50µs) pulse on the pin and clear itself.

Polarity (IEA – bit 4 – 0x10)

0 – Active Low – The interrupt pin will normally be HIGH, but will transition to LOW when an interrupt is triggered.

1 – Active High – The interrupt pin will normally be LOW, but will transition to HIGH when an interrupt is triggered.

Enable/Disable (IEN – bit 5 – 0x20)

0 – Disabled – Interrupt conditions will not be reflected on the physical interrupt pin.

1 – Enabled – Interrupt conditions will be reflected on the physical interrupt pin.

A Few Interrupt Tips

Read the Interrupt Release Register to Clear

In latched mode, the INT_REL register must be read in order to clear the physical interrupt pin. This will also clear the Interrupt Source Registers and the INT bit (0x10) in the Status Register.

Microcontroller/GPIO Interrupt Handling –

GPIO configuration is based solely on the connected hardware. The KX021, KX022 and KX023 can be configured to issue interrupts depending on how the GPIO is programmed to catch them (if this is not the case, please contact your Kionix Sales Representative). Generally, when an interrupt is triggered, the developer should take the following steps:

1- Disable GPIO interrupt

2- Clear GPIO interrupt and generate desired functionality

3- Enable GPIO interrupt

These steps should be taken without calling any digital communication transactions if done in an interrupt context, because the operating system or kernel will not allow busy-waiting on an I/O operation during an interrupt service routine.

Interrupt Polling - If physical interrupts are not used, a polling mechanism can be devised, which checks the INT bit in STATUS_REG. This mechanism should then look at INT_SRC_REG2 to determine which engine caused the interrupt and what steps should be taken before clearing the interrupt source information by reading the INT_REL register.

Troubleshooting

All Interrupt Issues

- Make sure the KX021, KX022, and/or KX023 are configured to issue interrupt signals in the way that your GPIO is programmed to handle them.
- An oscilloscope on the physical interrupt pin can be a valuable tool to confirm physical interrupt operation.
- Double check the Tilt Position State Mask bits in Control Register 2 (Tilt Position Function), the axis mask bits in Interrupt Control Register 2 (Wake-up Function), and/or the Tap/Double-Tap Mask bits in Interrupt Control Register 3 (Tap/Double-Tap Function).
- The Tilt Timer, WUF Timer, and TDT Timer(s) are based on their respective Output Data Rates, so make sure the correct cycle time is used when calculating the expected timer length (please refer to the KX023 and KX022 product specification).

Tilt Interrupt Not Working

- Make sure that the Tilt Position engine is enabled (TPE bit in Control Register 1).
- Try shortening the timer requirements and make sure the next state transition does not occur until after the expiration of the Tilt Timer.
- Try increasing the Tilt Angle to ensure that the engine can see the transition between the X and Y axes and the Z axis (this should not be necessary if using the default value for Tilt Angle, but it's worth looking into if problems continue).

WUF (Wake Up Function) Interrupt Not Working

- Make sure that the WUF engine is enabled (WUFE bit in Control Register 1).
- Try altering the threshold requirements to achieve desired operation. If the part is waking up too easily, try increasing the threshold. If the interrupt is not firing at all, the threshold may be set too high.
- Try shortening the timer requirements, and make sure the acceleration on an unmasked axis is above the threshold until the expiration of the WUF Timer.

TDT (Tap/Double-Tap) Interrupt Not Working

- Make sure that the TDT engine is enabled (TDTE bit in Control Register 1).
- Try altering the threshold requirements to achieve desired operation. If the part is generating interrupts too often, perhaps due to a large noise floor created by excessive environmental vibrations, try increasing the performance index low threshold (TTL) and/or reducing the performance index high threshold (TTH). If the interrupt is not firing at all, perhaps the low threshold may be set too high, or the high threshold may be set too low.
- There are many timers in this engine which have to work together closely, so for standard operation if one timer is changed the other timers may need to be changed proportionally.

Accelerometer Placement and Orientation

Placement – It is important to note that the placement of the accelerometer within the target device can have a significant effect on tap/double-tap direction resolution. If tap detection is desired, the part should be placed as far away from the edges of the device housing as possible, with the ideal location being at the target device's center of mass.

Orientation – While it is recommended to align the accelerometer's axes with those of the target device, it will sometimes be desirable or necessary to alter the part's orientation with respect to the device housing. Rotating about the Z axis at intervals of 90 degrees or about the X or Y axes at intervals of 180 degrees should not impact functionality. However, it is highly recommended that the device is not rotated 90 or 270 degrees about the X or Y axes. Due to the asymmetrical nature of the tilt position function, altering the orientation of the Z axis in this manner can cause incorrect screen rotation direction resolution.

The Kionix Advantage

Kionix technology provides for X, Y, and Z-axis sensing on a single, silicon chip. One accelerometer can be used to enable a variety of simultaneous features including, but not limited to:

Hard Disk Drive protection
Vibration analysis
Tilt screen navigation
Sports modeling
Theft, man-down, accident alarm
Image stability, screen orientation & scrolling
Computer pointer
Navigation, mapping
Game playing
Automatic sleep mode

Theory of Operation

Kionix MEMS linear tri-axis accelerometers function on the principle of differential capacitance. Acceleration causes displacement of a silicon structure resulting in a change in capacitance. A signal-conditioning CMOS technology ASIC detects and transforms changes in capacitance into an analog output voltage, which is proportional to acceleration. These outputs can then be sent to a micro-controller for integration into various applications.

For product summaries, specifications, and schematics, please refer to the Kionix MEMS accelerometer product catalog at http://www.kionix.com/parametric/Accelerometers.