Integrated Circuit Systems, Inc.

ICS8501

LOW SKEW, 1-TO-16 DIFFERENTIAL CURRENT MODE FANOUT BUFFER

GENERAL DESCRIPTION

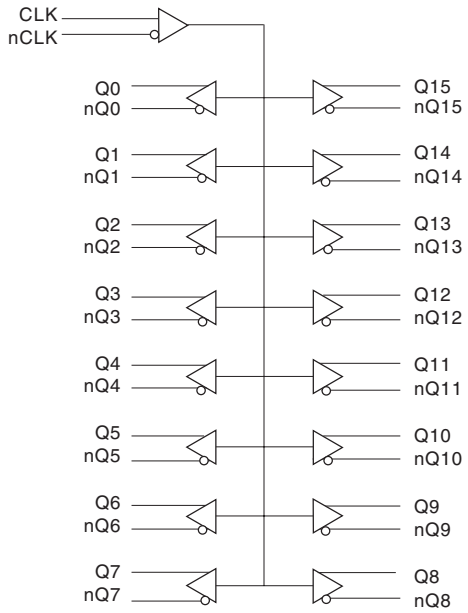
The ICS8501 is a low skew, 1-to-16 Differential Current Mode Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8501 is designed to translate any differential signal levels to small swing differential current mode (DCM) output levels. An external reference resistor is used to set the value of the current supplied to an external load load/termination resistor. The load resistor value is chosen to equal the value of the characteristic line impedance of 50Ω. The ICS8501 is characterized at an operating supply voltage of 3.3V.

The small swing outputs, accurate crossover voltage and duty cycle makes the ICS8501 ideal for interfacing to today's most advanced microprocessors.

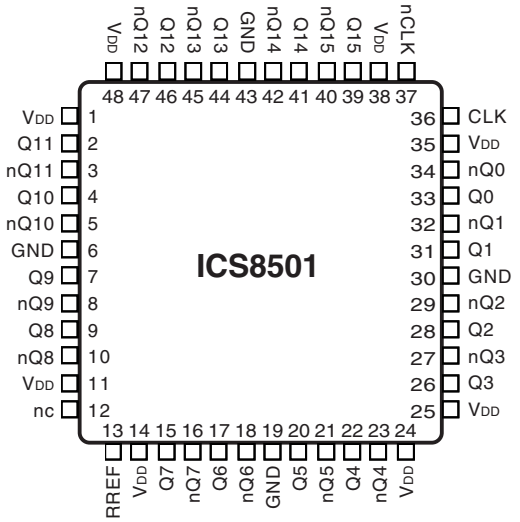
FEATURES

- 16 small swing DCM outputs
- Translates any differential input signal (LVPECL, LVHSTL, LVDS, DCM) to DCM levels without external bias networks
- Translates single ended input levels to DCM levels with a resistor bias network on the nCLK input
- Translates single ended input levels to inverted DCM levels with a resistor bias network on the CLK input
- Maximum output frequency: 500MHz
- Output skew: 100ps (maximum)
- Part-to-part skew: 650ps (maximum)
- V_{OH}: 850mV (maximum)
- 3.3V operating supply
- 0°C to 70°C ambient operating temperature

BLOCK DIAGRAM



PIN ASSIGNMENT



48-Lead LQFP
7mm x 7mm x 1.4mm body package
Y Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type	Description
1, 11, 14, 24, 25, 35, 38, 48	V_{DD}	Power	Positive supply pins.
2, 3	Q11, nQ11	Output	Differential output pair. Differential current mode interface levels.
4, 5	Q10, nQ10	Output	Differential output pair. Differential current mode interface levels.
6, 19, 30, 43	GND	Power	Power supply ground.
7, 8	Q9, nQ9	Output	Differential output pair. Differential current mode interface levels.
9, 10	Q8, nQ8	Output	Differential output pair. Differential current mode interface levels.
12	nc	Unused	No connect.
13	RREF	Input	Reference current input. Used to set the output current. Connect to 475Ω resistor to ground.
15, 16	Q7, nQ7	Output	Differential output pair. Differential current mode interface levels.
17, 18	Q6, nQ6	Output	Differential output pair. Differential current mode interface levels.
20, 21	Q5, nQ5	Output	Differential output pair. Differential current mode interface levels.
22, 23	Q4, nQ4	Output	Differential output pair. Differential current mode interface levels.
26, 27	Q3, nQ3	Output	Differential output pair. Differential current mode interface levels.
28, 29	Q2, nQ2	Output	Differential output pair. Differential current mode interface levels.
36	CLK	Input	Non inverting differential clock input.
37	nCLK	Input	Inverting differential clock input.
39, 40	Q15, nQ15	Output	Differential output pair. Differential current mode interface levels.
41, 42	Q14, nQ14	Output	Differential output pair. Differential current mode interface levels.
44, 45	Q13, nQ13	Output	Differential output pair. Differential current mode interface levels.
46, 47	Q12, nQ12	Output	Differential output pair. Differential current mode interface levels.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			2		pF
C_{PD}	Power Dissipation Capacitance (per output)	V_{DD} = 3.465V, f = 250MHz		4.6		pF
R_{OUT}	Output Impedance			14		KW

TABLE 3. FUNCTION TABLE

Inputs		Outputs		Input to Output Mode	Polarity
CLK	nCLK	Q0:Q15	nQ0:nQ15		
0	1	0	1	Differential to Differential	Non Inverting
1	0	1	0	Differential to Differential	Non Inverting
0	Biased; NOTE 1	0	1	Single Ended to Differential	Non Inverting
1	Biased; NOTE 1	1	0	Single Ended to Differential	Non Inverting
Biased; NOTE 1	0	1	0	Single Ended to Differential	Inverting
Biased; NOTE 1	1	0	1	Single Ended to Differential	Inverting

NOTE 1: Please refer to the Application Information Section, *Wiring the Differential Input to Accept Single Ended Level*s.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				70	mA

TABLE 4B. DIFFERENTIAL DC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK, nCLK	$V_{DD} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	CLK, nCLK	V_{DD} = 3.465V, V_{IN} = 0V			5	µA
V_{PP}	Peak-to-Peak Input Voltage			0.31		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2		LVPECL Levels	1.8		2.4	V
			DCM, HSTL, LVDS, SSTL Levels	0.31		1.3	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for CLK, nCLK is V_{DD} + 0.3V.

TABLE 4C. HCSL DC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
I_{OH}	Output High Current; NOTE 1	3.135 ≤ V_{DD} ≤ 3.465V	11	14	17	mA
V_{OH}	Output HighVoltage; NOTE 2	RREF = 475Ω, RLOAD - 50Ω	600	710	850	mV
V_{OL}	Output Low Voltage; NOTE 2	RREF = 475Ω, RLOAD - 50Ω		0	0.05	V
V_{OX}	Output Crossover Voltage; NOTE 3		40		60	%

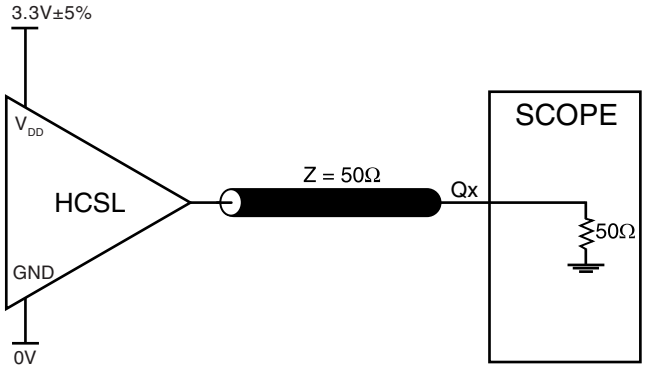
NOTE 1: I_{OH} is the current per output being supplied to the load and should be included in the total supply current calculation. Therefore, I_{DD} (total) is equal to I_{OH} * 16 + I_{DD}.
NOTE 2: Outputs terminated with 50Ω to V_{DD} - 2V.
NOTE 3: Define with respect to output voltage swing at a given condition.

TABLE 5. HCSL AC CHARACTERISTICS, V_{DD} = 3.3V±5%, T_A = 0°C TO 70°C

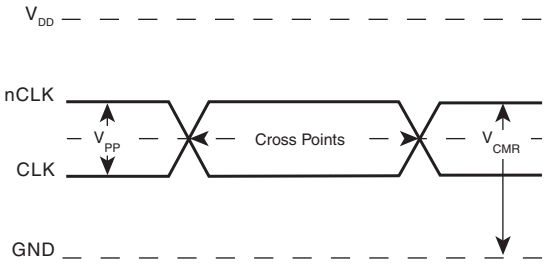
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency	Measured at the -3dB rolloff of the peak-to-peak output voltage			500	MHz
$tp_{LH,}$	Propagation Delay; Low-to-High	0 < f ≤ 250MHz	2		3	ns
tp_{HL}	Propagation Delay; High-to-Low	0 < f ≤ 250MHz	2		3	ns
*t*sk(o)	Output Skew; NOTE 1, 3	Measured on at VOX			100	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 3	Measured on at VOX			650	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	175		700	ps
t_{PW}	Output Pulse Width		$t_{PERIOD}/2$ - 0.3	$t_{PERIOD}/2$	$t_{PERIOD}/2$ + 0.3	ns

Current adjust set for V_{OH} = 0.7V. Measurements refer to PCIEX outputs only.
NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 2: Defined as the skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DD}/2$.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

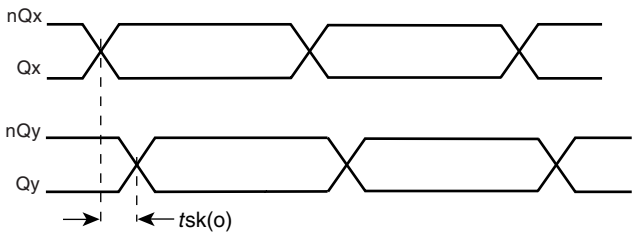
PARAMETER MEASUREMENT INFORMATION



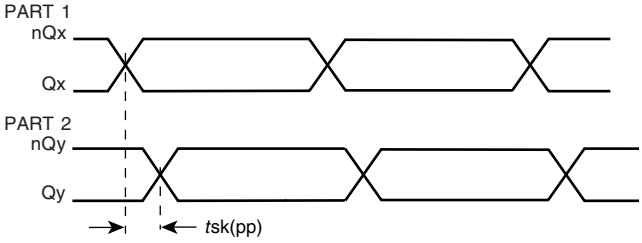
3.3V HCSL OUTPUT LOAD AC TEST CIRCUIT



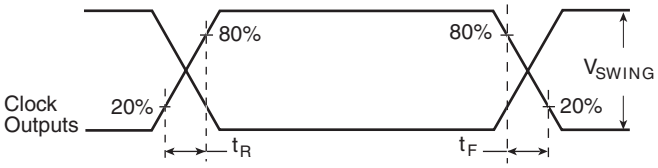
DIFFERENTIAL INPUT LEVEL



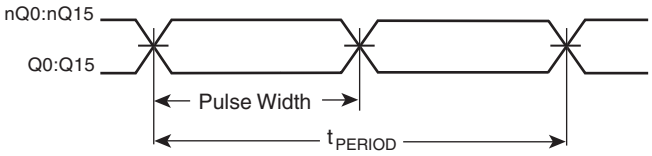
OUTPUT SKEW



PART-TO-PART SKEW



HCSL OUTPUT RISE/FALL TIME



OUTPUT PULSE WIDTH/PERIOD

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

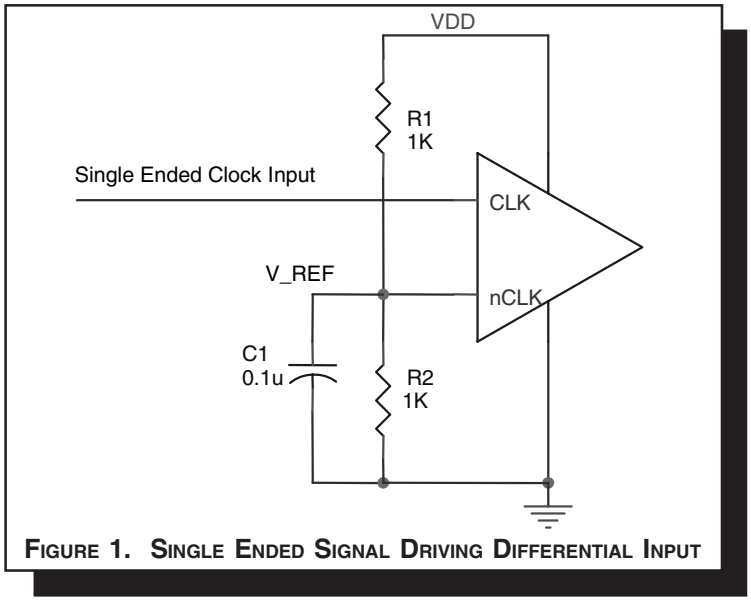


FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 2A to 2D show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 2A,* the input termination applies for ICS HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

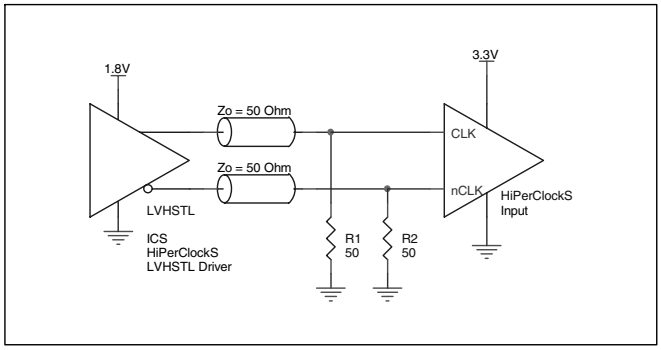


FIGURE 2A. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY ICS HIPERCLOCKS LVHSTL DRIVER

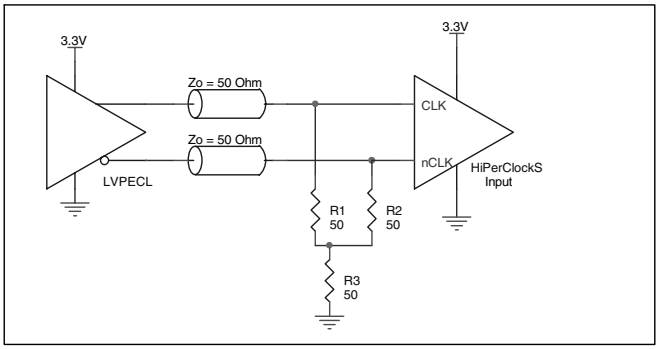


FIGURE 2B. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

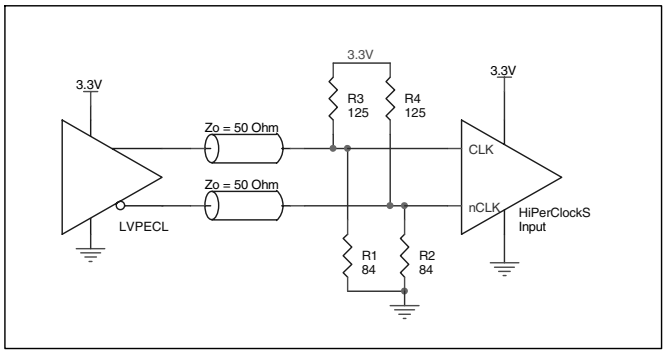


FIGURE 2C. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

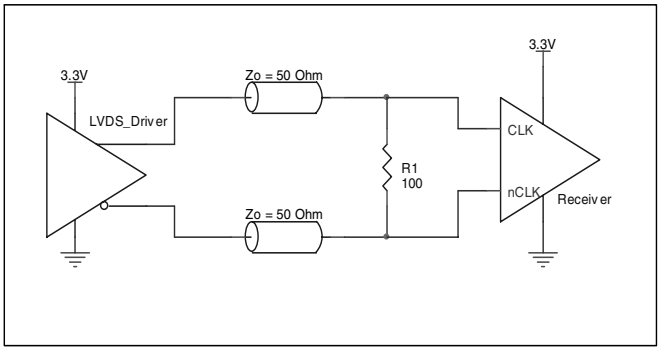


FIGURE 2D. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVDS DRIVER

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 48 LEAD LQFP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS8501 is: 1358

PACKAGE OUTLINE - Y SUFFIX FOR 48 LEAD LQFP

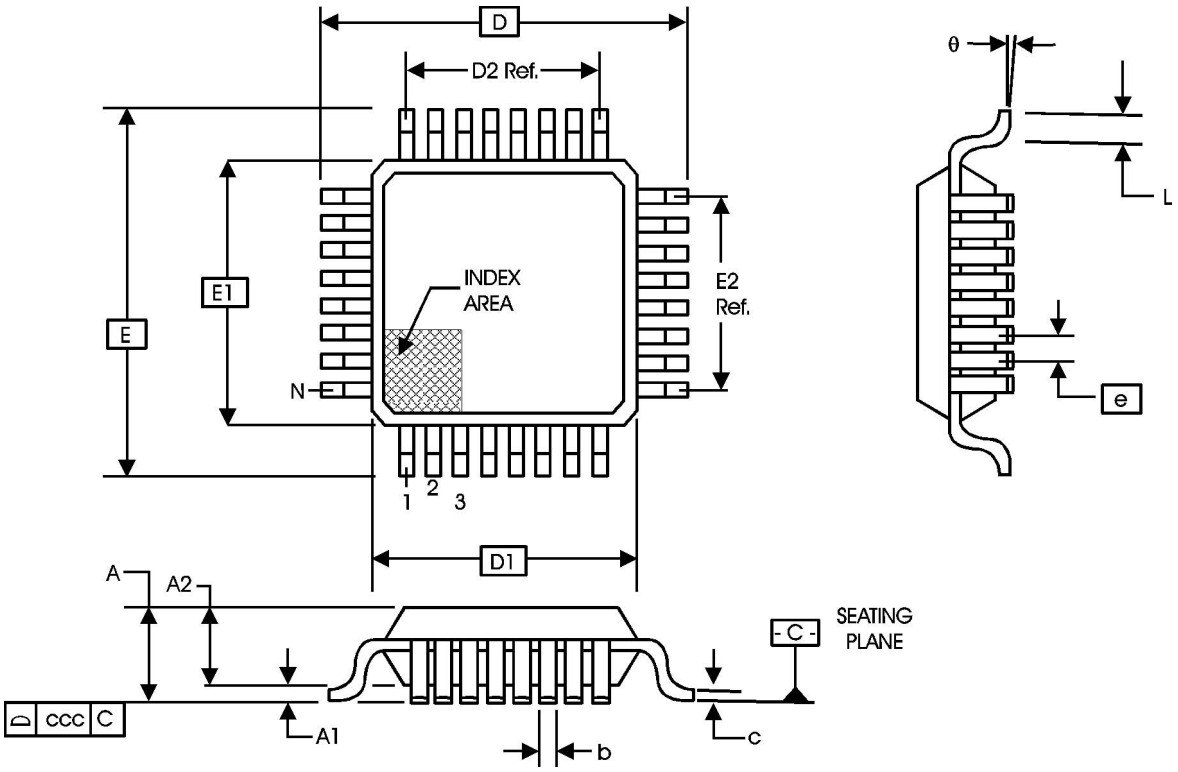


TABLE 7. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBC		
	MINIMUM	NOMINAL	MAXIMUM
N		48	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.50 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.50 Ref.	
e		0.50 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.08

Reference Document: JEDEC Publication 95, MS-026

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS8501BY	ICS8501BY	48 Lead LQFP	250 per tray	0°C to 70°C
ICS8501BYT	ICS8501BY	48 Lead LQFP on Tape and Reel	1000	0°C to 70°C

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
B	T1	2	Pin Description Table - changed V_{DD} and GND descriptions.	10/3/03
	T3	2	Function Table - revised NOTE 1.	
	T4A	3	Added Power Supply Table.	
	T4C	3	Added HCSL Table. Changed V_{OH} max. spec from 1.2V to 850mV; converted min. from 0.6V to 600mV and typical from 0.71V to 710mV.	
	T5	6 & 7	Changed units of V_{OX} from V to % and added note 3. Added Applications Section. Updated format throughout data sheet.	