MITSUBISHI ELECTRIC

Super mini DIP-IPM Ver.4

APPLICATION NOTE

PS2196X-4 series
PS2196X-T series

Jan. 2008

Table of Contents

CHAPTER 1 Super Mini DIP-IPM Ver.4 INTRODUCTION

1.1 Target Applications

Motor drives for household electric appliances, such as air conditioners, washing machines, refrigerators. Low power industrial motor drives with 1500V isolation voltage except automotive applications.

1.2 Product Line-up

Table 1-1. Super Mini DIP-IPM Ver.4 Line-up

Type Name (Note 1)	IGBT Rating	Motor Rating (Note 2)	Isolation Voltage
PS21961-4/-4A/-4C/-4S/-4W	3A/600V	0.2kW/220V_{AC}	V_{iso} = 1500Vrms (Sine 60Hz, 1min All shorted pins-heat sink)
PS21962-4/-4A/-4C/-4S/-4W	5A/600V	0.4kW/220V_{AC}	
PS21963-4E/-4AE/-4CE/-4ES/-4EW	8A/600V	0.75kW/220V_{AC}	
PS21963-4/-4A/-4C/-4S/-4W	10A/600V	0.75kW/220V_{AC}	
PS21964-4/-4A/-4C/-4S/-4W	15A/600V	0.75kW/220V_{AC}	
PS21965-4/-4A/-4C/-4S/-4W	20A/600V	1.5kW/220V_{AC}	

Table 1-2. Super Mini DIP-IPM Ver.4 Line-up with over temperature protection function type

Type Name (Note 1)	IGBT Rating	Motor Rating (Note 2)	Isolation Voltage
PS21961-T/-AT/-CT/-TW/-ST	3A/600V	0.2kW/220V_{AC}	V_{iso} = 1500Vrms (Sine 60Hz, 1min All shorted pins-heat sink)
PS21962-T/-AT/-CT/-TW/-ST	5A/600V	0.4kW/220V_{AC}	
PS21963-ET/-AET/-CET /-ETW/-EST	8A/600V	0.75kW/220V_{AC}	
PS21963-T/-AT/-CT/-TW/-ST	10A/600V	0.75kW/220V_{AC}	
PS21964-T/-AT/-CT/-TW/-ST	15A/600V	0.75kW/220V_{AC}	
PS21965-T/-AT/-CT/-TW/-ST	20A/600V	1.5kW/220V_{AC}	

Note 1: Type name suffixed by '-A' indicates the option for long pin type, '-C' for zigzag pin type, '-S' for N-side open emitter type, '-W' for both sides zigzag pin type and '-T' with over temperature protect. Please refer to chapter 2 for details.

Note 2: The motor ratings are simulation results under following conditions: V_{AC}=220V, V_D=V_{DB}=15V, Tc=100°C, Tj=125°C, f_{PWM}=5kHz, P.F=0.8, motor efficiency=0.75, current ripple ratio=1.05, motor over load 150% 1min.

1.3 Functions and Features

Super Mini DIP-IPM Ver.4 is an ultra-small compact intelligent power module with transfer mold package favorable for larger mass production. Power chips, drive and protection circuits are integrated in the module, which makes it easy for AC100-200V class low power motor inverter control. Fig.1-1, Fig.1-2 and Fig.1-3 show the photograph, internal cross-section structure and the circuit block diagram respectively.

One of the most important features of Super Mini DIP-IPM Ver.4 is that it realized higher thermal dissipation by incorporating thermal structure with high thermal conductive isolating sheet, due to which, the chip shrink becomes possible and therefore achieved super-small package with lower temperature rise than previous DIP-IPM Ver.3.

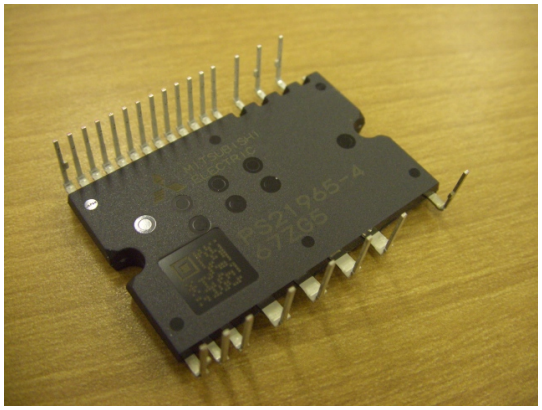


Fig.1-1 Package photograph

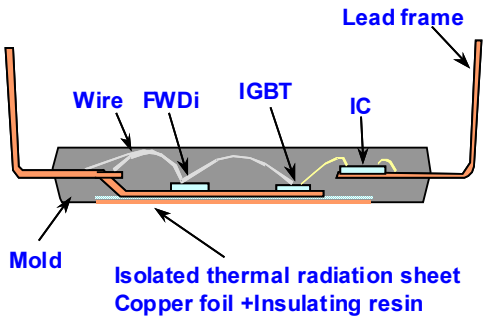


Fig.1-2 Internal cross-section structure
(except for PS21961)

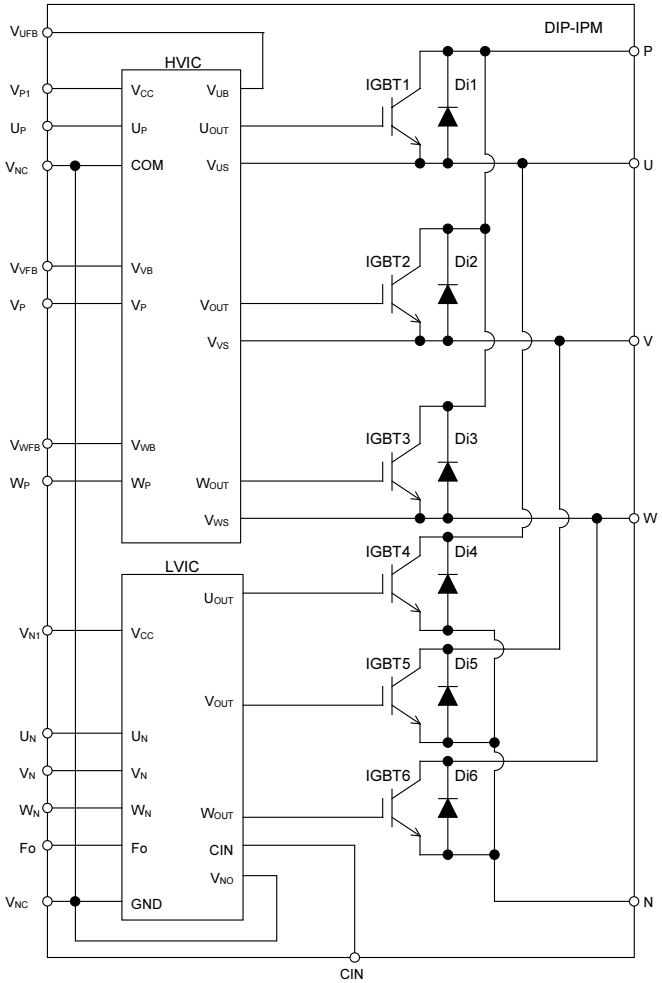


Fig.1-3 Internal circuit schematic (except for type '-S')

Features:

- For P-side IGBTs:
  - -Drive circuit;
  - -High voltage level shift circuit;
  - -Control supply under voltage (UV) lockout circuit (without fault signal output).
- For N-side IGBTs:
  - -Drive circuit;
  - -Short circuit (SC) protection circuit (by using external shunt resistor)
  - -Control supply under voltage (UV) lockout circuit (with fault signal output)
  - -Over temperature (OT) protection (by monitoring LVIC temp). (-T series only)
- Fault Signal Output
  - -Corresponding to N-side IGBT SC protection, N-side UV protection and OT.
- IGBT Drive Supply
  - -Single DC15V power supply.
- Control Input Interface
  - -Schmitt-triggered 3V,5V input compatible, high active logic.

1.4 The differences between previous series (PS2196X-XXX) and this series (PS2196X-4,-T)

(1) Terminal frame change
The terminal frame is changed. This change intends to increase the insulation distance between terminals with high voltage potential so as to ensure the electric space meet the Japanese PSE（Product Safety of Electric home appliance and materials）standard requirements of clearance and creepage distances. For more detail, refer section 2.3.1~6 and 2.4.1.

(2) Change into internal connection between V_{NO} and V_{NC} terminals
In the previous series(PS2196X-XXX), the V_{NO} terminal (17pin) needs to be connected externally to the V_{NC} terminal (16pin) on the PCB. But in these series, the V_{NO} terminal is changed to connect with V_{NC} terminal inside the module. So, the external wiring connection becomes no more needed.
For more detail, refer section 2.3.8 and 3.1.2~5.

(3) Addition over temperature protection function (-T series only)
PS2196X-T series have over temperature (OT) protection function that the previous series (PS2196X-XXX) didn't have. For more detail, refer section 2.2.3.

CHAPTER 2 SPECIFICATIONS AND CHARACTERISTICS

2.1 Super Mini DIP-IPM Ver.4 Specifications

The Super Mini DIP-IPM Ver.4 specifications are described below by using PS21964-4/-4A/-4C/-4W (15A/600V) as an example. Please refer to respective datasheet for the detailed description of other types.

2.1.1 Maximum Ratings

The maximum ratings of PS21964-4/-4A/-4C/-4W are shown in Table 2-1.

Table 2-1 Maximum Ratings of PS21964-4/-4A/-4C/-4W

Maximum Ratings (Tj=25°C, unless otherwise noted)

Inverter Part:

Item	Symbol	Condition	Rating	Unit	
Supply voltage	V_{CC}	Applied between P-N	450	V	(1)
Supply voltage (surge)	$V_{CC(surge)}$	Applied between P-N	500	V	(2)
Collector-emitter voltage	V_{CES}		600	V	(3)
Each IGBT collector current	$\pm I_C$	Tc=25°C	15	A	(4)
Each IGBT collector current (peak)	$\pm I_{CP}$	Tc=25°C, less than 1ms	30	A	
Collector dissipation	P_C	Tc=25°C, per 1 chip	33.3	W	
Junction temperature	Tj	(Note 1)	-20 ~ +125	°C	(5)

(Note1) The maximum junction temperature rating of the power chips integrated within the DIP-IPM is 150°C(@Tc≤100°C). However, to ensure safe operation of the DIP-IPM, the average junction temperature should be limited to Tj(ave) ≤125°C (@Tc≤100°C).

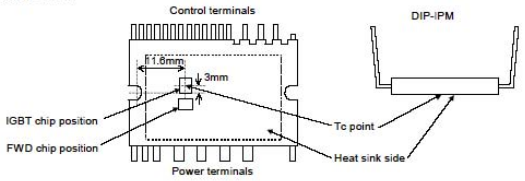
Control (Protection) Part

Item	Symbol	Condition	Rating	Unit
Control supply voltage	V_D	Applied between V_{P1}-V_{NC}, V_{N1}-V_{NC}	20	V
Control supply voltage	V_{DB}	Applied between V_{UFB}-U, V_{VFB}-V, V_{WFB}-W	20	V
Input voltage	V_{IN}	Applied between U_P,V_P,W_P-V_{NC}, U_N,V_N,W_N-V_{NC}	-0.5 ~ V_D+0.5	V
Fault output supply voltage	V_{FO}	Applied between Fo-V_{NC}	-0.5 ~ V_D+0.5	V
Fault output current	I_{FO}	Sink current at Fo terminal	1	mA
Current sensing input voltage	V_{SC}	Applied between CIN-V_{NC}	-0.5 ~ V_D+0.5	V

Total System

Item	Symbol	Condition	Rating	Unit	
Supply voltage self protection limit (short circuit protection capability)	$V_{CC(PROT)}$	V_D=13.5~16.5V, Inverter part Tj=125°C, non-repetitive less than 2μs	400	V	(6)
Module case operation temperature	Tc	(Note2)	-20 ~ +100	°C	
Storage temperature	Tstg		-40 ~ +125	°C	
Isolation voltage	Viso	60Hz, Sinusoidal, AC 1 minutes, All connected pins to heat-sink plate	1500	Vrms	

(Note2) Tc measurement position



(7)

Item explanation:

(1) Vcc The maximum P-N voltage in no switching state. A voltage suppressing circuit such as a brake circuit is necessary if P-N voltage exceeds this value.

(2) Vcc(surge) The maximum P-N surge voltage in no switching state. A snubber circuit is necessary if P-N voltage exceeds Vcc(surge).

(3) V_{CES} The maximum sustained collector-emitter voltage of built-in IGBT and FWDi.

(4) +/-I_C The allowable DC current continuously flowing at collect electrode (Tc=25°C)

(5) Tj Power cycles are ensured no less than 10 millions under the condition of Tf=100°C and Tj≤125°C. The rating value becomes low when temperature rises high.

(6) Vcc(prot) The maximum supply voltage for IGBT turning off safely in case of an SC fault. The power chip might be damaged if supply voltage exceeds this specification.

(7) Tc position Tc (case temperature) is defined to be the temperature just underneath the specified power chip. Please mount a thermistor in a heat sink surface at the defined position so as to get accurate temperature information.

2.1.2 Thermal Resistance

Table 2-2 shows the thermal resistance of PS21964-4/-4A/-4C/-4W.

Table 2-2. Thermal resistance of PS21964-4/-4A/-4C/-4W

Thermal Resistance

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Junction to case thermal resistance (Note3)	$R_{th(j-c)Q}$	Inverter IGBT part (per 1/6 module)	-	-	3.0	°C/W
	$R_{th(j-c)F}$	Inverter FWD part (per 1/6 module)	-	-	3.9	

(Note3) Grease with good thermal conductivity and long-term quality should be applied evenly with +100μm~+200μm on the contacting surface of DIP-IPM and heat-sink. The contacting thermal resistance between DIP-IPM case and heat sink ($R_{th(c-f)}$) is determined by the thickness and the thermal conductivity of the applied grease. For reference, $R_{th(c-f)}$ (per 1/6 module) is about 0.3°C/W when the grease thickness is 20μm and the thermal conductivity is 1.0W/m·k

The above data shows the thermal resistance between chip junction and case at steady state. The thermal resistance goes into saturation in about 10 seconds. The thermal resistance under 10sec is called as transient thermal impedance which is shown in Fig.2-1.

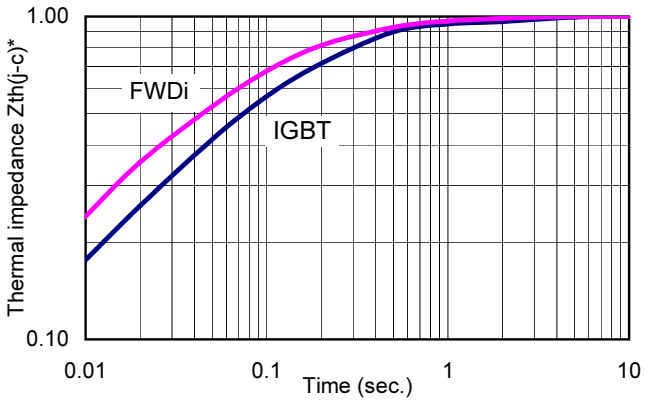


Fig.2-1 Typical transient thermal impedance

$Z_{th(j-c)}^{*}$ is the normalized value of the transient thermal impedance

$$Z_{th(j-c)}^{*} = Z_{th(j-c)} / R_{th(j-c)max}$$

for example, the IGBT transient thermal impedance of PS21964 in 0.3sec is 3.0×0.8=2.4°C/W.

2.1.3 Electric Characteristics (Power Part)

Table 2-3 shows the typical static characteristics and switching characteristics of PS21964-4/-4A/-4C/-4W.

Table 2-3. Static characteristics and switching characteristics of PS21964-4/-4A/-4C/-4W

Electrical Characteristics (Tj=25°C, unless otherwise noted) :

Inverter Part

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Collector-emitter saturation voltage	$V_{CE(sat)}$	$V_D=V_{DB}=15V$, $I_C=15A$, $V_{IN}=5V$	Tj=25°C	—	1.70	2.20	V
			Tj=125°C	—	1.80	2.30	
FWD forward voltage	V_{EC}	$-I_C=15A$, $V_{IN}=0V$		—	1.70	2.20	V
Switching times	t_{on}	$V_{CC}=300V$, $V_D=V_{DB}=15V$, $I_C=15A$, Tj=125°C, Inductive load, $V_{IN}=0⇔5V$		0.70	1.30	1.90	μs
	t_{rr}			—	0.30	—	
	$t_{c(on)}$			—	0.50	0.75	
	t_{off}			—	1.60	2.20	
	$t_{c(off)}$			—	0.50	0.80	
Collector-emitter cut-off current	I_{CES}	$V_{CE}=V_{CES}$	Tj=25°C	—	—	1	mA
			Tj=125°C	—	—	10	

Switching time definition and performance test method are shown in Fig.2-2 and 2-3.

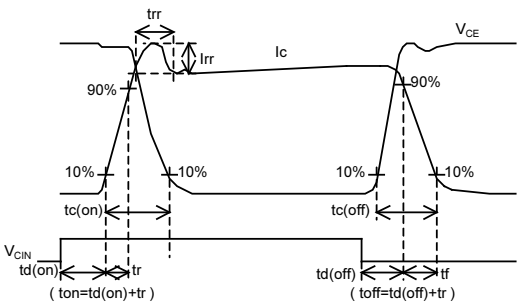


Fig.2-2 Switching time definition

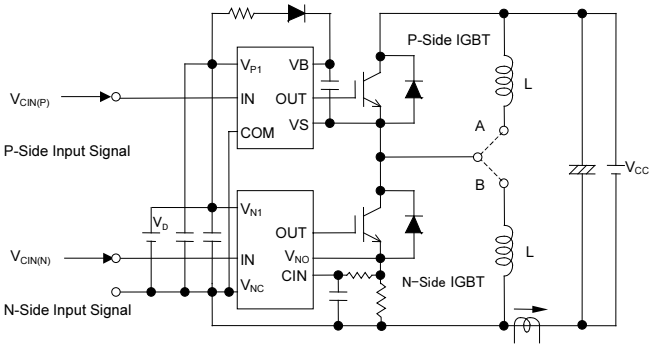


Fig.2-3 Evaluation circuit (inductive load)
Short A for N-side IGBT, and short B for P-side IGBT evaluation

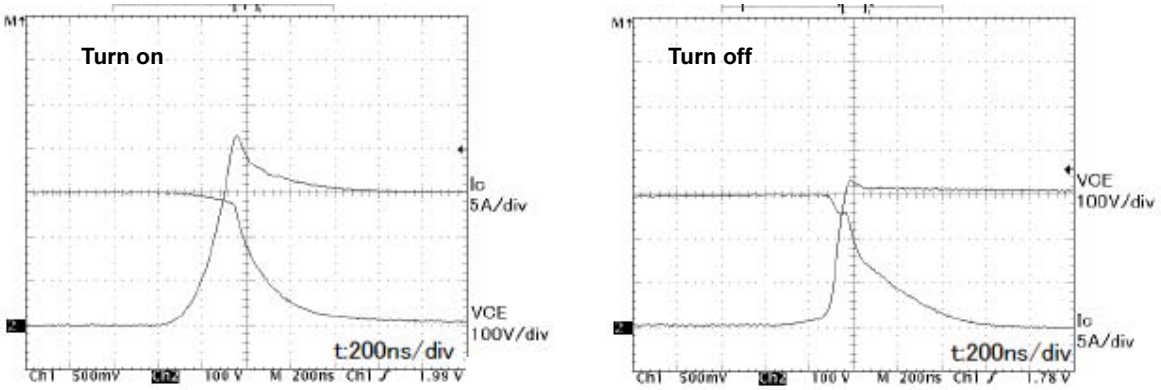


Fig.2-4 Typical switching waveform (PS21964-4)
Conditions : V_{CC}=300V, V_D=V_{DB}=15V, Tj=125°C, Ic=15A, Inductive load half-bridge circuit

2.1.4 Electric Characteristics (Control Part)

Table 2-4 Control (Protection) characteristics of PS21964-4/-4A/-4C/-4W

Control (Protection) Part:

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Circuit current	I_D	V_D=V_{DB}=15V, V_{IN}=5V	Total of V_{P1}-V_{NC}, V_{N1}-V_{NC}	—	—	2.80	mA
			V_{UFB}-U, V_{VFB}-V, V_{WFB}-W	—	—	0.55	
		V_D=V_{DB}=15V, V_{IN}=0V	Total of V_{P1}-V_{NC}, V_{N1}-V_{NC}	—	—	2.80	
			V_{UFB}-U, V_{VFB}-V, V_{WFB}-W	—	—	0.55	
Fo output voltage	V_{FOH}	V_{SC}=0V, Fo terminal pull-up to 5V by 10kΩ		4.9	—	—	V
	V_{FOL}	V_{SC}=1V, I_{FO}=1mA		—	—	0.95	
Input current	I_{IN}	V_{IN}=5V		0.70	1.00	1.50	mA
Short circuit trip level	$V_{SC(ref)}$	V_D=15V	(Note4)	0.43	0.48	0.53	V
Supply circuit under-voltage protection	UV_{DBt}	Tj≤125°C	Trip level	10.0	—	12.0	V
	UV_{DBr}		Reset level	10.5	—	12.5	
	UV_{Dt}		Trip level	10.3	—	12.5	
	UV_{Dr}		Reset level	10.8	—	13.0	
Fault output pulse width	t_{FO}		(Note5)	20	—	—	μs
ON threshold voltage	$V_{th(on)}$	Applied between U_P,V_P,W_P-V_{NC}, U_N,V_N,W_N-V_{NC}		—	2.1	2.6	V
OFF threshold voltage	$V_{th(off)}$			0.8	1.3	—	
ON/OFF threshold hysteresis voltage	$V_{th(hys)}$			0.35	0.65		

(Note4) Short circuit protection is functioning only for the lower-arms. Please select the external shunt resistance such that the SC trip-level is less than 1.7 times of the current rating.

(Note5) Fault signal is asserted corresponding to a short circuit or lower side control supply under-voltage failure.

2.1.5 Recommended Operating Conditions

The recommended operating conditions of PS21964-4/-4A/-4C/-4W are given in Table 2-5.

Although these conditions are the recommended but not the necessary ones, it is highly recommended to operate the modules within these conditions so as to ensure DIP-IPM safe operation.

Table 2-5 Recommended operating conditions of PS21964-4/-4A/-4C/-4W

Recommended Operation Conditions:

Item	Symbol	Condition		Recommended			Unit
				Min.	Typ.	Max.	
Supply voltage	V_{CC}	Applied between P-N		0	300	400	V
Control supply voltage	V_D	Applied between V_{P1}-V_{NC}, V_{N1}-V_{NC}		13.5	15.0	16.5	V
Control supply voltage	V_{DB}	Applied between V_{UFB}-U, V_{VFB}-V, V_{WFB}-W		13.0	15.0	18.5	V
Control supply variation	ΔV_D,ΔV_{DB}			-1	—	1	V/μs
Arm-shoot-through blocking time	t_{dead}	For each input signal, Tc≤100°C		1.5	—	—	μs
Output r.m.s. current	I_O	V_{CC}=300V, V_D=V_{DB}=15V, P.F=0.8, sinusoidal PWM, Tj≤125°C, Tc≤100°C (Note 8)	f_{PWM}=5kHz	—	—	7.5	Arms
			f_{PWM}=15kHz	—	—	4.5	
Allowable minimum input pulse width	PWIN(on)	(Note 9)		0.5	—	—	μs
	PWIN(off)			0.5	—	—	
V_{NC} voltage variation	V_{NC}	between V_{NC}-N (including surge)		-5.0	—	5.0	V

(Note 8) The allowable r.m.s. current value depends on the actual application conditons.
(Note 9) IPM might not work properly or make response if the Input signal pulse width is less than the recommended minimum value.

2.1.6 Mechanical Characteristics and Ratings

The mechanical characteristics and ratings are shown in Table 2-6

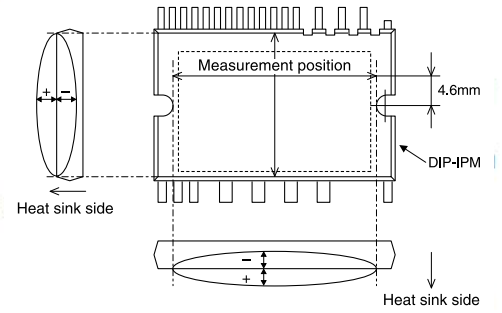
Please refer to Section 2.4 for the detailed mounting instruction of Super Mini DIP-IPM Ver.4.

Table 2-6 Mechanical characteristics and ratings of PS21964-4/-4A/-4C/-4W

Mechanical Characteristics and Ratings

Item	Condition		Min.	Typ.	Max.	Unit
Mounting torque	Mounting screw: M3 (Note 6)	Recommended: 0.69N· m	0.59	–	0.78	N· m
Weight			–	10	–	g
Heat-sink flatness	(Note 7)		–50	–	+100	μm

(Note 6) Plain washers (ISO 7089～7094) are recommended.
(Note 7) Flatness measurement position:



2.2 Protective Functions and Operating Sequence

There are SC protection, UV protection and OT protection (-T only) in the Super Mini DIP-IPM Ver.4. The operating principle and sequence are described below.

2.2.1 Short Circuit Protection

Super Mini DIP-IPM Ver.4 uses external shunt resistor for the current detection as shown in Fig.2-4. The internal protection circuit inside the IC captures the excessive large current by comparing the CIN voltage feedback from the shunt with the referenced SC trip voltage, and perform protection automatically. The threshold voltage trip level of the SC protection is 0.48V(typ.), according to which the shunt resistance should be correctly selected.

In case of SC protection happens, all the gates of N-side three phase IGBTs will be interrupted together with a fault signal output.

To prevent DIP-IPM erroneous protection due to normal switching noise and/or recovery current, it is necessary to set an RC filter(time constant: 1.5μ ~ 2μs) to the CIN terminal input (Fig.2-4, 2-5). Also, please make the pattern wiring around the shunt resistor as short as possible.

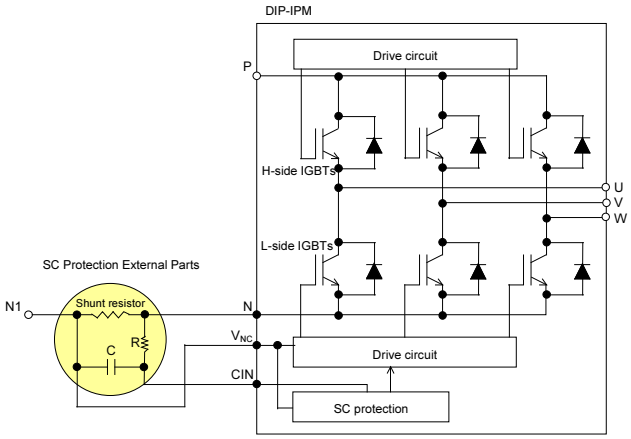


Fig.2-4 SC protecting circuit

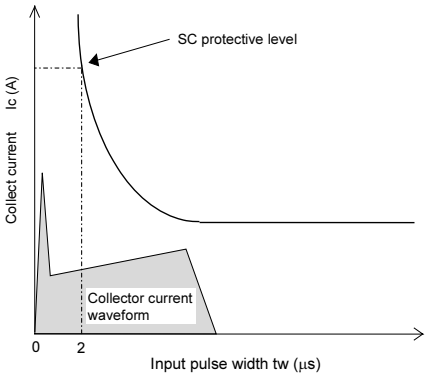


Fig.2-5 Filter time constant setting

SC protection (Lower-side only with the external shunt resistor and RC filter)

a1. Normal operation: IGBT ON and carrying current.
a2. Short circuit detection (SC trigger).
a3. IGBT gate hard interruption.
a4. IGBT turns OFF.
a5. Fo outputs (tFO(min)=20μs).
a6. Input = “L”. IGBT OFF.
a7. Input = “H”.
a8. IGBT OFF in spite of “H” input.

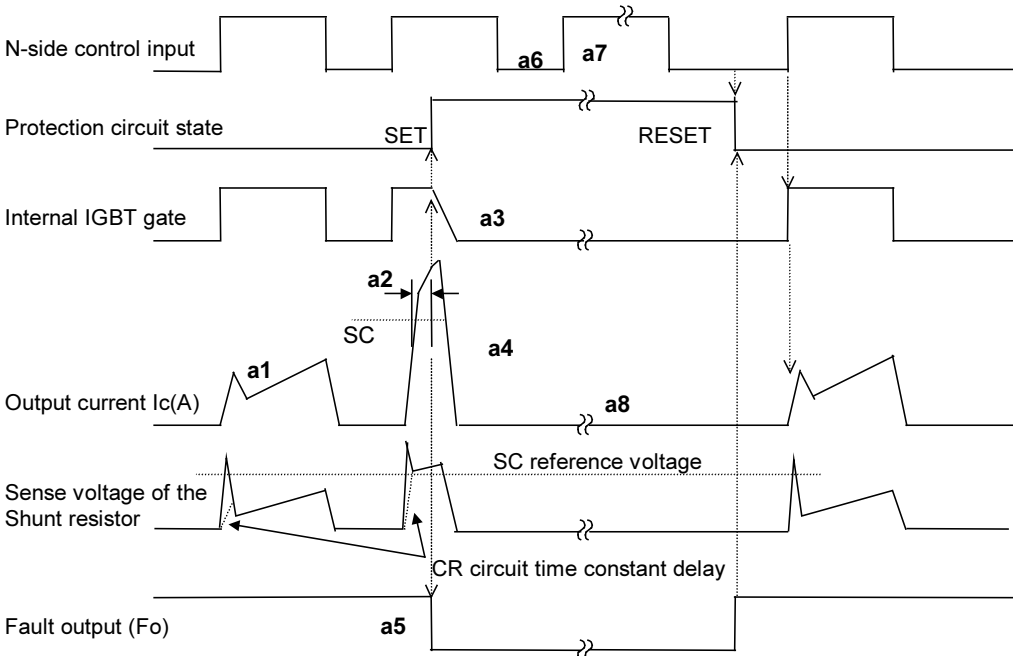


Fig.2-6 SC protection timing chart

2.2.2 Control Supply UV Protection

The UV protection is designed to prevent unexpected operating behavior as described in Table 2-7.

Both P-side and N-side have UV protecting function. However, fault signal (Fo) output only corresponds to N-side UV protection. Fo output continuously during UV state.

In addition, there is a noise filter (typ. 10μs) integrated in the UV protection circuit to prevent instantaneous UV erroneous trip. Therefore, the control signals are still transferred in the initial 10μs after UV happened.

Table 2-7 DIP-IPM operating behavior versus control supply voltage

Control supply voltage	Operating behavior
0-4.0V (P, N)	Equivalent to zero power supply. UV function is inactive, no Fo output. Normally IGBT does not work. But, external noise may cause DIP-IPM malfunction (turns ON), so DC-link voltage need to turn on after control supply turning on.
4.0-12.5V (P, N)	UV function become active and output Fo (N-side only). Even if control signals are applied, IGBT does not work
12.5-13.5V (P, N)	IGBT can work. However, conducting loss and switching loss will increase, and result extra temperature rise at this state,.
13.5-16.5V (N), 13.0-18.5V (P)	Recommended conditions.
16.5-20.0V (N),18.5-20.0V (P)	IGBT works. However, switching speed becomes fast and saturation current becomes large at this state, increasing SC broken risk.
20.0V- (P, N)	The control circuit will be destroyed.

Ripple Voltage Limitation of Control Supply

If high frequency noise superimposed to the control supply line, IC malfunction might happen and cause DIP-IPM erroneous operation. To avoid such problem happens, line ripple voltage should meet the following specifications:

$dV/dt \leq +/-1V/\mu s$, $Vripple \leq 2Vp\text{-}p$

N-side UV Protection Sequence

a1. Control supply voltage rising: After the voltage level reaches UV_{Dr}, the circuits start to operate when next input is applied.
a2. Normal operation : IGBT ON and carrying current.
a3. Under voltage trip (UV_{Dt}).
a4. IGBT OFF in spite of control input condition.
a5. Fo outputs(tFO ≥20μs and Fo outputs continuously during UV period.)
a6. Under voltage reset (UV_{Dr}).
a7. Normal operation : IGBT ON and carrying current.

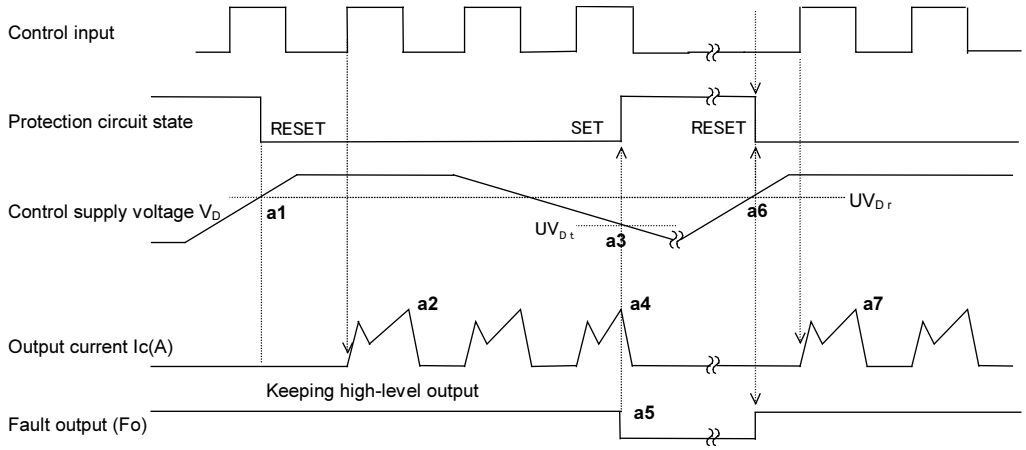


Fig.2-7 Timing chart of N-side UV protection

P-side UV Protection Sequence

a1. Control supply voltage rising : After the voltage reaches UV_{DBr}, the circuits start to operate when next input is applied.
a2. Normal operation : IGBT ON and carrying current.
a3. Under voltage trip (UV_{DBt}).
a4. IGBT OFF in spite of control input condition, but there is no Fo signal outputs.
a5. Under voltage reset (UV_{DBr}).
a6. Normal operation : IGBT ON and carrying current.

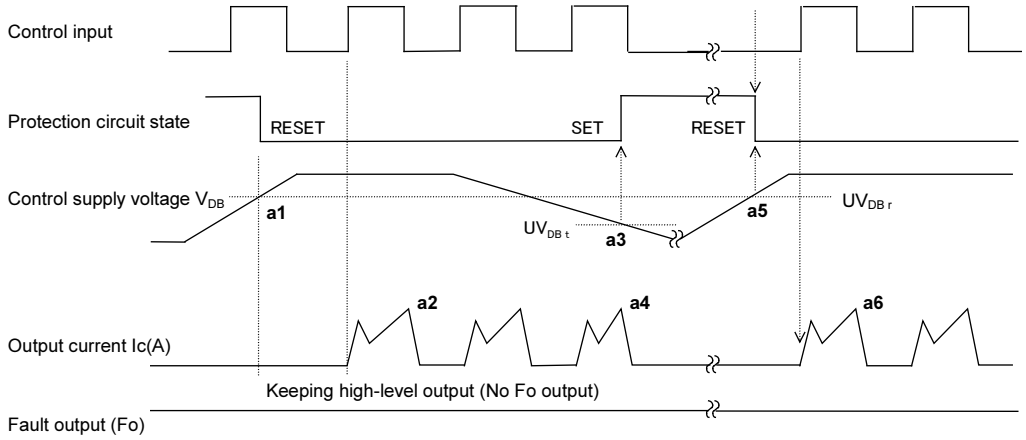


Fig.2-8 Timing Chart of P-side UV protection

2.2.3 OT Protection

PS2196X-T series have OT (over temperature) protection function by monitoring LVIC temperature rise.
While LVIC temp go over and keeps over OT trip temperature, error signal Fo outputs and all N-side IGBTs are shut down without reference to input signal. (P-side IGBTs are not shut down)

The specification of OT trip temp.and its sequence are described in Table 2-8 and Fig.2-9.

Table 2-8 OT trip temp. specification

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Over temperature protection (Note5)	OT_t	V_D=15V, At temperature of LVIC	Trip level	100	120	140	°C
	OT_{rh}		Trip/reset hysteresis	-	10	-	

OT Protection Sequence

a1. Normal operation : IGBT ON and carrying current
a2. LVIC temperature exceeds over temperature trip level(OT_t).
a3. IGBT OFF in spite of control input condition.
a4. Fo outputs during over temperature period, however, the minimum pulse width is 20μs.
a5. LVIC temperature becomes under over temperature reset level.
a6. Circuits start to operate normally when next input is applied.

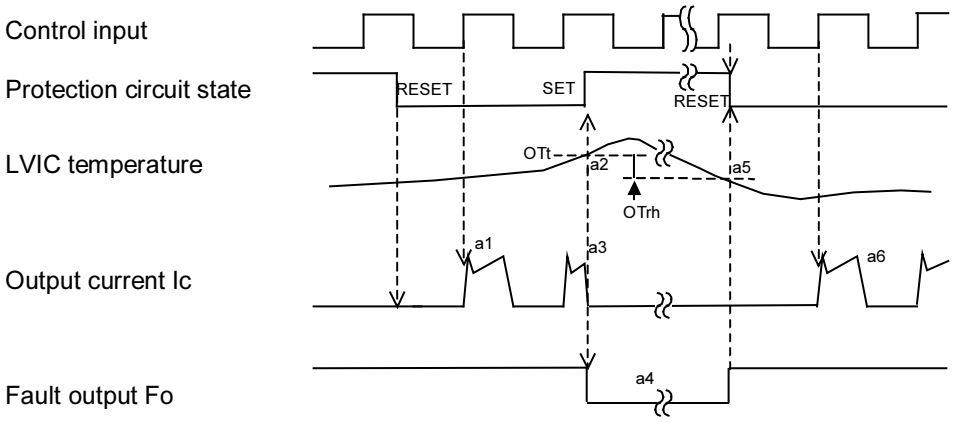


Fig.2-9 Timing Chart of OT protection

Precaution about this OT protection function

(1)This OT protection will not work effectively in the case of rapid temperature rise like motor lock or over current . (This protection monitors LVIC temperature, so it cannot respond to rapid temperature rise of power chips.)

(2)If the cooling system is abnormal state (e.g. heat sink comes off, fixed loosely, or cooling fun stops) when OT protection works, can't reuse the DIP-IPM . (Because the junction temperature of power chips will exceeded the maximum rating of Tj(150°C).)

2.3 Package Outlines

Super Mini DIP-IPM Ver.4 packages are developed with 5 types terminal shapes optional for different mounting requirement. There are short pin type (standard type), long pin type, control pin zigzag type, N-side IGBT open emitter type and both sides zigzag type with same size package.

2.3.1 Terminal frame change from previous series (PS2196X-XXX)

The terminal frame is changed to the shape shown in Fig.2-10. This change intends to increase the insulation distance between terminals with high voltage potential so as to ensure the electric space meet the Japanese PSE（Product Safety of Electric home appliance and materials）standard requirements of 2.5mm(min) for clearance and 3.0mm(min.) for creepage distance. Table 2-9 shows the location of the changes in terminal frame, and Table 2-10 shows a comparison of the insulation distance before and after change. However, there is no change in the pin assignment and pin pitch.

Table 2-9 Location of the change in terminal frame for Super Mini DIP-IPM Ver.4

	Changed location	Changed pins
(a)	Root shape of stopper terminal	Pin number 2, 3, 17, 18, 25
(b)	Space between roots of power terminals	Between pins of 21-22, 22-23 and 23-24

Table 2-10 Insulation distance between each pair terminals of Super Mini DIP-IPM Ver.4

	Clearance distance		Creepage distance	
	Previous	New	Previous	New
Between control terminals with high potential (Between pins of 2-3,3-4,4-5)	2.256mm(typ)	**2.5mm(min)**		
Between power terminals (Between pins of 21-22, 22-23, 23-24)			2.88mm(min)	**3.0mm(min)**

The insulation distances except for stated above already meet the PSE standard.

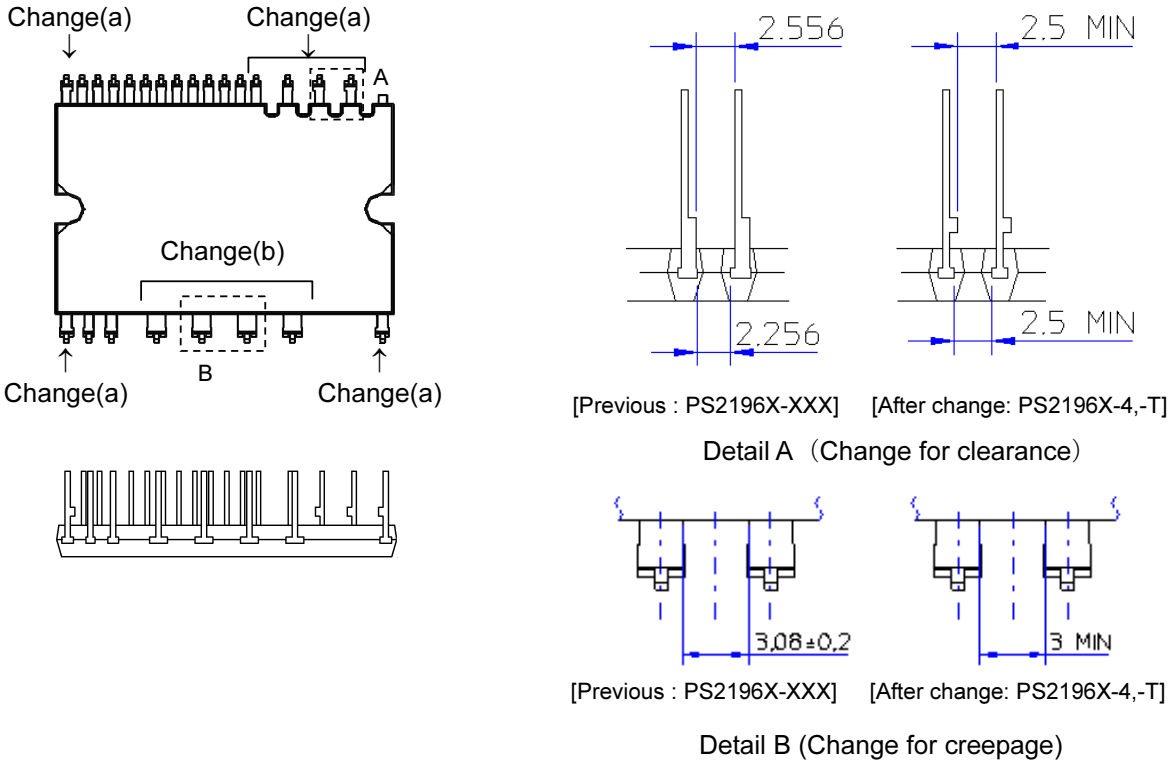


Fig.2-10 Locations of the change in the terminal frame shape

2.3.2 Short Pin Type Package Outline Drawing

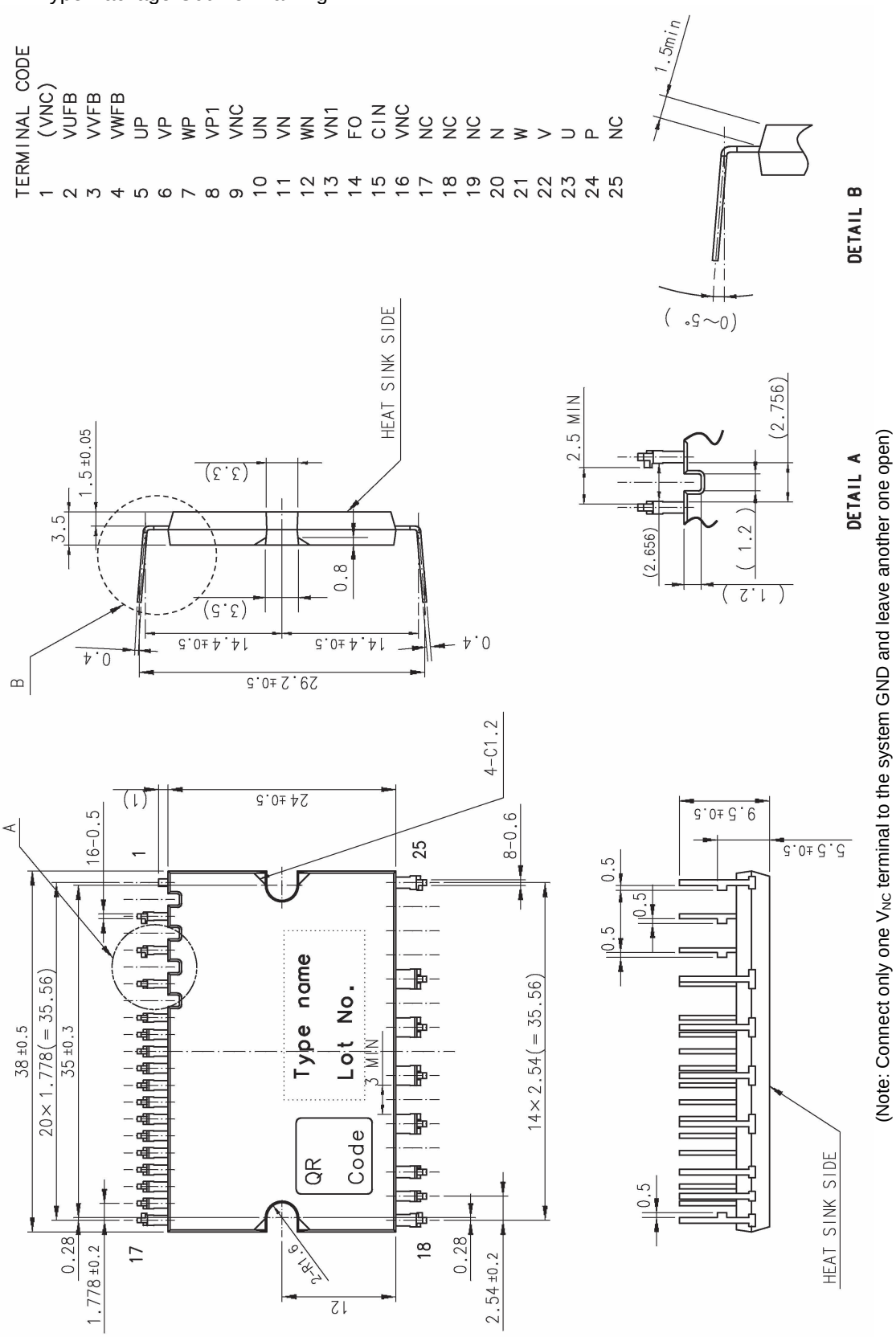


Fig.2-11 Short pin type package(-4/-T) outline drawing

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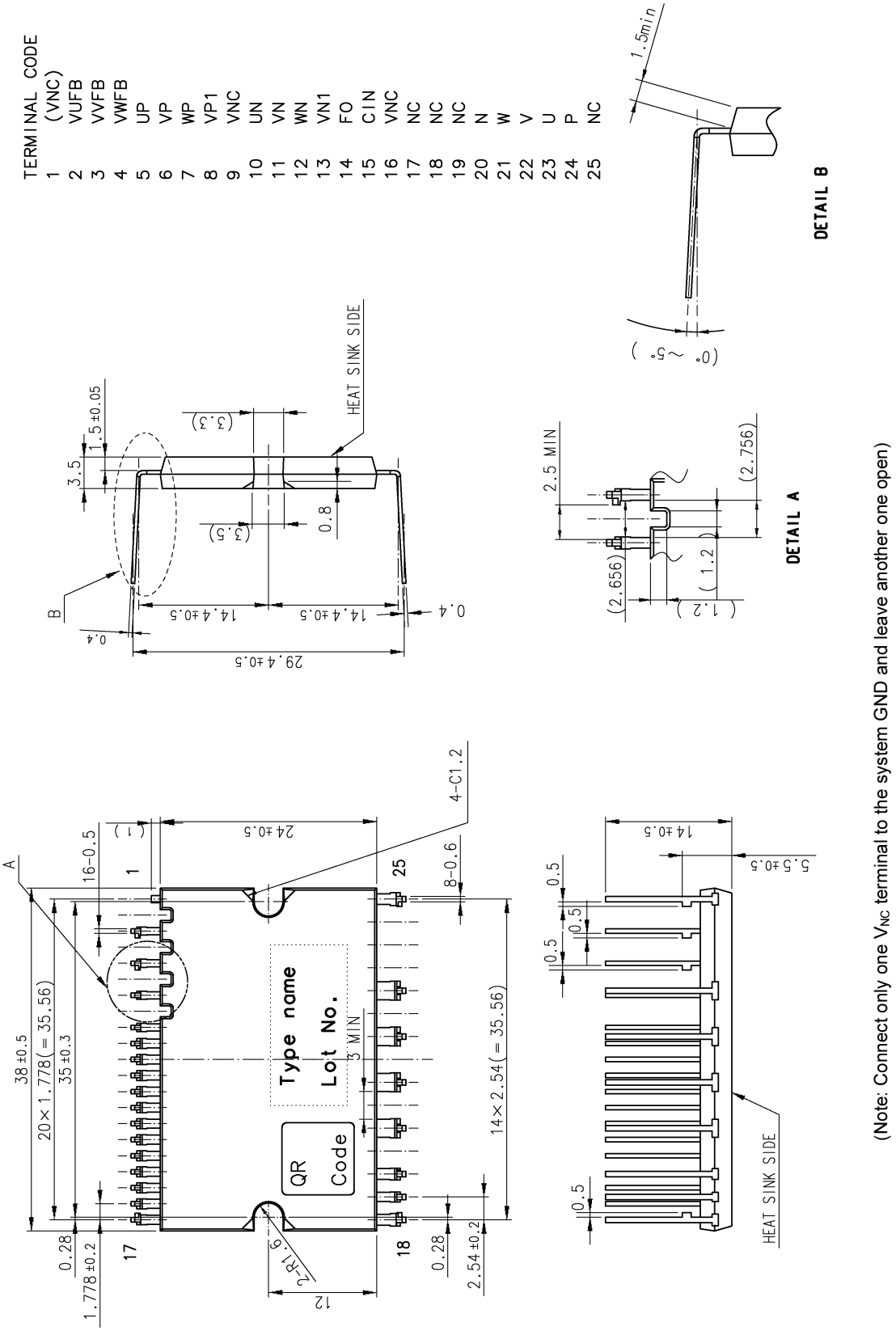
2.3.3 Long Pin Type Package Outline Drawing



(Note: Connect only one V_{NC} terminal to the system GND and leave another one open)

Fig.2-12 Long pin type package(-4A/-AT) outline drawing

2.3.4 Zigzag Pin Type Package Outline Drawing

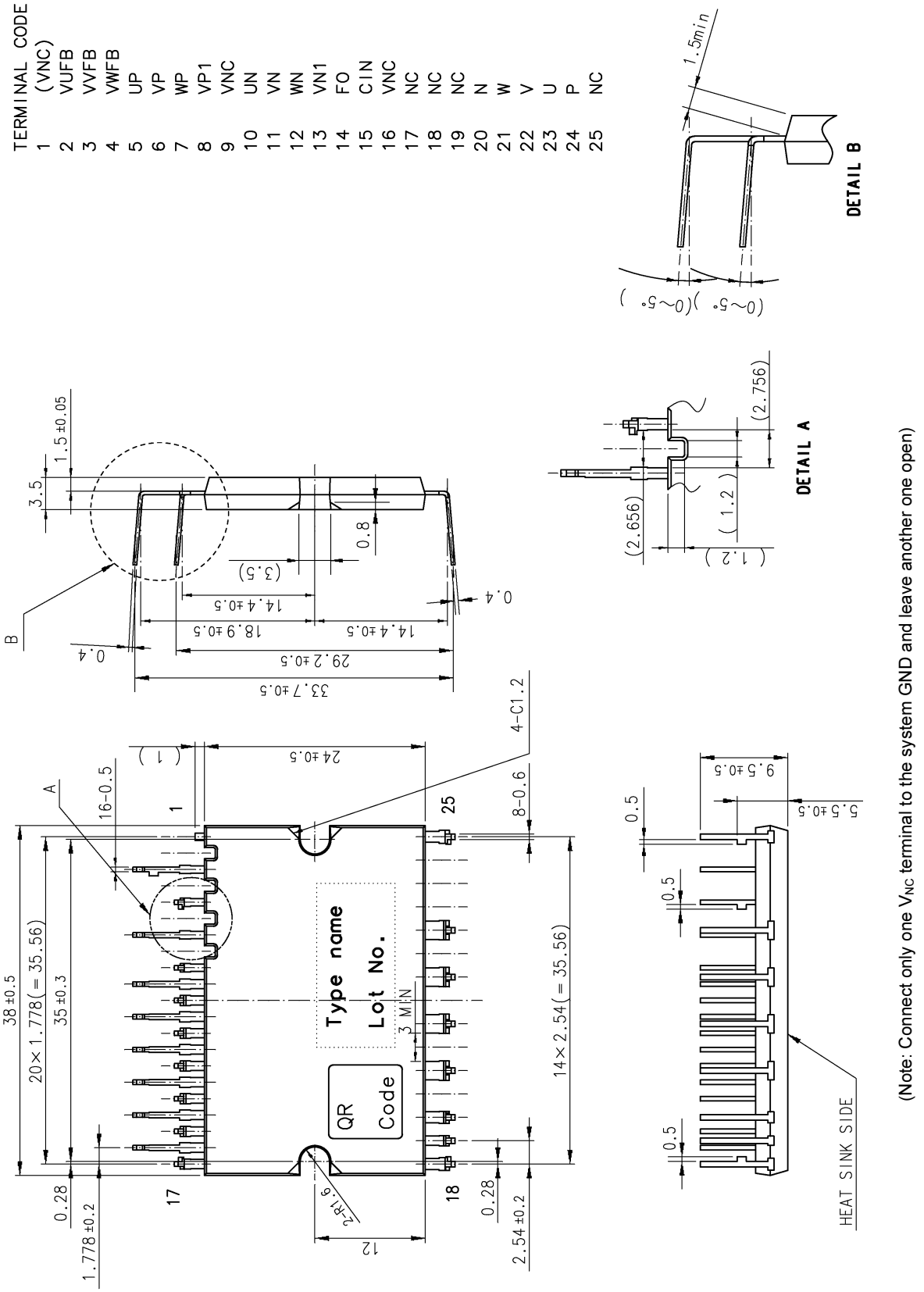
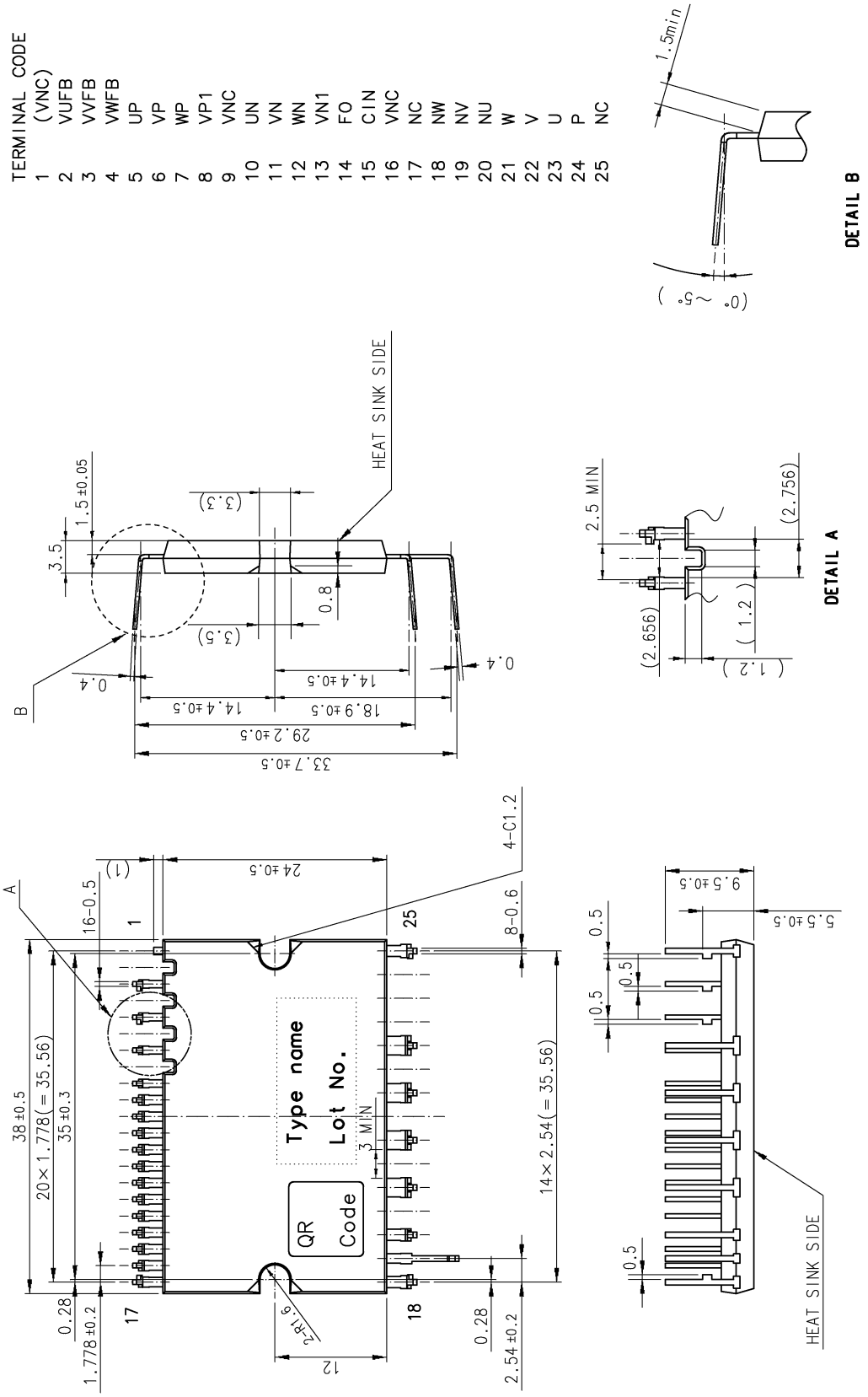


Fig.2-13 Zigzag pin type package(-4C/-CT) outline drawing

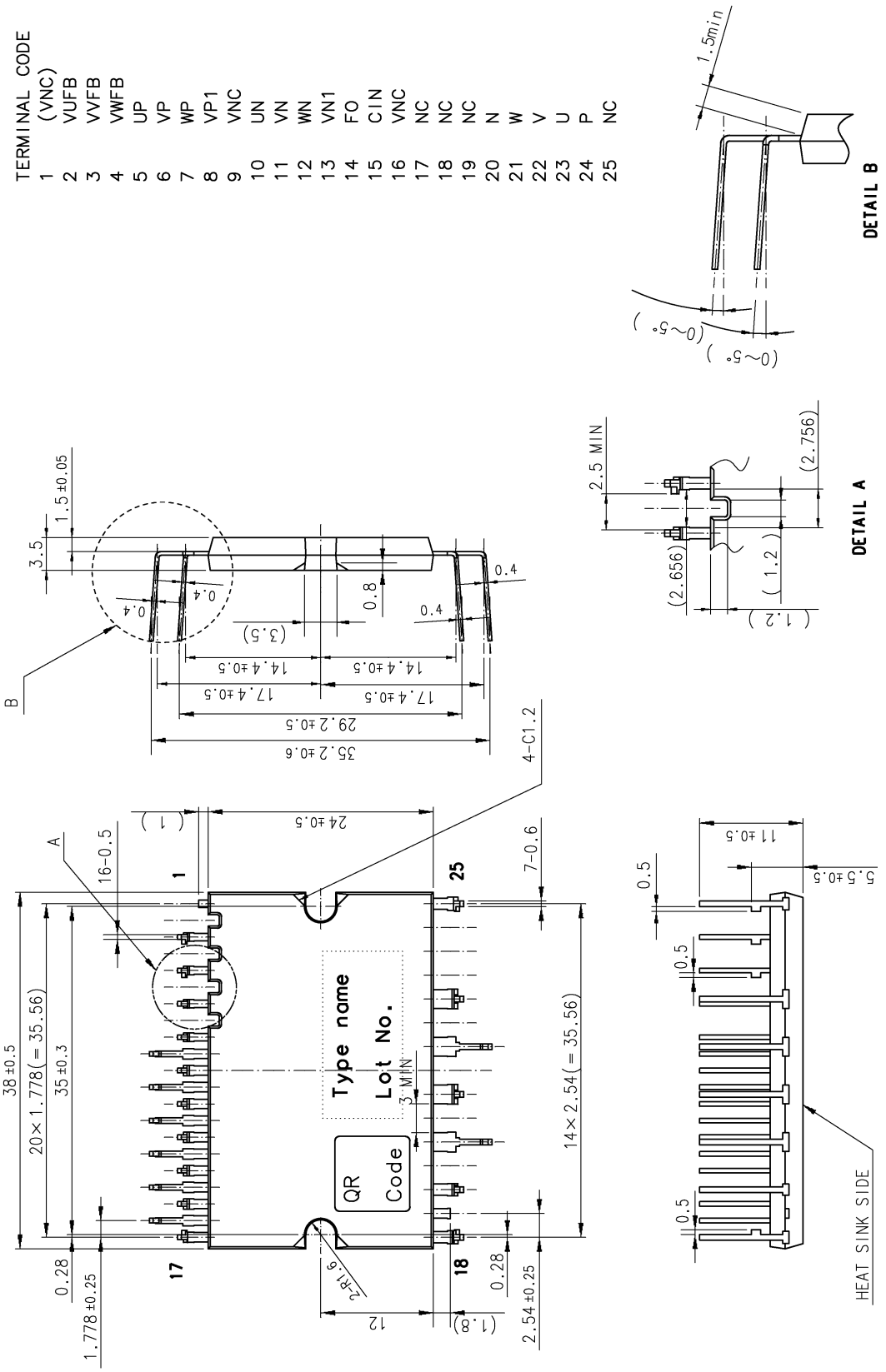
2.3.5 N-side Open Emitter Type Package Outline Drawing



(Note: Connect only one V_{NC} terminal to the system GND and leave another one open)

Fig.2-14 N-side open emitter type package(-4S/-ST) outline drawing

2.3.6 Both Sides Zigzag Pin Type Package Outline Drawing



(Note: Connect only one V_{NC} terminal to the system GND and leave another one open)

Fig.2-15 Both sides zigzag pin type package(-4W/-TW) outline drawing

2.3.7 Laser Marking

The laser marking specification of Super Mini DIP-IPM Ver.4 is described in Fig.2-16. Mitsubishi Corporation mark, Type name, Lot number, and QR code mark are marked in the upper side of module.

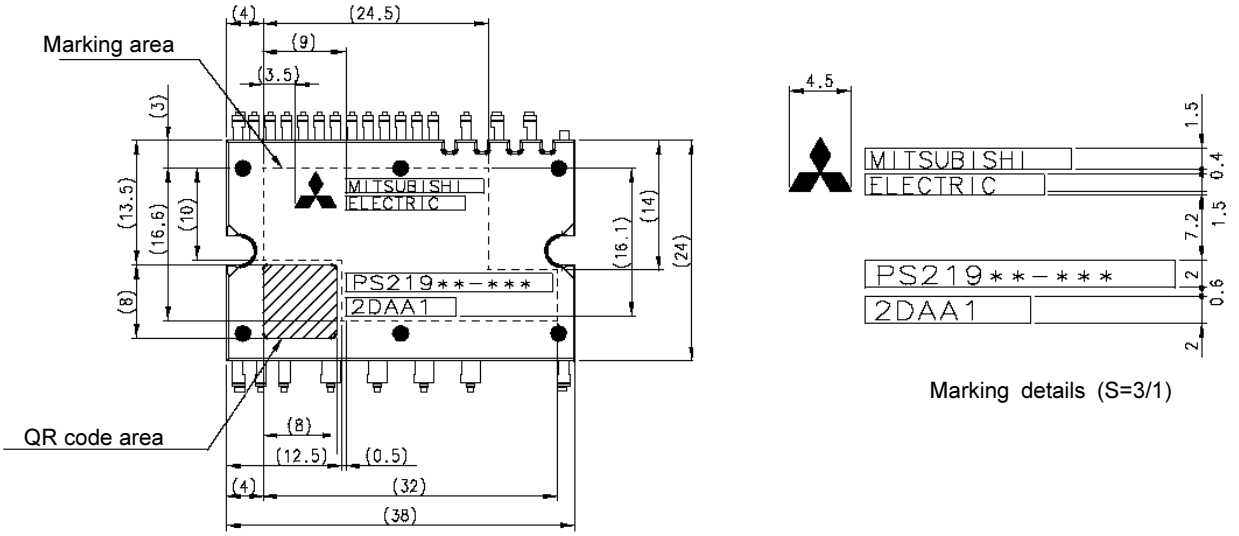


Fig.2-16 Laser marking view

2.3.8 Terminal Description

Table 2-11 Terminal description

Pin	Except for –S type		PS2196X-4S or -ST	
	Name	Description	Name	Description
1	NC	No connection	NC	Same in the left
2	V_{UFB}	U-phase P-side drive supply positive terminal	V_{UFB}	Same in the left
3	V_{VFB}	V-phase P-side drive supply positive terminal	V_{VFB}	Same in the left
4	V_{WFB}	W-phase P-side drive supply positive terminal	V_{WFB}	Same in the left
5	U_P	U-phase P-side control input terminal	U_P	Same in the left
6	V_P	V-phase P-side control input terminal	V_P	Same in the left
7	W_P	W-phase P-side control input terminal	W_P	Same in the left
8	V_{P1}	P-side control supply positive terminal	V_{P1}	Same in the left
9	V_{NC}*1	P-side control supply GND terminal	V_{NC}*1	Same in the left
10	U_N	U-phase N-side control input terminal	U_N	Same in the left
11	V_N	V-phase N-side control input terminal	V_N	Same in the left
12	W_N	W-phase N-side control input terminal	W_N	Same in the left
13	V_{N1}	N-side control supply positive terminal	V_{N1}	Same in the left
14	F_O	Fault signal output terminal	F_O	Same in the left
15	CIN	SC trip voltage detecting terminal	CIN	Same in the left
16	V_{NC}*1	N-side control supply GND terminal	V_{NC}*1	Same in the left
17	NC*2	No connection	NC*2	Same in the left
18	NC	No connection	NW	WN-phase IGBT emitter
19	NC	No connection	NV	VN-phase IGBT emitter
20	N	Inverter DC-link negative terminal	NU	UN-phase IGBT emitter
21	W	W-phase output terminal(W-phase drive supply GND)	W	Same in the left
22	V	V-phase output terminal (V-phase drive supply GND)	V	Same in the left
23	U	U-phase output terminal (U-phase drive supply GND)	U	Same in the left
24	P	Inverter DC-link positive terminal	P	Same in the left
25	NC	No connection	NC	Same in the left

*1) Connect only one V_{NC} terminal to the system GND and leave another one open.

*2) In the previous series, the V_{NO} terminal (17pin) needs to be connected externally to the V_{NC} terminal (16pin) on the PCB. But in this series, the V_{NO} terminal is changed to connect with V_{NC} terminal inside the module. So, the external wiring connection becomes no more needed. Furthermore, because there is no electric connection of this terminal (17pin) to other circuit inside the module, If the PCB which the 17pin is connected to 16pin(V_{NC}) is used, there is no any problem.

Table 2-12 Detailed description of input and output terminals

Item	Symbol	Description
P-side drive supply positive terminal P-side drive supply GND terminal	V_{UFB}-U V_{VFB}-V V_{WFB}-W Note 1	• Drive supply terminals for P-side IGBTs. • By virtue of applying the bootstrap circuit scheme, individual isolated power supplies are not needed for the DIP-IPM P-side IGBT drive. Each bootstrap capacitor is charged by the N-side V_D supply during ON-state of the corresponding N-side IGBT in the loop. • Abnormal operation might happen if the V_D supply is not aptly stabilized or has insufficient current capability. In order to prevent malfunction caused by such unstability as well as noise and ripple in supply voltage, a bypass capacitor with favorable frequency and temperature characteristics should be mounted very closely to each pair of these terminals. • Inserting a Zener diode (24V/1W) between each pair of control supply terminals is helpful to prevent control IC from surge destruction.
P-side control supply terminal N-side control supply terminal	V_{P1} V_{N1} Note 1	• Control supply terminals for the built-in HVIC and LVIC. • In order to prevent malfunction caused by noise and ripple in the supply voltage, a bypass capacitor with favorable frequency characteristics should be mounted very closely to these terminals. • Carefully design the supply so that the voltage ripple caused by noise or by system operation is within the specified minimum limitation. • It is recommended to insert a Zener diode (24V/1W) between each pair of control supply terminals to prevent surge destruction.
N-side control GND terminal	V_{NC} Note 2	• Control ground terminal for the built-in HVIC and LVIC. • Ensure that line current of the power circuit does not flow through this terminal in order to avoid noise influences.
Control input terminal	U_P,V_P,W_P U_N,V_N,W_N	• Control signal input terminals. • Voltage input type. These terminals are internally connected to Schmitt trigger circuit. • The wiring of each input should be as short as possible to protect the DIP-IPM from noise interference. • Use RC coupling in case of signal oscillation.
Short-circuit trip voltage detecting terminal	CIN	• Current sensing resistor should be connected between this terminal and V_{NC} to detect short-circuit accidents (short-circuit voltage trip level). Input impedance for CIN terminal is approximately 600kΩ. • RC filter should be connected for noise immunity.
Fault signal output terminal	F_O	• Fault signal output terminal. • This output is open drain type. F_O signal line should be pulled up to a 5V logic supply with approximately 10kΩ resistor.
Inverter DC-link positive terminal	P Note 1	• DC-link positive power supply terminal. • Internally connected to the collectors of all P-side IGBTs. • To suppress surge voltage caused by DC-link wiring or PCB pattern inductance, smoothing capacitor should be inserted very closely to the P and N terminal. It is also effective to add small film capacitor with good frequency characteristics.
Inverter DC-link negative terminal	N (Except Type '-S')	• DC-link negative power supply terminal (power ground) of the inverter. • This terminal is connected internally to the emitters of all N-side IGBTs.
	NU,NV,NW (for Type '-S')	• Open emitter terminal of each N-side IGBT • Usually, these terminals are connected to the power GND through individual shunt resistor.
Inverter power output terminal	U, V, W	• Inverter output terminals for connection to inverter load (e.g. AC motor). • Each terminal is internally connected to the intermidiate point of the corresponding IGBT half bridge arm.

Note: 1) Use oscilloscope to check voltage waveform of each power supply terminals and P&N terminals, the time division of OSC should be set to about 1μs/div. Please ensure the voltage (including surge) not exceed the specified limitation.

2) Connect only one V_{NC} terminal to the system GND, and leave another one open.

2.4 Mounting Method

This section shows the electric spacing and mounting precautions of Super Mini DIP-IPM Ver.4.

2.4.1 Electric Spacing

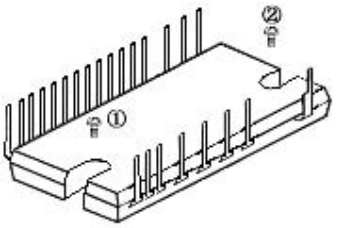
The electric spacing specification of Super Mini DIP-IPM Ver.4 is shown in Table 2-13

Table 2-13 Minimum insulation distance of Super Mini DIP-IPM Ver.4

	Clearance (mm)	Creepage (mm)
Between live terminals with high potential	2.50	3.00
Between terminals and heat sink	1.45	1.50

2.4.2 Mounting Method and Precautions

When installing a module to a heat sink, excessive uneven fastening force might apply stress to inside chips, which will lead to a broken or degradation of the device. An example of recommended fastening order is shown in Fig.2-17



Temporary fastening
1→2
Permanent fastening
1→2

Fig.2-17 Recommended screw fastening order

Note: Generally, the temporary fastening torque is set to 20-30% of the maximum torque rating.

Table 2-14. Mounting torque and heat sink flatness specifications

Item	Condition	Min.	Typ.	Max.	Unit
Mounting torque	Recommended 0.69N·m, Screw : M3	0.59	-	0.78	N·m
Flatness of heat radiation part	Heat radiation side of DIP-IPM package and External heat sink Refer Fig.2-18	-50	-	+100	μm

Note : Recommend to use plain washer (ISO7089-7094) in fastening the screws.

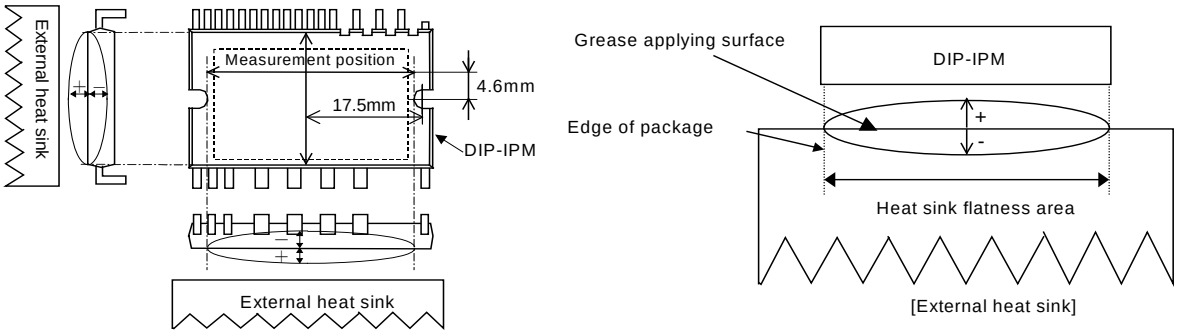


Fig.2-18 Measurement point of heat sink flatness

In order to get effective heat dissipation, it is necessary to enlarge the contact area as much as possible to minimize the contact thermal resistance. Regarding the heat sink flatness (warp/concavity and convexity) on the module installation surface (refer to Fig.2-18), the surface finishing-treatment should be within Rz12.

Evenly apply thermally-conductive grease with 100μ-200μm thickness over the contact surface between a module and a heat sink, which is also useful for preventing corrosion. Furthermore, the grease should be with stable quality and long-term endurance within wide operating temperature range. Use a torque wrench to fasten up to the specified torque rating. Exceeding the maximum torque limitation might cause a module damage or degrade. Also, pay attention not to have any desert remaining on the contact surface between the module and the heat sink.

CHAPTER 3 SYSTEM APPLICATION HIGHLIGHT

3.1 Application Guidance

This chapter states the Super Mini DIP-IPM Ver.4 application method and interface circuit design hints.

3.1.1 System connection

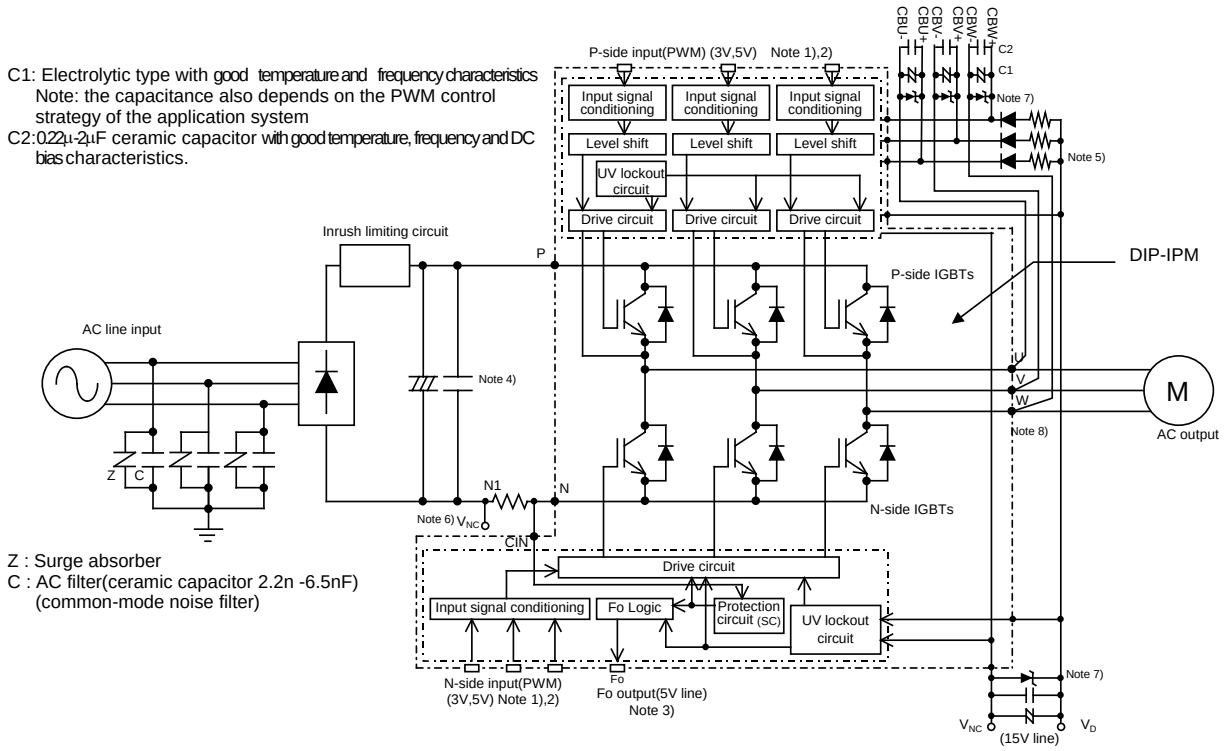


Fig.3-1 Application System block diagram of Super Mini DIP-IPM Ver.4 (except for type '-S')

Note 1) Input signal is high active logic. A 3.3kΩ(min.) pull down resistor is built-in each input circuit. If external RC filter is used for noise immunity, pay attention to the variation of the input signal level.

Note 2) By virtue of integrating HVIC inside the module, direct coupling to MCU/DSP without any opto-coupler or transformer for electric isolation is possible.

Note 3) Fo output is open drain type. This signal line should be pulled up to the positive side of a 5V supply with an approximate 10kΩ resistor.

Note 4) The wiring between the power DC-link capacitor and the P/N1 terminals should be as short as possible to protect DIP-IPM against catastrophic high surge voltage. For extra precaution, a small film type snubber capacitor (0.1μ~0.22μF, high voltage type) is recommended to mount closely to the P and N1 terminals.

Note 5) Use high-voltage (over 600V) and high-speed recovery diode for the bootstrap circuit.

Note 6) To prevent HVIC from surge destruction, it is recommended to insert a Zener diode (24V, 1W) between each control supply terminals.

Note 7) To prevent unexpected floating potential variation generated by extra wiring inductance and motor current, the negative electrodes of bootstrap supplies should be connected directly to DIP-IPM U, V, W terminals and separated from the main inverter output wires.

3.1.2 Interface Circuit (Direct Coupling Interface example except for type '-S')

Fig.3-2 shows a typical application circuit of interface schematic, in which control signals are transfered directly from a controller (MCU or DSP).

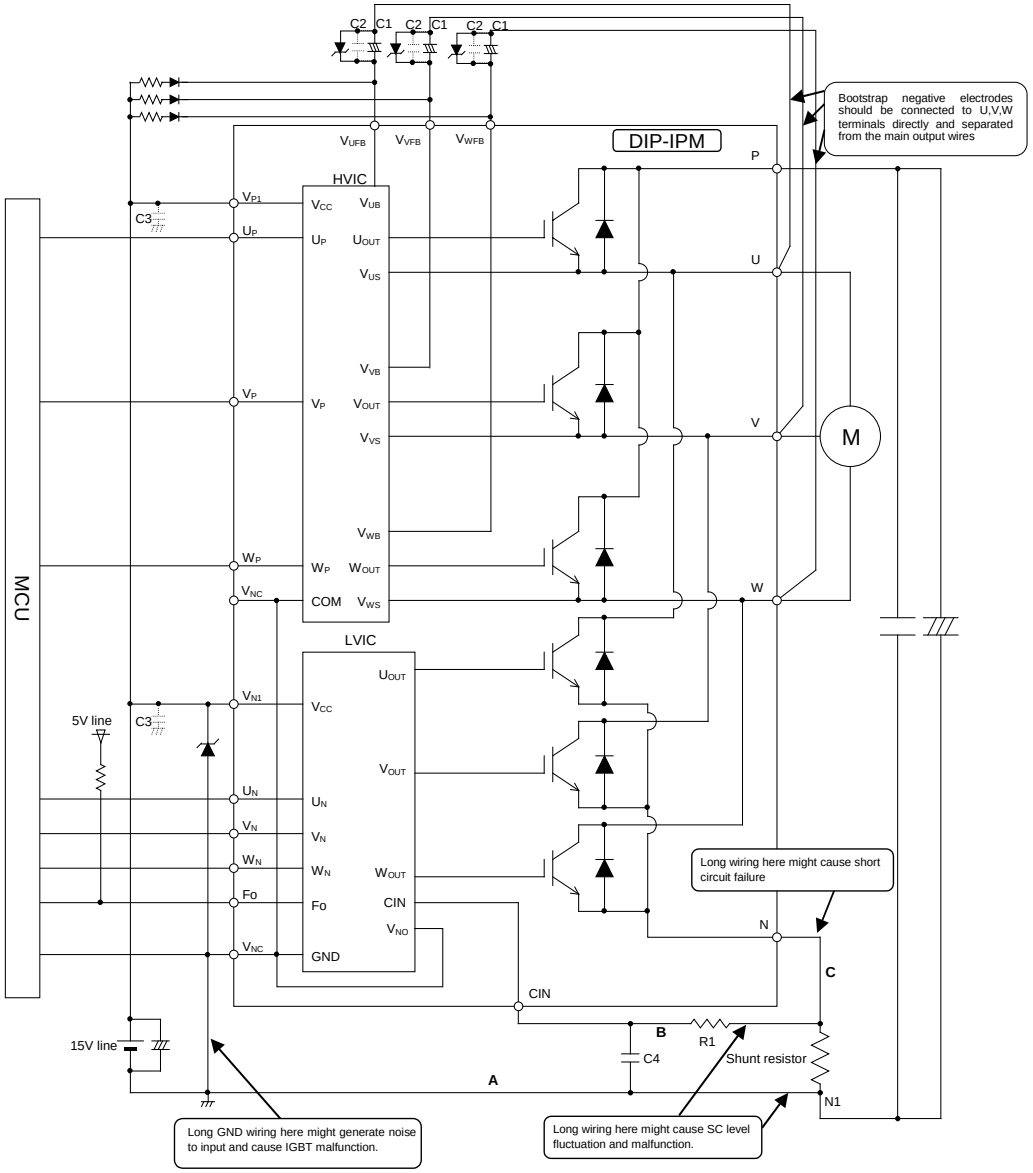


Fig.3-2 Interface circuit example except for type '-S'

Note:

(1) Input drive is High-Active type. There is a 3.3kΩ(min.) pull-down resistor integrated in the IC input circuit. To prevent malfunction, the wiring of each input should be as short as possible. When using RC coupling circuit, make sure the input signal level meet the turn-on and turn-off threshold voltage.

(2) Thanks to HVIC inside the module, direct coupling to MCU without any opto-coupler or transformer isolation is possible.

(3) Fo output is open drain type. It should be pulled up to the positive side of a 5V power supply by a resistor of about 10kΩ.

(4) To prevent erroneous protection, the wiring of A, B, C should be as short as possible.

(5) The time constant R1C4 of the protection circuit should be selected in the range of 1.5μ~2μs. SC interrupting time might vary due to the wiring pattern. Tight tolerance, temp-compensated type is recommended for R1,C4

(6) All capacitors should be mounted as close to the terminals of the DIP-IPM as possible. (C1: good temperature, frequency characteristic electrolytic type, and C2, C3 : good temperature, frequency and DC bias characteristic ceramic type are recommended.)

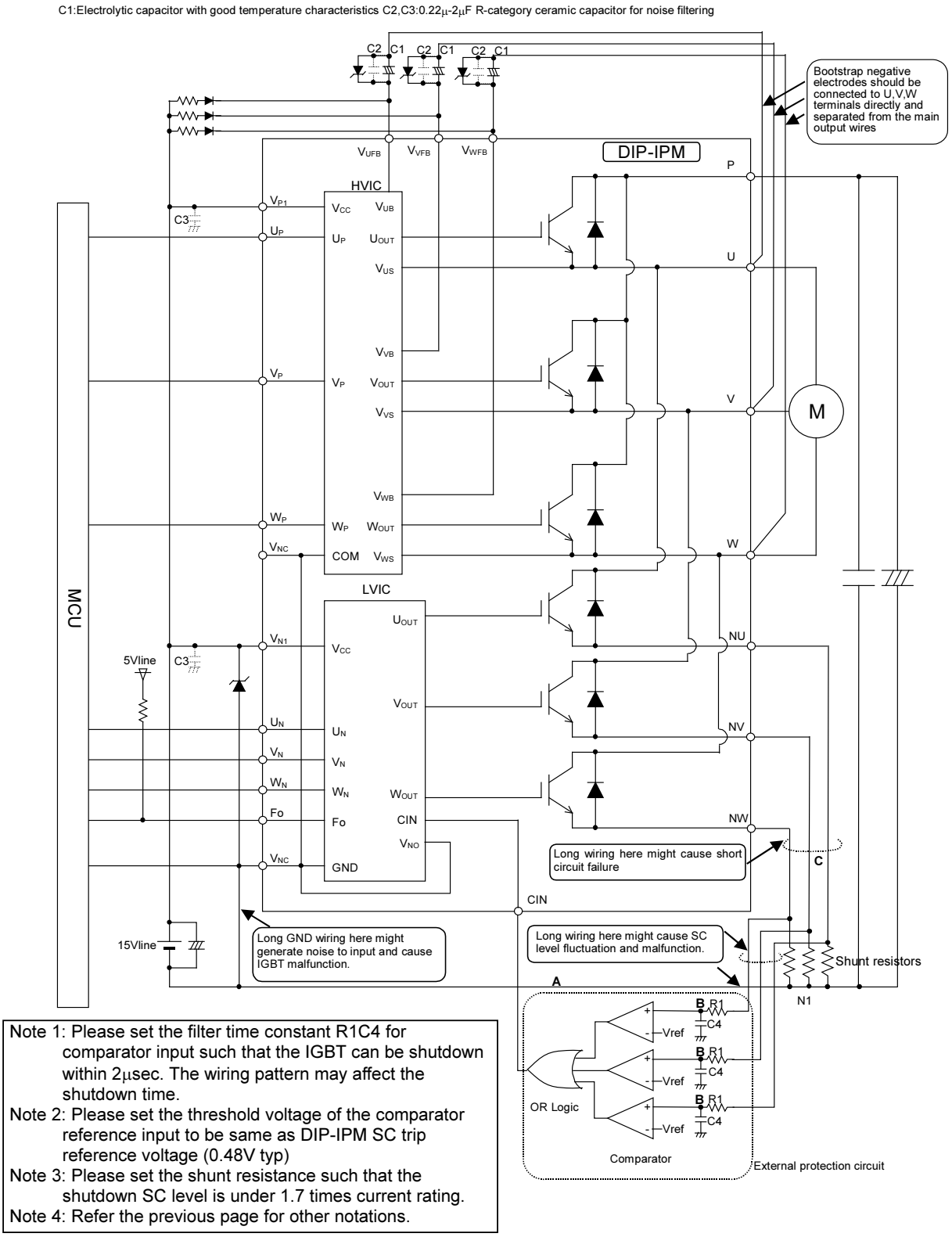
(7) To prevent surge destruction, the wiring between the smoothing capacitor and the P,N1 terminals should be as short as possible. Generally a 0.1μ~0.22μF snubber between the P-N1 terminals is recommended.

(8) Two VNC terminals (9 & 16 pin) are connected inside DIP-IPM, please connect either one to the 15V power supply GND outside and leave another one open.

(9) It is recommended to insert a Zener diode (24V/1W) between each pair of control supply terminals to prevent surge destruction.

(10) If control GND is connected to power GND by broad pattern, it may cause malfunction by power GND fluctuation. It is recommended to connect control GND and power GND at only a point.

3.1.3 Interface Circuit (Direct Coupling Interface Example for type '-S')



Note 1: Please set the filter time constant R1C4 for comparator input such that the IGBT can be shutdown within 2μsec. The wiring pattern may affect the shutdown time.
Note 2: Please set the threshold voltage of the comparator reference input to be same as DIP-IPM SC trip reference voltage (0.48V typ)
Note 3: Please set the shunt resistance such that the shutdown SC level is under 1.7 times current rating.
Note 4: Refer the previous page for other notations.

Fig.3-3 Interface circuit example for type '-S'

3.1.4 Interface Circuit (Opto-coupler Isolated Interface)

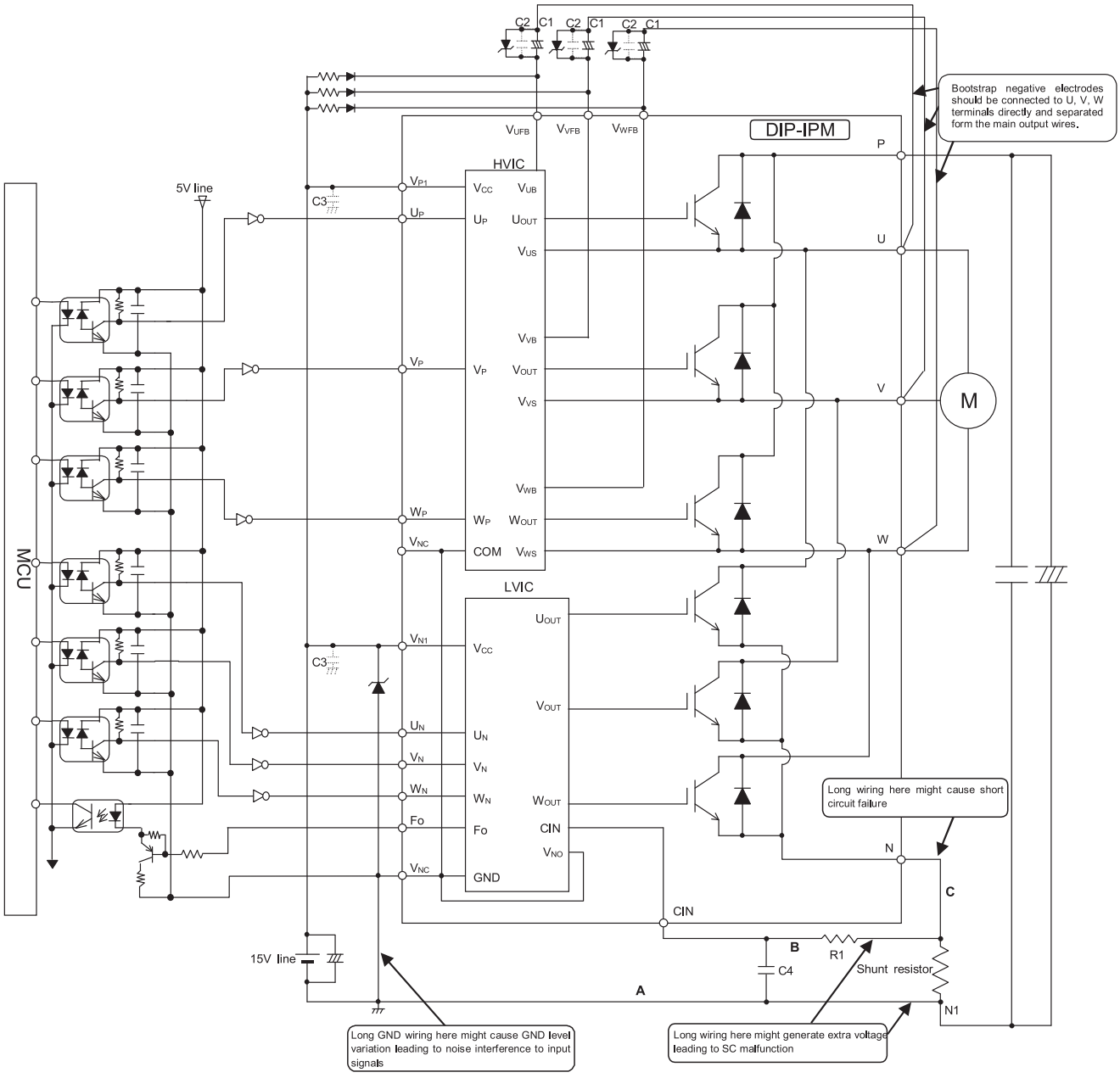


Fig.3-4 Interface circuit example except for type '-S'

Note 1: High speed (high CMR) opto-coupler is recommended;
2: Fo terminal sink current is 1mA. A buffer circuit is necessary to drive an opto-coupler.

3.1.5 Change into internal connection between V_{NO} and V_{NC} terminals

In the previous series, the V_{NO} terminal (17pin) needs to be connected externally to the V_{NC} terminal (16pin) on the PCB(Fig.3-5). But in this series, the V_{NO} terminal is changed to connect with V_{NC} terminal inside the module. (Fig.3-6) So, the external wiring connection becomes no more needed. Furthermore, because there is no electric connection of this terminal (17pin) to other circuit inside the module, If the PCB which the 17pin is connected to 16pin(V_{NC}) is used, there is no any problem.

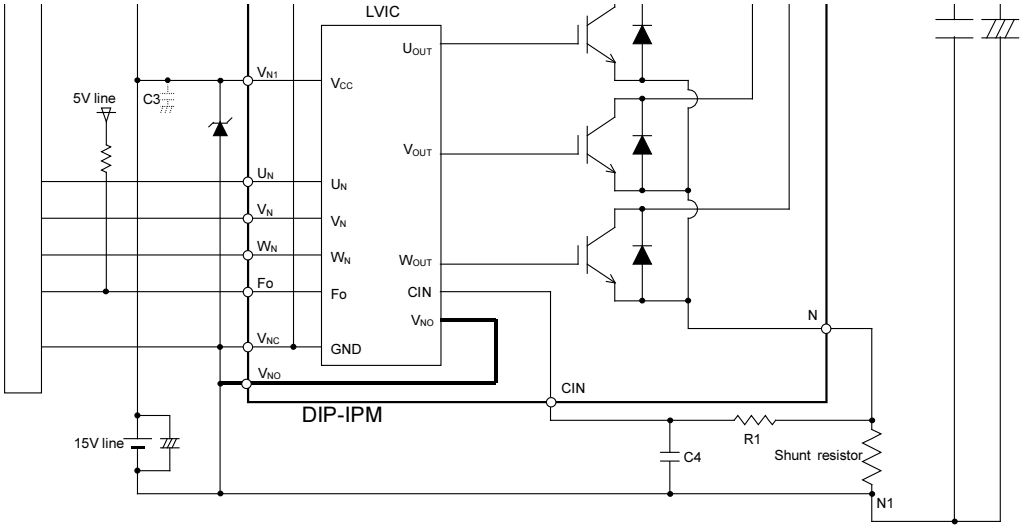


Fig.3-5 Previous series (PS2196X-XXX)

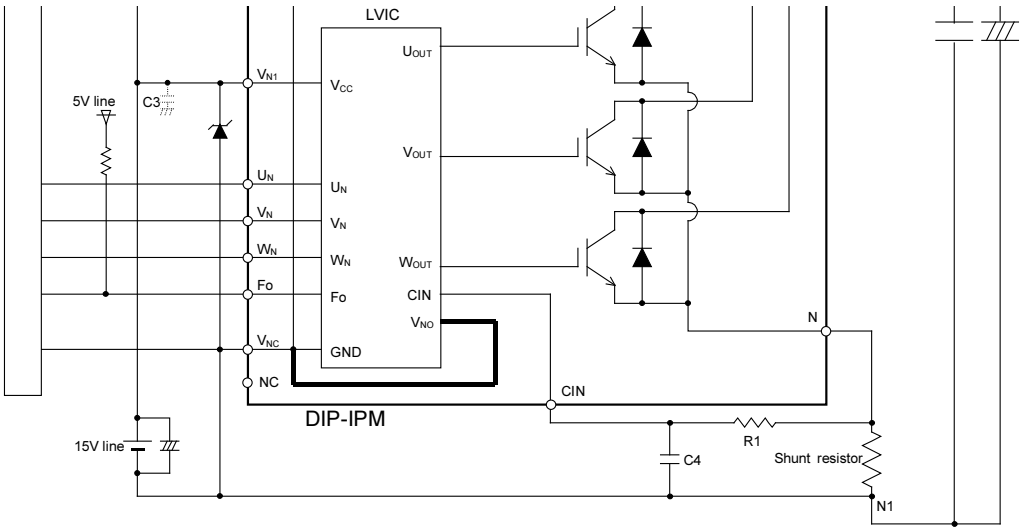


Fig.3-6 These series (PS2196X-4/-T)

3.1.6 Circuits of Signal Input terminals and Fo Terminal

(1) Internal Circuit of Control Input Terminals

Super Mini DIP-IPM Ver.4 series adopt High-Active input logic which released the sequence restriction between the control supply and the input signal in start-up or shut down operation, therefore, make the system fail-safe.

In addition, a 3.3kΩ(min) pull-down resistor is built-in each input circuit of the DIP-IPM as shown in Fig.3-7, hence, external pull-down resistor is not needed.

Furthermore, by lowering the turn on and turn off threshold value of input signal as shown in Table 3-1, a direct coupling to 3V-class microcomputer or DSP becomes possible.

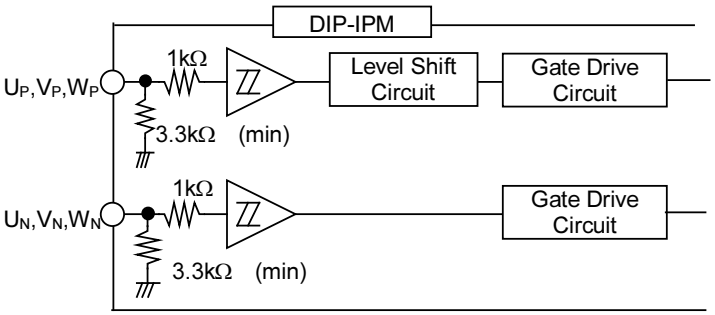


Fig.3-7. Internal structure of control input terminals

Table 3-1. Input threshold voltage ratings(Tj=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Turn-on threshold voltage	Vth(on)	U_P,V_P,W_P-V_{NC} terminals U_N,V_N,W_N-V_{NC} terminals	-	2.1	2.6	V
Turn-off threshold voltage	Vth(off)		0.8	1.3	-	
Threshold voltage hysterisis	Vth(hys)		0.35	0.65	-	

Note:There are limits for the minimum input pulse width in Super Mini DIP-IPM Ver.4. DIP-IPM might make no response or not work normally if the input signal pulse width (both on and off) is less than the limited value. Please refer to the datasheet for the specification.

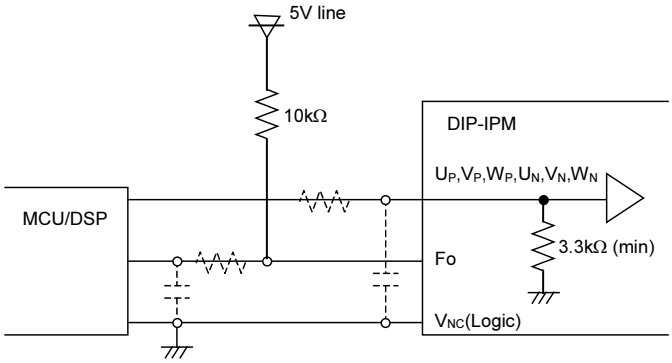


Fig.3-8 Control input connection

Note: The RC coupling (parts shown in the dotted line) at each input depends on user's PWM control strategy and the wiring impedance of the printed circuit board.
The DIP-IPM signal input section integrates a 3.3kΩ(min) pull-down resistor. Therefore, when using an external filtering resistor, please pay attention to the signal voltage drop at input terminal.

(2) Internal Circuit of Fo Terminal

F_O terminal is an open drain type, it should be pulled up to a 5V supply as shown in Fig.3-8. Fig.3-9 shows the typical V-I characteristics of Fo terminal. The maximum sink current of Fo terminal is 1mA. If opto-coupler is applied to this output, please pay attention to the opto-coupler drive ability.

Table 3-2 Electric characteristics of Fo terminal

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Fault output voltage	V_{FOH}	V_{SC}=0V,Fo=10kΩ,5V pulled-up	4.9	-	-	V
	V_{FOL}	V_{SC}=1V,Fo=1mA	-	-	0.95	V

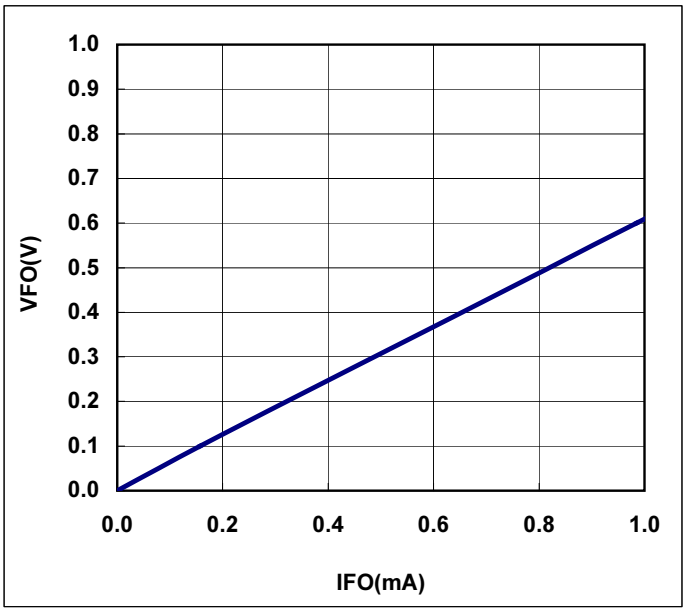


Fig.3-9 Fo terminal typical V-I characteristics (V_D=15V, T_j=25°C)

3.1.7 Snubber Circuit

In order to prevent DIP-IPM from extra surge destruction, the wiring length between the smoothing capacitor and DIP-IPM P-N terminals should be as short as possible. Also, a 0.1μ~0.22μF/630V snubber capacitor should be mounted in the DC-link close to DIP-IPM.

There are two positions ((1)or(2)) to mount a snubber capacitor as shown in Fig.3-10. Snubber capacitor should be installed in the position (2) so as to suppress surge voltage effectively. However, the charging and discharging currents generated by the wiring inductance and the snubber capacity will flow through the shunt resistor, which might cause erroneous protection if this current is large enough.

In order to suppress the surge voltage maximally, the wiring at part-A should be as short as possible when mounting a snubber capacitor outside the shunt resistor as shown in position (1). A better wiring example is shown in location (3).

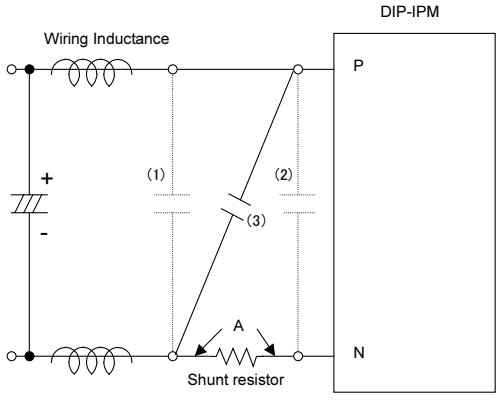
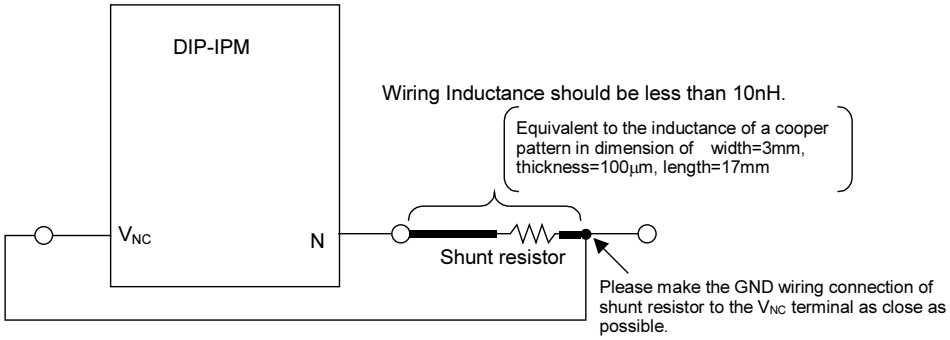


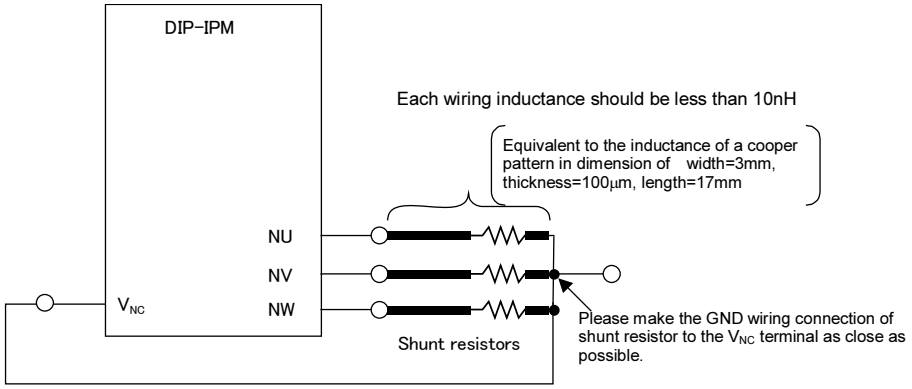
Fig.3-10 Recommended snubber circuit location

3.1.8 Recommended Wiring method around Shunt Resistor

External shunt resistor is employed to detect short-circuit accident. A longer wiring between the shunt resistor and DIP-IPM might cause so much large surge that might damage built-in IC. To decrease the pattern inductance, the wiring between the shunt and DIP-IPM should be as short as possible, and using low inductance type resistor such as SMT resistor instead of long-lead type resistor.



(a) Wiring instruction (except for type '-S')



(b) Wiring instruction for type '-S'

Fig.3-11 Recommended wiring method of shunt resistor

Influence of pattern wiring around the shunt resistor is shown below.

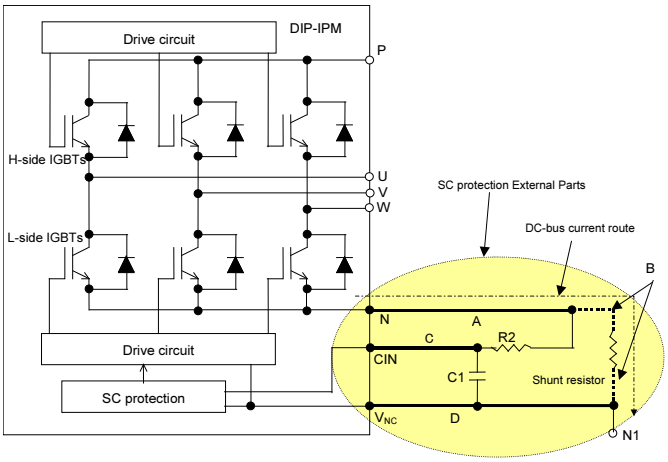


Fig.3-12 External protection circuit

(1) Influence of the part-A wiring

The ground of Low-side IGBT gate is V_{NC}. If part-A wiring pattern in Fig.3-12 is too long, extra voltage generated by the wiring parasitic inductor will result the potential of IGBT emitter variation during switching operation. Please install shunt resistor as close to the N terminal as possible.

(2) Influence of the part-B wiring

The part-B wiring affects SC protection level. SC protection works by judging the voltage of the CIN terminals. If part-B wiring is too long, extra surge voltage generated by the wiring inductance will lead to deterioration of SC protection level. Please connect CIN and V_{NC} terminals directly to the two ends of shunt resistor and avoid superfluous wiring.

(3) Influence of the part-C wiring pattern

C1R2 filter is added to remove noise influence occurring on shunt resistor. Filter effect will dropdown and noise will easily superimpose on the wiring if part-C wiring is too long. Please install the C1R2 filter near CIN, V_{NC} terminals as close as possible.

(4) Influence of the part-D wiring pattern

Part-D wiring pattern gives influence to all the items described above, maximally shorten the GND wiring is expected.

3.1.9 Precaution for wiring on PCB

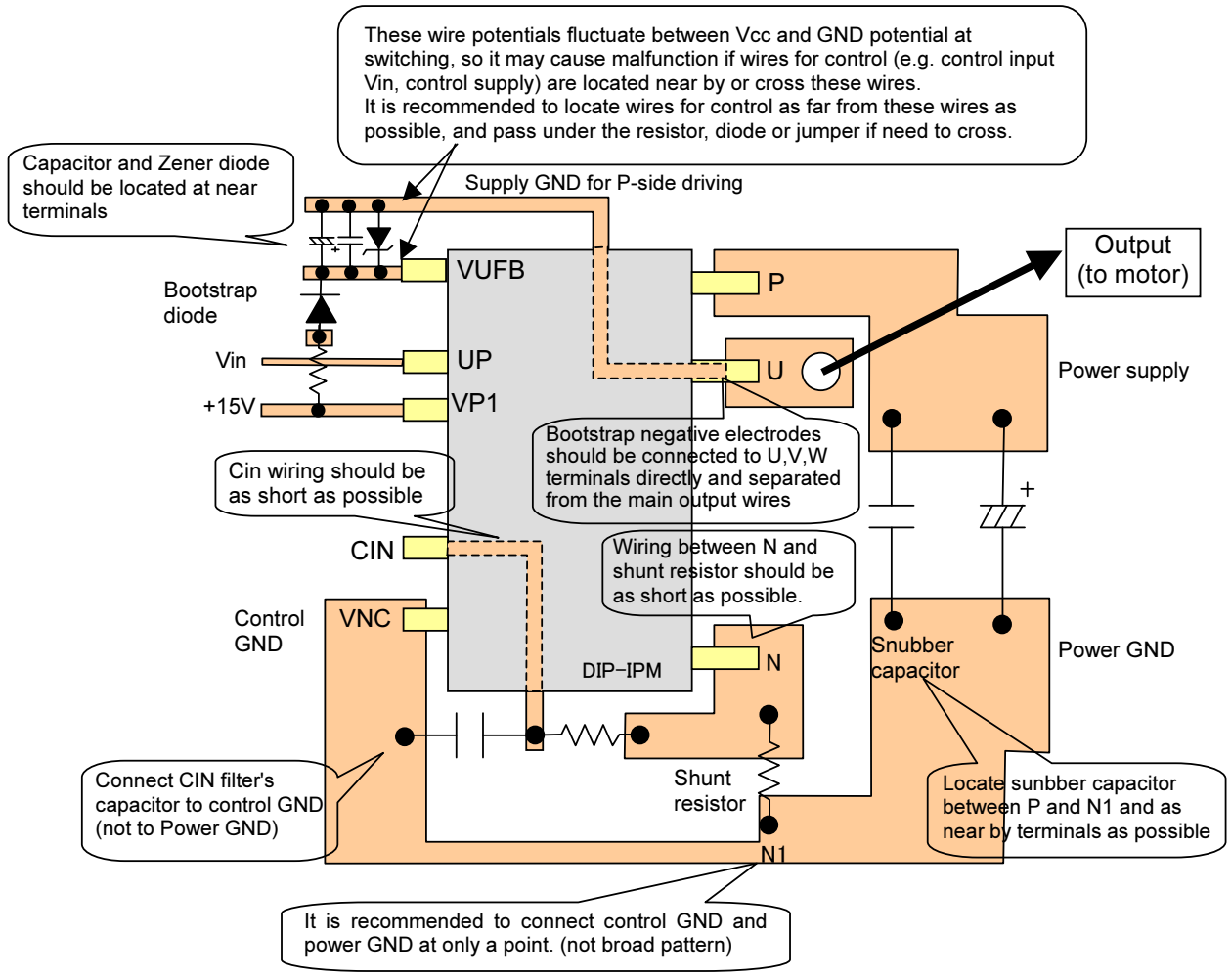


Fig.3-13 Precaution for wiring on PCB

3.1.10 SOA of Super Mini DIP-IPM Ver.4

The following describes the SOA (Safety Operating Area) of the Super Mini DIP-IPM Ver.4.

V_{CES} : Maximum rating of IGBT collector-emitter voltage

V_{CC} : Supply voltage applied on P-N terminals

$V_{CC(surge)}$: The total amount of V_{CC} and the surge voltage generated by the wiring inductance and the DC-link capacitor.

$V_{CC(PROT)}$: DC-link voltage that DIP-IPM can protect itself.

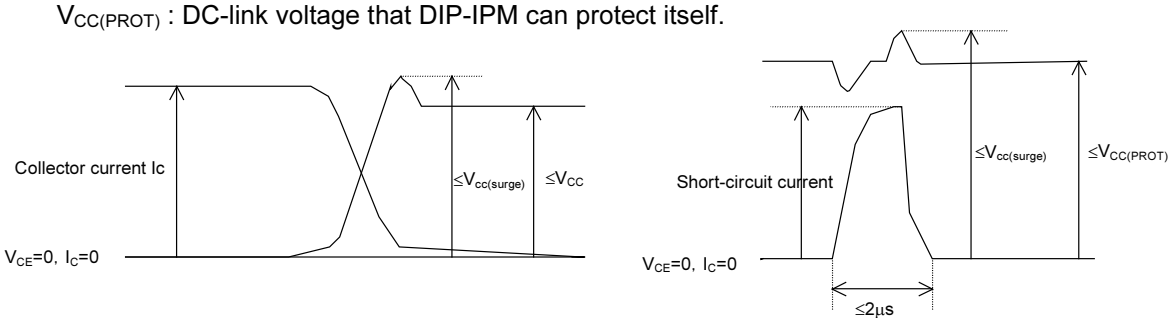


Fig.3-14 SOA at switching mode and short-circuit mode

In Case of switching

V_{CES} represents the maximum voltage rating (600V) of the IGBT. By subtracting the surge voltage (100V or less) generated by internal wiring inductance from V_{CES} is $V_{CC(surge)}$, that is 500V. Furthermore, by subtracting the surge voltage (50V or less) generated by the wiring inductor between DIP-IPM and DC-link capacitor from $V_{CC(surge)}$ derives V_{CC}, that is 450V.

In Case of Short-circuit

V_{CES} represents the maximum voltage rating (600V) of the IGBT . By Subtracting the surge voltage (100V or less) generated by internal wiring inductor from V_{CES} is $V_{CC(surge)}$, that is, 500V. Furthermore, by subtracting the surge voltage (100V or less) generated by the wiring inductor between the DIP-IPM and the electrolytic capacitor from $V_{CC(surge)}$ derives V_{CC}, that is, 400V.

3.1.11 Power Life Cycles

When DIP-IPM is in operation, repetitive temperature variation will happens on the IGBT junctions (ΔTj). The amplitude and the times of the junction temperature variation affect the device lifetime.

Fig.3-15 shows the IGBT power cycle curve as a function of average junction temperature variation (ΔTj).

(The curve is a regression curve based on 3 points of ΔTj=46, 88, 98°C with regarding to failure rate of 0.1%, 1% and 10%. These data are obtained from the reliability test of intermittent conducting operation)

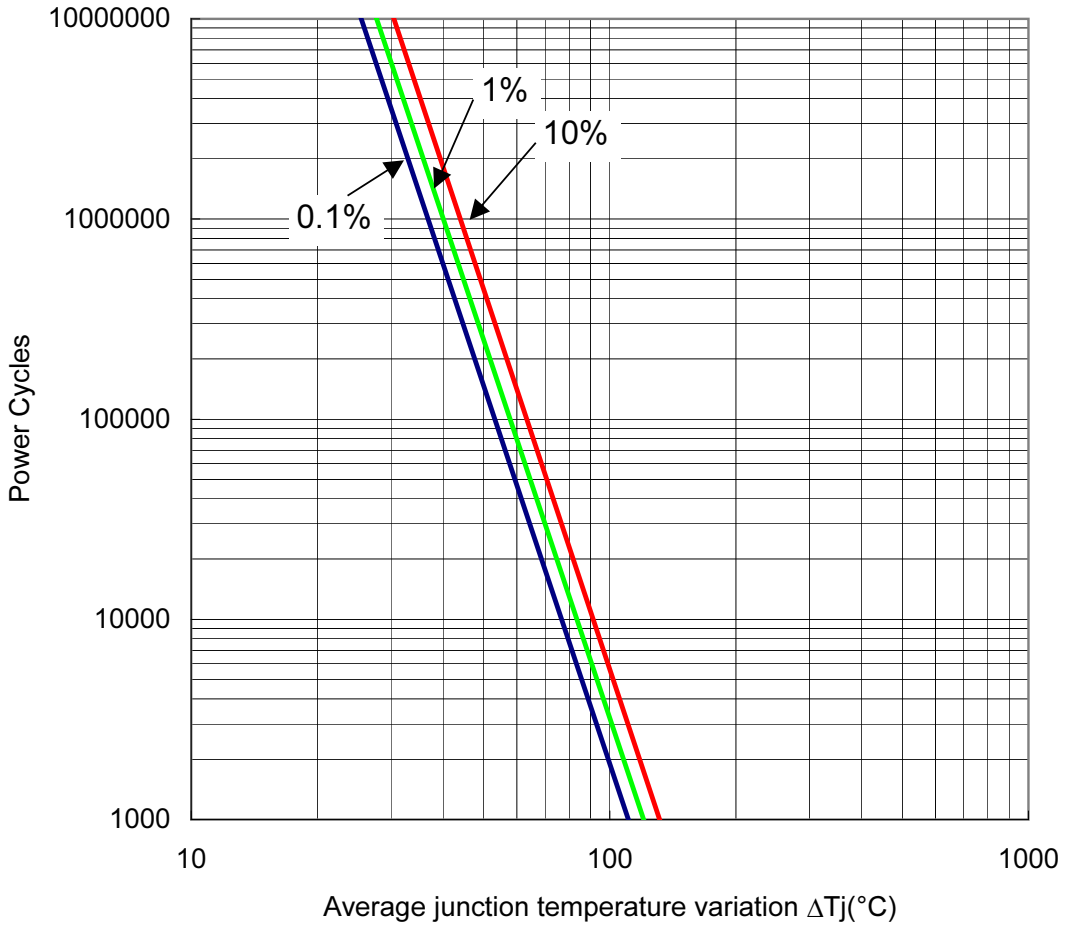


Fig.3-15 Power cycle curve

3.2 Power Loss and Thermal Dissipation Calculation

3.2.1 Power Loss Calculation

Simple expressions for calculating average power loss are given below:

● Scope

The power loss calculation intends to provide users a way of selecting a matched power device for their VVVF inverter application. However, it is not expected to use for limit thermal dissipation design.

● Assumptions

(1) PWM controlled VVVF inverter with sinusoidal output;
(2) PWM signals are generated by the comparison of sine waveform and triangular waveform.
(3) Duty amplitude of PWM signals varies between $\frac{1-D}{2} \sim \frac{1+D}{2}$ (%/100), (D: modulation depth).
(4) Output current various with Icp·sinx and it does not include ripple.
(5) Power factor of load output current is cosθ, ideal inductive load is used for switching.

● Expressions Derivation

PWM signal duty is a function of phase angle x as $\frac{1+\mathrm{D}\times\sin\mathrm{x}}{2}$ which is equivalent to the output voltage variation. From the power factor cosθ, the output current and its corresponding PWM duty at any phase angle x can be obtained as below:

$$Output\ \ current = Icp \times \sin x$$
$$PWM\ \ \ Duty = \frac{1 + D \times \sin(x + \theta)}{2}$$

Then, $V_{CE(sat)}$ and V_{EC} at the phase x can be calculated by using a linear approximation:

$$Vce(sat) = Vce(sat)(@\, Icp \times \sin x)$$
$$Vec = (-1) \times Vec(@\, Iecp(= Icp) \times \sin x)$$

Thus, the static loss of IGBT is given by:

$$\frac{1}{2\pi}\int_0^{\pi} (Icp \times \sin x) \times Vce(sat)(@\, Icp \times \sin x) \times \frac{1 + D\sin(x + \theta)}{2} \bullet dx$$

Similarly, the static loss of free-wheeling diode is given by:

$$\frac{1}{2\pi}\int_{\pi}^{2\pi} ((-1) \times Icp \times \sin x)((-1) \times Vec(@\, Icp \times \sin x) \times \frac{1 + D\sin(x + \theta)}{2} \bullet dx$$

On the other hand, the dynamic loss of IGBT, which does not depend on PWM duty, is given by:

$$\frac{1}{2\pi}\int_0^{\pi} (Psw(on)(@\, Icp \times \sin x) + Psw(off)(@\, Icp \times \sin x)) \times fc \bullet dx$$

FWDi recovery characteristics can be approximated by the ideal curve shown in Fig.3-16, and its dynamic loss can be calculated by the following expression:

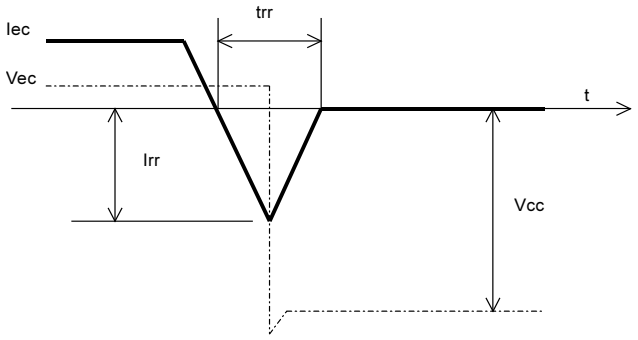


Fig.3-16 Ideal FWDi recovery characteristics curve

$$Psw = \frac{Irr \times Vcc \times trr}{4}$$

Recovery occurs only in the half cycle of the output current, thus the dynamic loss is calculated by:

$$\frac{1}{2}\int_{\pi}^{2\pi} \frac{Irr(@Icp \times \sin x) \times Vcc \times trr(@Icp \times \sin x)}{4} \times fc \bullet dx$$

$$= \frac{1}{8}\int_{\rho}^{2\pi} Irr(@Icp \times \sin x) \times Vcc \times trr(@Icp \times \sin x) \times fc \bullet dx$$

- Attention of applying the power loss simulation for inverter designs
  - Divide the output current period into fine-steps and calculate the losses at each step based on the actual values of PWM duty, output current, $V_{CE(sat)}$, V_{EC}, and Psw corresponding to the output current. The worst condition is most important.
  - PWM duty depends on the signal generating way.
  - The relationship between output current waveform or output current and PWM duty changes with the way of signal generating, load, and other various factors. Thus, calculation should be carried out on the basis of actual waveform data.
  - $V_{CE(sat)}$,V_{EC} and Psw(on, off) should be the values at Tj=125°C.

3.2.2 Temperature Rise Considerations and Calculation Example

Fig.3-17 shows the typical characteristics of allowable motor rms current versus carrier frequency under the following inverter operating conditions based on power loss simulation results.

Conditions: V_{CC}=300V, V_D=V_{DB}=15V, $V_{CE(sat)}$=Typ., Switching loss=Typ., Tj=125°C, Tf=100°C, Rth(j-f)=Max., Rth(c-f)=0.3°C/W (per 1/6 module), P.F=0.8, 3-phase PWM modulation, 60Hz sine waveform output

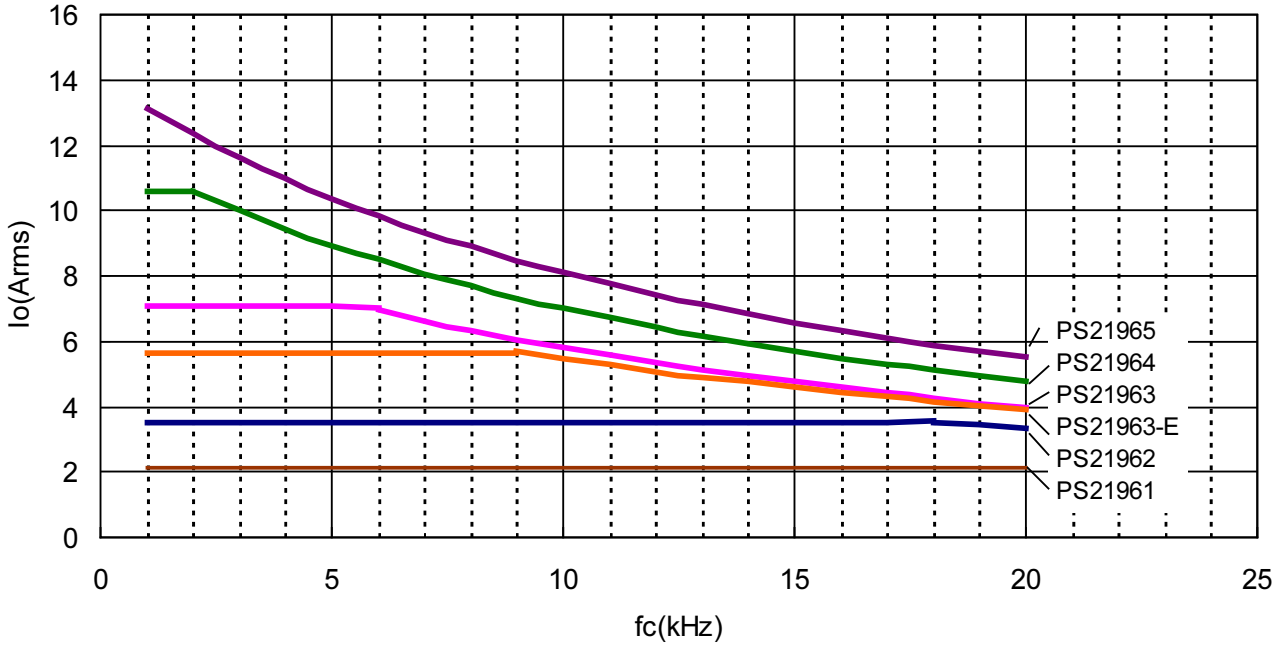


Fig.3-17. Effective current-carrier frequency characteristics

Fig.3-17 shows an example of estimating allowable inverter output rms current under different carrier frequency and permissible maximum operating temperature condition (Tf=100°C. Tj=125°C). The results may change for different control strategy and motor types. Anyway please ensure that there is no large current over device rating flowing continuously.

The allowable motor current can also be obtained from the free power loss simulation software provided by Mitsubishi electric on its web site (URL: http://www.mitsubishichips.com/).

3.3 Noise Withstand Capability

3.3.1 Evaluation Circuit

Super Mini DIP-IPM Ver.4 series have been confirmed to be with over +/-2.0kV noise withstand capability by the noise evaluation under the conditions shown in Fig.3-18. However, noise withstand capability greatly depends on the test environment, the wiring patterns of control substrate, parts layout, and other factors; therefore an additional confirmation on prototype is necessary.

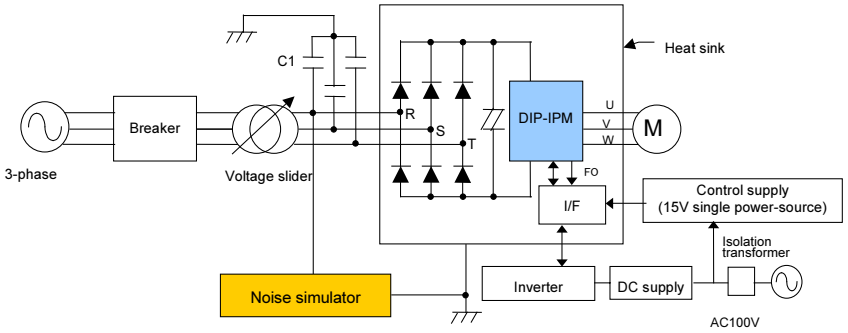


Fig.3-18 Noise withstand capability evaluation circuit

Note:

C1: AC line common-mode filter 4700pF
PWM signals are inputted from microcomputer both directly and through opto-coupler
15V single power supply
Test is performed with both IM and DCBLM motors

Test conditions

V_{CC}=300V, V_D=15V, Ta=25°C, no load
Scheme of applying noise : From AC line (R, S, T), Period T=16ms, Pulse width tw=0.05-1μs, input in random.

3.3.2 Countermeasures and Precautions

DIP-IPM improves noise withstand capabilities by means of reducing parts quantity, lowering internal wiring parasitic inductance, and reducing leakage current.

For malfunction caused by external noise, please consider the following countermeasures:

(1) Improving power supply filtering (close to DIP-IPM terminals)
(2) Lowering impedance of input parts (reducing pull-up resistance)
(3) Connecting filter between input parts and GND (bypassing noise)

3.3.3 Static Electricity Withstand Capability

Super Mini DIP-IPM Ver.4 series have been confirmed to be with +/-200V or more withstand capability against static electricity from the following tests shown in Fig.3-19 and Fig.3-20.

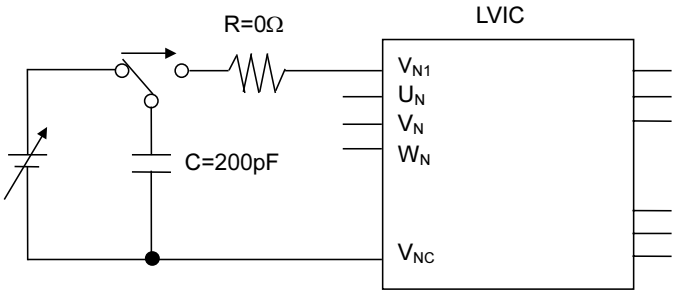


Fig.3-19 V_{N1} terminal Surge Test circuit

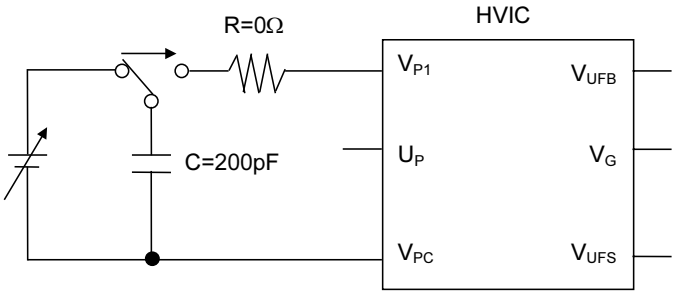


Fig.3-20 V_{P1} terminal Surge Test circuit

CHAPTER 4 KEY PARAMETERS SELECTING GUIDANCE

4.1 Determination of Shunt Resistance

(1) Shunt resistance

The value of current sensing resistance is calculated by the following expression:

$$R_{Shunt} = V_{SC(ref)}/SC$$

where $V_{SC(ref)}$ is the referenced SC trip voltage.

The maximum value of SC trip level should be set less than the IGBT minimum saturation current which is 1.7 times as large as the rated current. For example, the maximum SC trip level of PS21964 is 1.7 x 15=25.5A.

The parameters ($V_{SC(ref)}$, R_{Shunt}) dispersion should be considered in the design.

for example of PS21964-4, there is 0.1V dispersion in the data of $V_{SC(ref)}$ as shown in Table 4-1.

Table 4-1. Specification for $V_{SC(ref)}$ (unit: V)

	Min	Typ	Max
Specification at Tj=25°C, VD=15V	0.43	0.48	0.53

Then, the variation of SC trip level can be calculated by the following expressions:

$$SC(max) = V_{SC(max)} / R_{Shunt(min)}$$
$$SC(typ) = V_{SC(typ)} / R_{Shunt(typ)}$$
$$SC(min) = V_{SC(min)} / R_{Shunt(max)}$$

Supposing shunt resistance dispersion is +/-5%, then the SC range can be obtained as shown in Table 4-2

Table 4-2. Operative SC Range (unit: A) (R_{Shunt}=20.8mΩ(min), 21.9mΩ(typ), 23.0mΩ(max)

	min.	typ.	max.
Operative SC level at Tj=25°C	18.7	21.9	25.5

It is possible that the actual SC protective level is less than the calculated one. This is considered due to the resonant signals caused mainly by parasitic inductance and parasitic capacity. It is recommended to make a confirmation of the resistance by prototype experiment.

(2) RC Filter Time Constant

It is necessary to set an RC filter in the SC sensing circuit in order to prevent malfunction of SC protection due to noise interference. The RC time constant is determined depending on the applying time of noise interference and the SCSOA of the DIP-IPM.

When the voltage drop on the external shunt resistor exceeds the SC trip level, The time (t1) that the CIN terminal voltage rises to the referenced SC trip level can be calculated by the following expression:

$$V_{SC} = R_{shunt} \cdot I_c \cdot (1 - \varepsilon^{-\frac{t1}{\tau}})$$
$$t1 = -\tau \cdot \ln(1 - \frac{V_{SC}}{R_{shunt} \cdot I_c})$$

where Vsc is the CIN terminal input voltage, Ic the peak current, τ the RC time constant.

On the other hand, the typical time delay t2 (from Vsc voltage reaches Vsc(ref) to IGBT gate shutdown) of IC is shown in Table 4-3.

Table 4-3. Internal time delay of IC

Item	min	typ	max	Unit
IC transfer delay time	0.3	0.5	1.0	μs

Therefore, the total delay time from an SC level current happened to the IGBT gate shutdown becomes:

$$t_{TOTAL}=t1+t2$$

Fig.4-1 shows the typical SCSOA performance curve of PS21962,3,4. The DIP-IPM can shutdown safely an SC current that is about 9.5 times of its current rating under the noted conditions only if the IGBT conducting period is less than 4.5μsec.

The SCSOA operation area will vary with the control supply voltage, DC-link voltage, and etc.

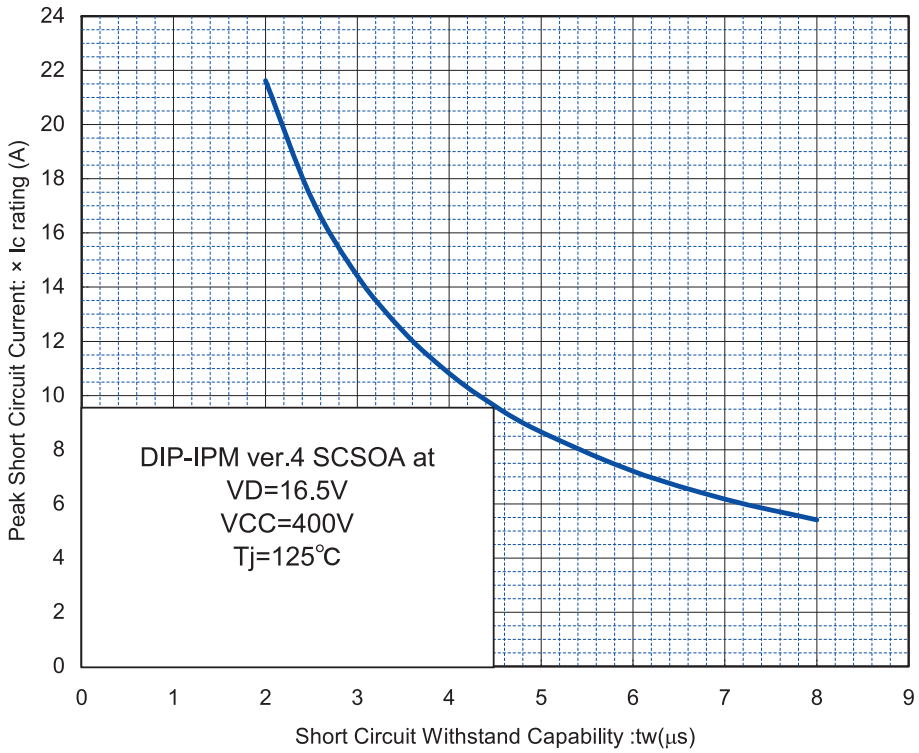


Fig.4-1 Typical SCSOA performance

4.2 Single Supply Drive Scheme

4.2.1 Bootstrap Capacitor Initial Charging

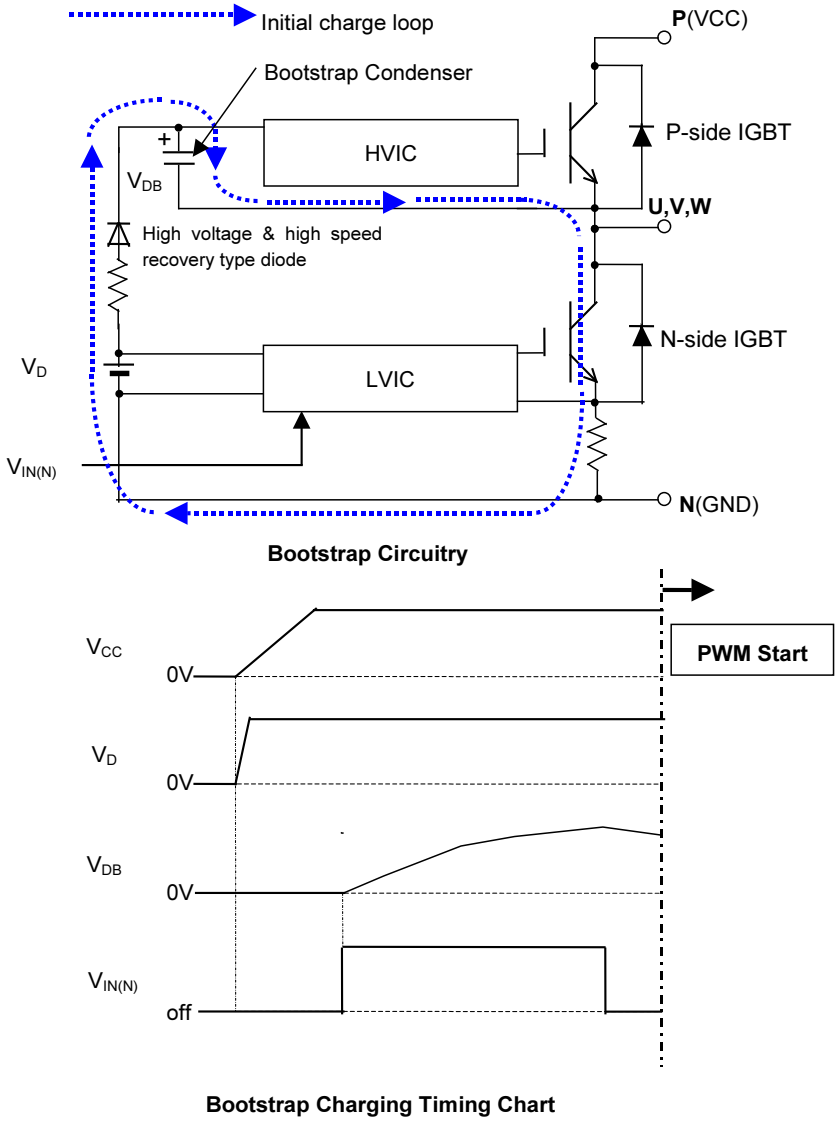


Fig.4-2 Initial charging loop and timing chart of bootstrap circuit

By using bootstrap circuit, conventional three isolated 15V power supply for P-side three IGBT drive can be eliminated. The initial charge of the bootstrap capacitors is necessary to start-up the inverter. Fig.4-2 shows the charge mechanism. The pulse width or pulse number should be large enough to make a full charge of the bootstrap capacitor.

For reference, the charging time for the bootstrap circuit with a 100μF capacitor and 50Ωcurrent limiting resistor is about 5msec.

4.2.2 Charging and Discharging of the Bootstrap Capacitor During Inverter Operation

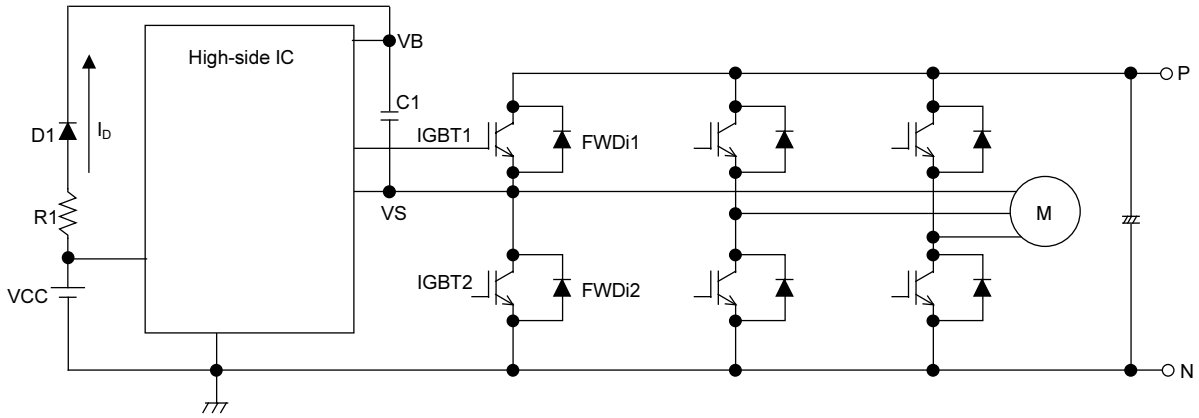


Fig.4-3 Inverter circuit diagram

(1) Charging operation Timing Chart of Bootstrap Capacitor (C1)

Sequence (1-1) : IGBT2 ON (Fig.4-4)

When IGBT2 is in ON state, charging voltage on C1 ($V_{C(1)}$) is calculated by

$V_{C(1)} = V_{CC}-V_{F1}-V_{sat2}-I_D \cdot R1$ (Transient state)

$V_{C(1)} = V_{CC}$ (Steady state)

where V_{CC} is the charging supply voltage, V_{F1} the forward voltage drop of diode D1, V_{sat2} the saturation voltage of IGBT2, I_D the charging current, and R1 the inrush current limitation resistance.

Then, IGBT2 is turned off. Motor current will flow through the free-wheel path of FWDi1. Once the electric potential of VS rises near to that of P, the charging to C1 is stopped.

When IGBT1 is in ON state, the voltage of C1 gradually declines from the potential $V_{C(1)}$ due to the current consumed by the drive circuit.

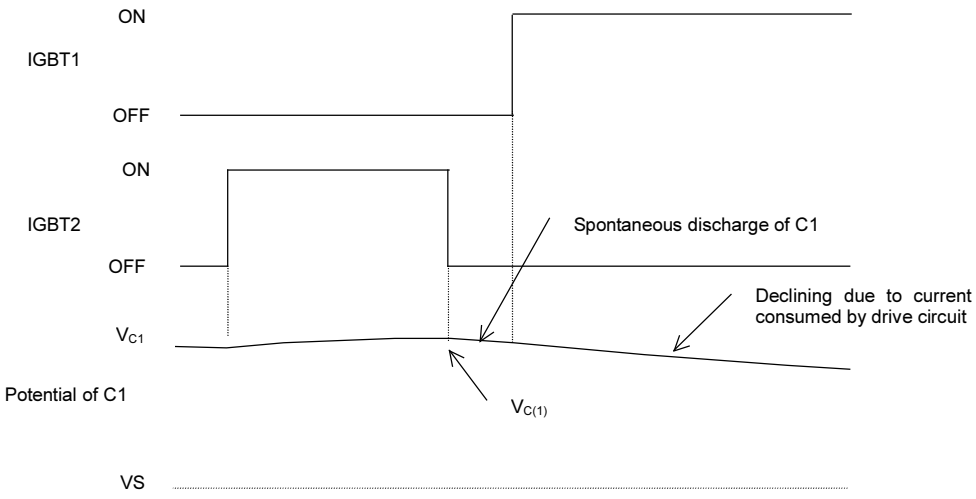


Fig.4-4 Timing chart of sequence (1-1)

Sequence (1-2): IGBT2 OFF and FWDi2 ON (Fig.4-5)
When IGBT2 is OFF and FWDi2 is ON, the voltage on C1 ($V_{C(2)}$) is calculated by:

$$V_{C(2)}=V_{CC}-V_{F1}+V_{EC2}$$

where V_{EC2} denotes the forward voltage drop of FWDi2. When both IGBT2 and IGBT1 are OFF, the regenerative current flows continuously through the free-wheel path of FWDi2. Therefore the potential of VS drops to $-V_{EC2}$, then C1 is recharged to restore the declined potential. When IGBT1 is turned ON, the potential of V_S rises to that of P, the charge to C1 stops and the voltage on C1 gradually declines from the potential $V_{C(2)}$ due to the current consumed by the drive circuit.

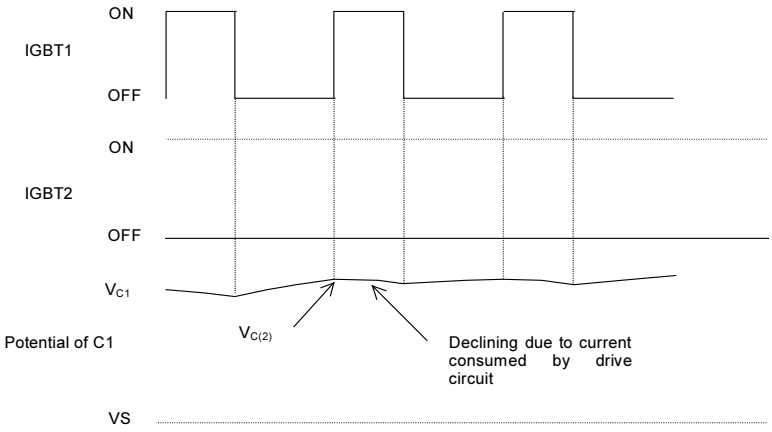


Fig.4-5 Timing chart of sequence (1-2)

（2）Instruction of Selecting the Bootstrap Capacitor (C1) and Resistance (R1)
The capacitance of bootstrap capacitor can be calculated by:

$$C1=I_{BS}\times T1/\Delta V$$

where T1 is the maximum ON pulse width of IGBT1 and I_{BS} is the drive current of the IC (depends on temperature and frequency characteristics), and ΔV is the allowable discharge voltage. A certain margin should be added to the calculated capacitance.
Resistance R1 should be basically selected such that the time constant C1R1 will enable the discharged voltage (ΔV) to be fully charged again within the minimum ON pulse width (T2) of IGBT2.
However, if only IGBT1 has an ON-OFF-ON control mode (Fig.4-6), the time constant should be set so that the consumed energy during the ON period can be charged during the OFF period.

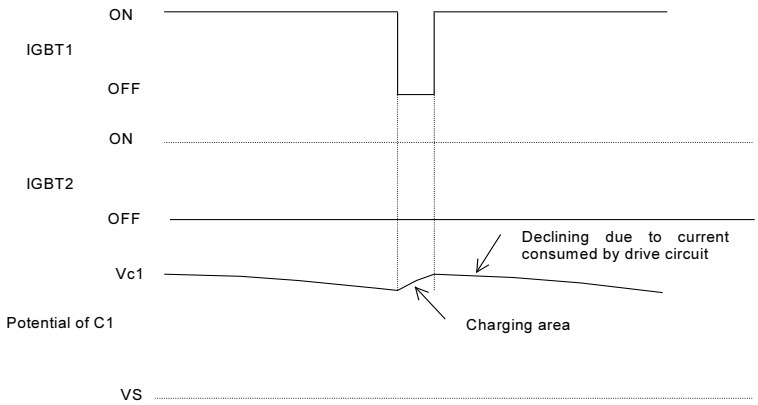


Fig.4-6 Timing Chart of ON-OFF-ON Control Mode

Design example of Bootstrap circuit

■ Selecting bootstrap capacitor

Suppose ΔV_{DB}(discharged voltage)=1V, the maximum ON pulse width T1 of P-side IGBT is 5msec, and I_{DB} is 0.55mA(Max. rating), then

$$C=I_{DB}\times T1/\Delta V_{DB}=2.75\times 10^{-6}$$

the calculated bootstrap capacitance is 2.75μF. By taking consideration of dispersion and reliability, the capacitance is generally selected as large as 2~3 times of the calculated one, for example, 10μF or above for this case is suitable.

■ Selecting bootstrap resistor

Suppose the bootstrap capacitance is 10μF, V_D=15V, V_{DB}=14V, and the minimum ON pulse width t_0 of N-side IGBT (or the minimum OFF pulse width t_0 of upper-side IGBT) is 20μs, then to recover V_{DB} to 15V during this period, the bootstrap resistance should be

$$R=\{(V_D-V_{DB})\times t_0\}/(C\times\Delta V_{DB})=2$$

This means a 2Ωresistor is suitable.

Note:

(1) In the case of the control for DCBLM or 2-phase modulation for IM (Induction Motor), there will be a long ON time period on the P-side IGBT, please pay attention to the bootstrap supply voltage drop.

(2) The above result is only a calculation example. It is recommended to design a system by taking consideration of the actual control pattern and lifetime of components.

■ Selecting bootstrap diode

The bootstrap diode with blocking voltage over 600V is recommended. In DIP-IPM, the maximum rating of power supply is 450V. The actual voltage applied on the diode is 500V by adding a surge voltage of about 50V. Furthermore, if considering 100V for the margin, 600V class diode is necessary. The diode is also highly recommended to be with fast recovery characteristics (recovery time less than 100nsec).

■ Noise filter for control supply

It is recommended to insert a film type or ceramic type noise filter with 0.22-2μF to the control supply terminals(V_{P1}-V_{NC}, V_{N1}-V_{NC}, V_{UFB}-U, V_{VFB}-V, V_{WFB}-W). The smaller the supply parasitic impedance is, the smaller a feasible noise filter capacitance can be . The supply circuit should be such designed that the noise fluctuation is less than +/-1V/μs, and the ripple voltage is less than +/-2V.

Reference:

There are tow kinds of control supply in general use. The first one is DC-DC converter (3-terminal regulator), of which input DC supply comes from AC-transformer. The other is DC-DC converter (switching regulator), of which input DC supply is generated by a SMPS.

Note:

After bootstrap capacitor voltage has been fully charged, input one pulse in the P-side input signals to reset internal IC state before starting formal PWM.

CHAPTER 5 INTERFACE DEMO BOARD

5.1 Super Mini DIP-IPM Ver.4 Interface Demo Board

This chapter describes the interface demo board of Super Mini DIP-IPM Ver.4 as a reference for the design of user application PCB with Super Mini DIP-IPM Ver.4.

(1) Demo Board Outline

The demo board consists the minimum necessary components such as snubber capacitor, bootstrap circuit elements of Super Mini DIP-IPM Ver.4 interface shown in Fig.5-1.

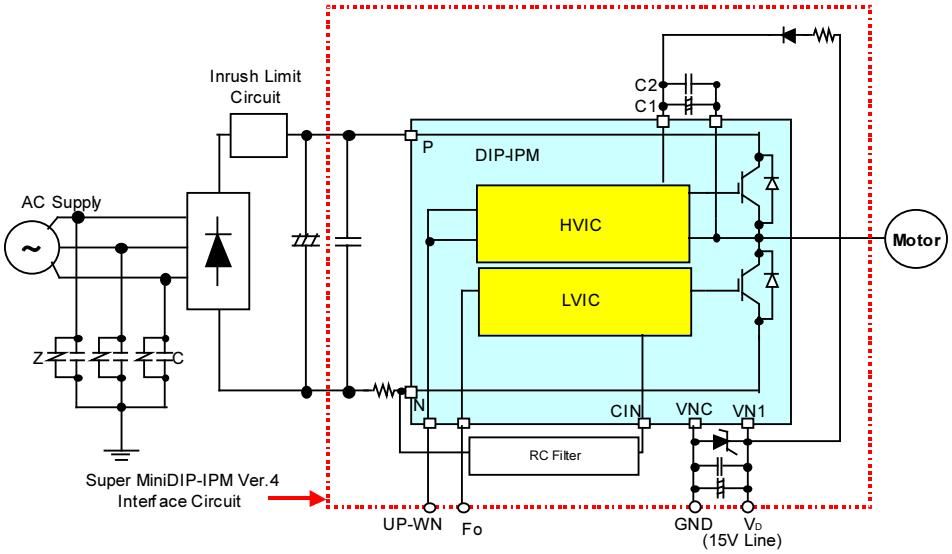
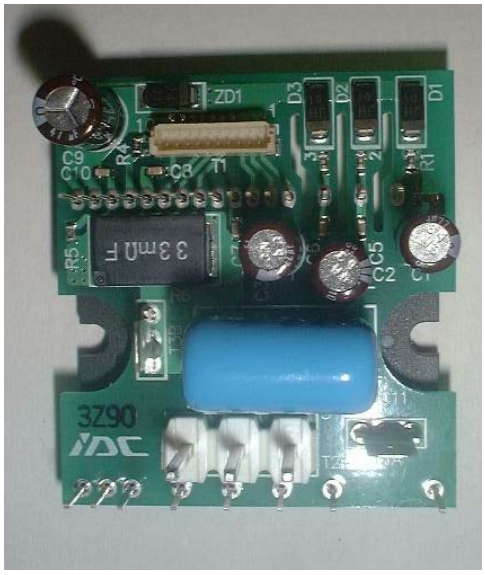
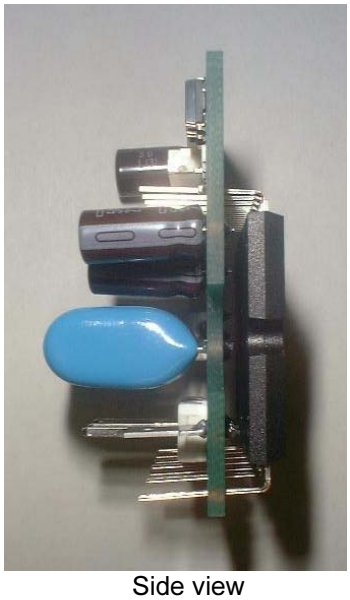


Fig.5-1 Demo board interface circuit

(2) Demo Board Photos



Top view



Side view

Fig.5-2 Demo board photo

Note: Board dimension 43.5×40×27.1mm (including snubber capacitor height and module height)

5.2 Pattern Wiring

(1) Component Layout

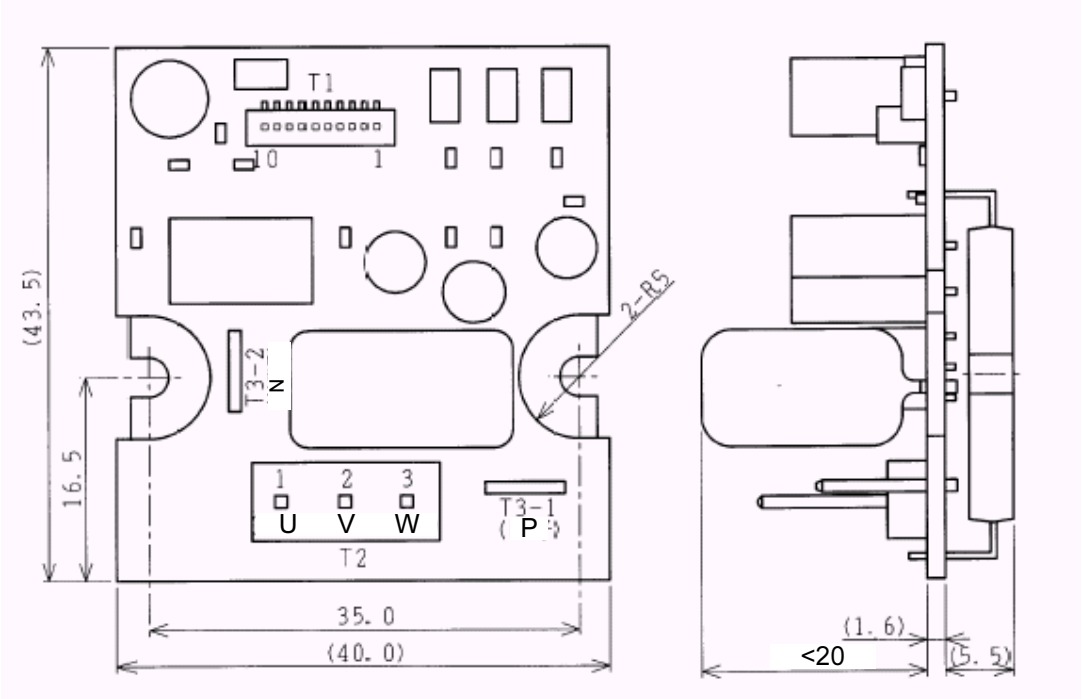
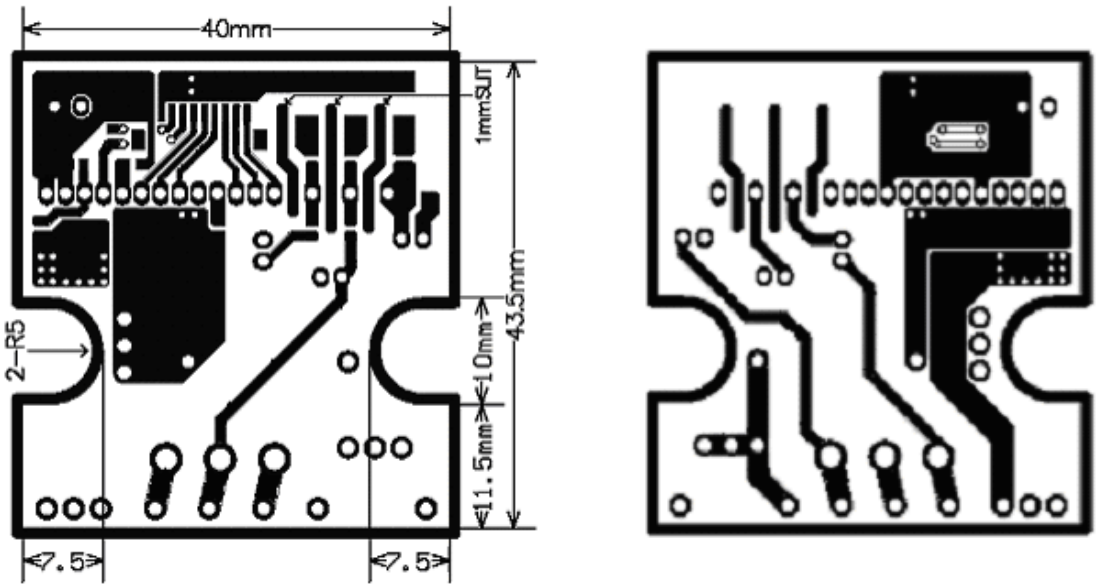


Fig.5-3 Demo board component layout

(2) PCB Pattern Layout



(a) Component side (b) Solder side

Fig.5-4 Demo board PCB pattern layout

5.3 Circuit Schematic and Parts List

(1) Circuit Schematic

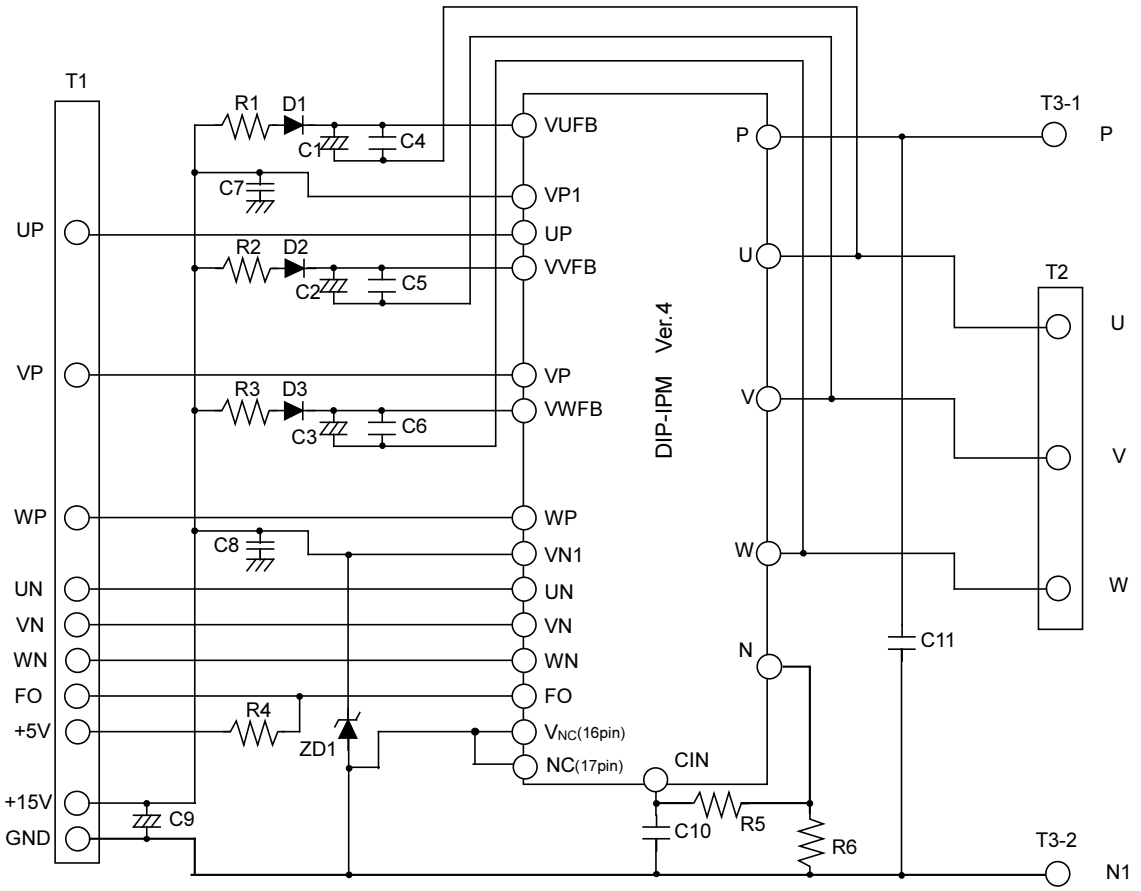


Fig.5-5 Demo board circuit schematic

Note: Although there is no zener diode mounted to P-side three floating drive supplies (between V_{UFB}-U, V_{VFB}-V, V_{WFB}-W) on this demo board, it is highly recommend to add these zener diodes in actual system board.

(2) Parts List

Table 5-1 Parts list (only for reference)

Symbol	Type Name	Description	pcs	Note
D1	U05JH44	0.5A 600V Diode	1	Toshiba, High speed type
D2	U05JH44	0.5A 600V Diode	1	Toshiba, High speed type
D3	U05JH44	0.5A 600V Diode	1	Toshiba, High speed type
ZD1	U1ZB24	24V 1W Zener Diode	1	Toshiba
C1	UFP1H220MEH	22μF50V Al electrolytic capacitor	1	Nichicon
C2	UFP1H220MEH	22μF50V Al electrolytic capacitor	1	Nichicon
C3	UFP1H220MEH	22μF50V Al electrolytic capacitor	1	Nichicon
C4	GRM188R11H102KA01	1000pF50V ceramic capacitor	1	Murata
C5	GRM188R11H102KA01	1000pF50V ceramic capacitor	1	Murata
C6	GRM188R11H102KA01	1000pF50V ceramic capacitor	1	Murata
C7	GRM188R11H102KA01	1000pF50V ceramic capacitor	1	Murata
C8	GRM188R11H102KA01	1000pF50V ceramic capacitor	1	Murata
C9	UFP1H470MEH	47μF50V Al electrolytic capacitor	1	Nichicon
C10	GRM188R11H102KA01	1000μF50V ceramic capacitor	1	Murata
C11	MDDSA2J224K	0.22μF630V snubber capacitor	1	Hitachi AIC
R1	RK73H1JTD10F	1/16W 10ΩF	1	KOA
R2	RK73H1JTD10F	1/16W 10ΩF	1	KOA
R3	RK73H1JTD10F	1/16W 10ΩF	1	KOA
R4	RK73H1JTD10kF	1/16W 10kΩF	1	KOA
R5	RK73H1JTD2kF	1/16W 2kΩF	1	KOA
R6	SL2TTE68LF	2W 0.016/0.021/0.033/0.068/0.11ΩF	1	KOA, Current detecting resistor
T1	BS10B-SRSS	10pin Socket	1	
T2	B3P-VB-2	3-terminal connector	1	
T3-1	TP42097-21	Faston® tab	1	
T3-2	TP42097-21	Faston® tab	1	

(3) Precaution in using the demo board for pre-evaluation

a. The accessories of the Super Mini DIP-IPM Ver.4demo board include an input signal connection cable and a power supply cable with a connector.
Cut the input signal cable to make the connection between MCU/DSP and the demo board as short as possible.

b. Please confirm and comply with your company's design standard when drawing upon these patterns. (These patterns are an example for reference.)

Faston® is a registered trademark of the AMP company.

CHAPTER 6 PACKAGE HANDLING

6.1 Packaging Specification

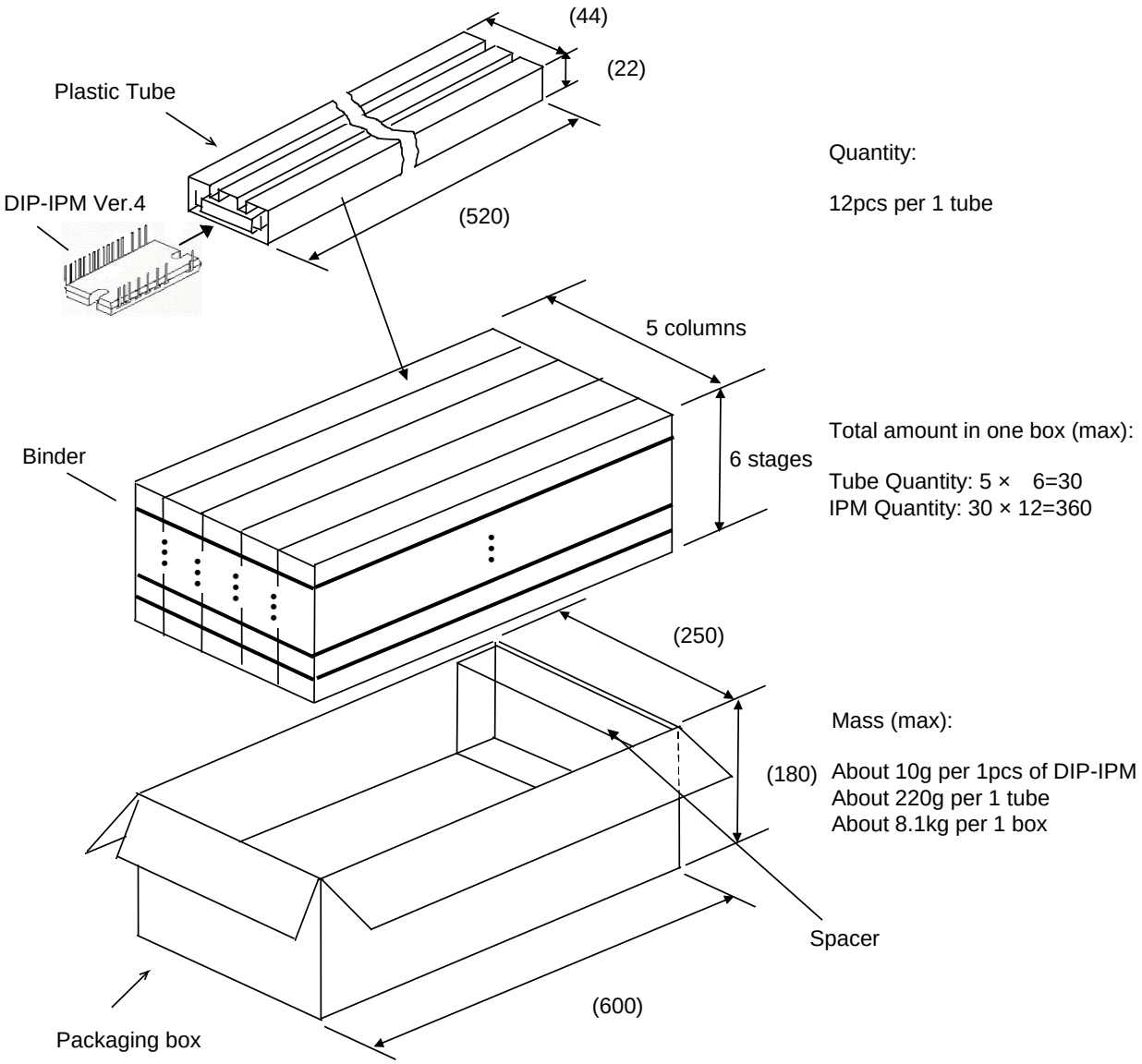


Fig.6-1 Super Mini DIP-IPM Ver.4 Packaging Specification

6.2 Handling Precautions

⚠ Cautions	
Transportation	·Put package boxes in the correct direction. Putting them upside down, leaning them or giving them uneven stress might cause electrode terminals to be deformed or resin case to be damaged. ·Throwing or dropping the packaging boxes might cause the devices to be damaged. ·Wetting the packaging boxes might cause the breakdown of devices when operating. Pay attention not to wet them when transporting on a rainy or a snowy day.
Storage	·We recommend temperature and humidity in the ranges 5-35°C and 45-75%, respectively, for the storage of modules. The quality or reliability of the modules might decline if the storage conditions are much different from the above.
Long storage	·When storing modules for a long time (more than one year), keep them dry. Also, when using them after long storage, make sure that there is no visible flaw, stain or rust, etc. on their exterior.
Surroundings	·Keep modules away from places where water or organic solvent may attach to them directly or where corrosive gas, explosive gas, fine dust or salt, etc. may exist. They might cause serious problems.
Flame resistance	·The epoxy resin and the case materials are flame-resistant type (UL standard 94-V0), but they are not noninflammable.
Static electricity	·ICs and power chips with MOS gate structure are used for the DIP-IPM power modules. Please keep the following notices to prevent modules from being damaged by static electricity. (1)Precautions against the device destruction caused by the ESD The ESD of human bodies and packaging and/or excessive voltage applied across the gate to emitter may damage and destroy devices. The basis of anti-electrostatic is to inhibit generating static electricity possibly and quick dissipation of the charged electricity. *Containers that charge static electricity easily should not be used for transit and for storage. *Terminals should be always shorted with a carbon cloth or the like until just before using the module. Never touch terminals with bare hands. *Should not be taking out DIP-IPM from tubes until just before using DIP-IPM and never touch terminals with bare hands. *During assembly and after taking out DIP-IPM from tubes, always earth the equipment and your body. It is recommended to cover the work bench and its surrounding floor with earthed conductive mats. *When the terminals are open on the printed circuit board with mounted modules, the modules might be damaged by static electricity on the printed circuit board. *If using a soldering iron, earth its tip. (2)Notice when the control terminals are open *When the control terminals are open, do not apply voltage between the collector and emitter. It might cause malfunction. *Short the terminals before taking a module off.

Keep safety first in your circuit designs!

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