



## TS4975

### Stereo Headphone Drive Amplifier with Digital Volume Control via I<sup>2</sup>C Bus

- Operating from  $V_{CC} = 2.5V$  to  $5.5V$
- I<sup>2</sup>C bus control interface
- 40mW output power @  $V_{CC} = 3.3V$ , THD = 1%, F = 1kHz, with 16 $\Omega$  load
- Ultra-low consumption in stdby mode: 0.6 $\mu$ A
- Digital volume control range from 18dB to -34dB
- 14-step digital volume control
- 9 different output mode selections
- Pop & click noise reduction circuitry
- Flip-chip package, 12 x 300 $\mu$ m bumps (lead-free)

### Description

The TS4975 is a stereo audio headphone driver capable of delivering up to 102mW per channel of continuous average power into a 16 $\Omega$  single-ended load with 1% THD+N from a 5V power supply. The overall gain of these headphone drivers is controlled digitally by volume control registers programmed via the I<sup>2</sup>C interface, minimizing the number of external components needed. This device can also easily be driven by an MCU to select the output modes, through the I<sup>2</sup>C bus interface.

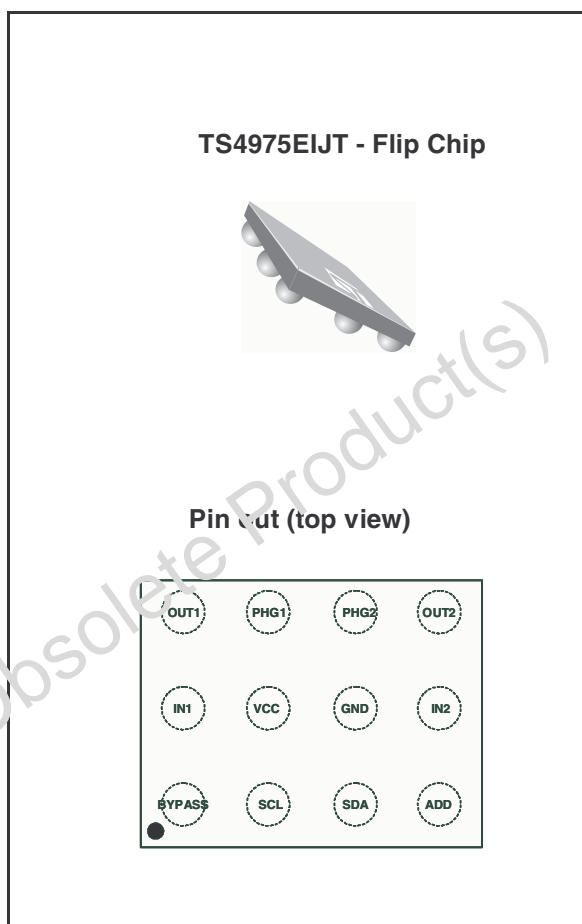
A phantom ground configuration allows one to avoid using bulky capacitors on the outputs of the headphone amplifiers.

The TS4975 is packaged in a 1.8mm X 2.3mm Flip-Chip package, ideally suited for space-conscious portable applications.

It has also an internal thermal shutdown protection mechanism.

### Order Codes

Part Number	Temperature Range	Package	Packing	Marking
TS4975EIJT	-40, +85°C	Flip-chip	Tape & Reel	A75



### Applications

- Mobile phones (cellular / cordless)
- PDAs
- Laptop/notebook computers
- Portable audio devices

# 1 Absolute Maximum Ratings

**Table 1. Key parameters and their absolute maximum ratings**

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply voltage <sup>(1)</sup>	6	V
V <sub>i</sub>	Input Voltage <sup>(2)</sup>	G <sub>ND</sub> to V <sub>CC</sub>	V
T <sub>oper</sub>	Operating Free Air Temperature Range	-40 to + 85	°C
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>j</sub>	Maximum Junction Temperature	150	°C
R <sub>thja</sub>	Thermal Resistance Junction to Ambient <sup>(3)</sup>	200	°C/W
P <sub>diss</sub>	Power Dissipation	Internally Limited <sup>(4)</sup>	
ESD	Susceptibility - Human Body Model <sup>(5)</sup>	2	kV
ESD	Susceptibility - Machine Model (min. Value)	200	V
Latch-up	Latch-up Immunity	200	mA
	Lead Temperature (soldering, 10sec)	260	°C

1. All voltages values are measured with respect to the ground pin.
2. The magnitude of input signal must never exceed V<sub>CC</sub> + 0.3V / G<sub>ND</sub> - 0.3V
3. Device is protected in case of over temperature by a thermal shutdown active @ 150°C.
4. Exceeding the power derating curves during a long period, may involve abnormal operating condition.
5. Human body model, 100pF discharged through a 1.5kOhm resistor, into pin to V<sub>CC</sub> device.

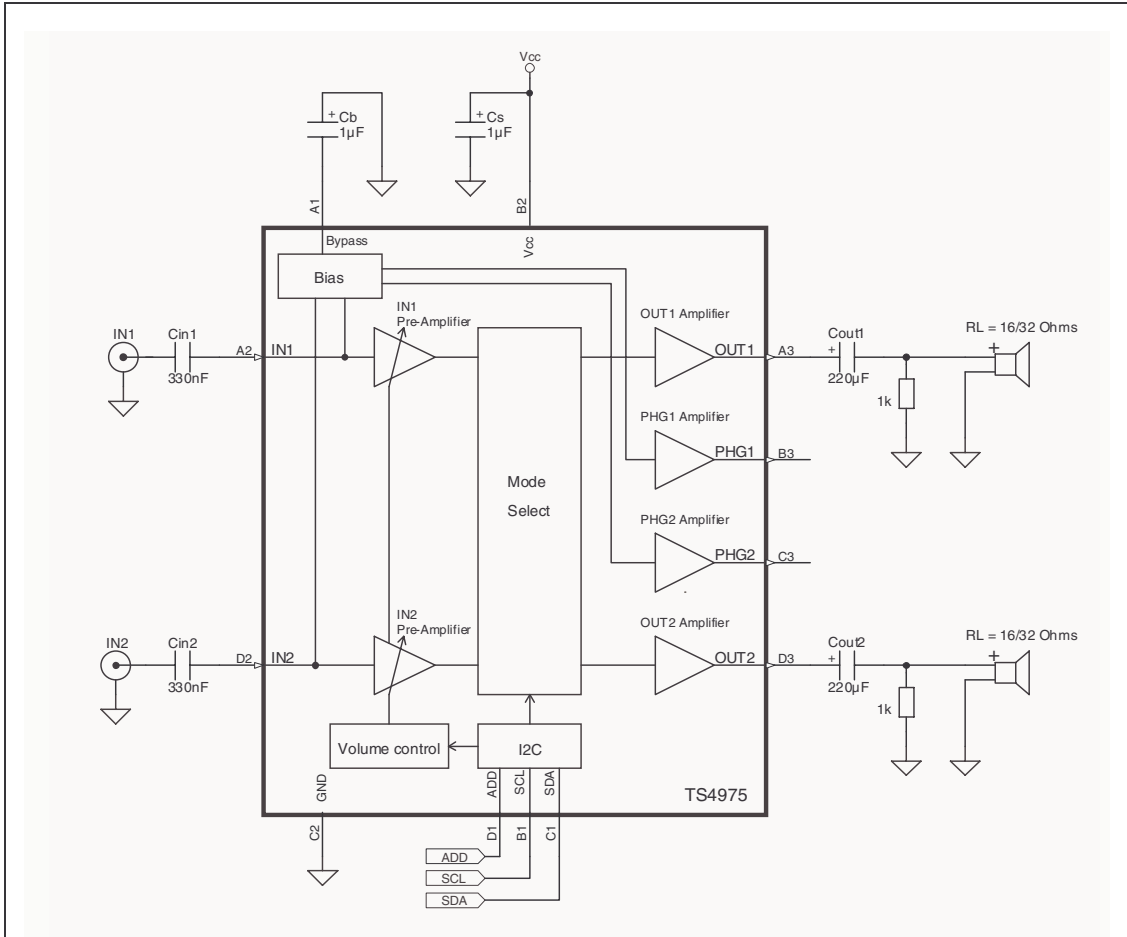
**Table 2. Operating conditions**

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply Voltage	2.5 to 5.5v	V
R <sub>L</sub>	Load Resistor	>16	Ω
C <sub>L</sub>	Load Capacitor R <sub>L</sub> = 16 to 100Ω, R <sub>L</sub> > 100Ω,	400 100	pF
T <sub>oper</sub>	Operating Free Air Temperature Range	-40 to +85	°C
R <sub>thja</sub>	Flip Chip Thermal Resistance Junction to Ambient	90	°C/W

## 2 Typical Application Schematics

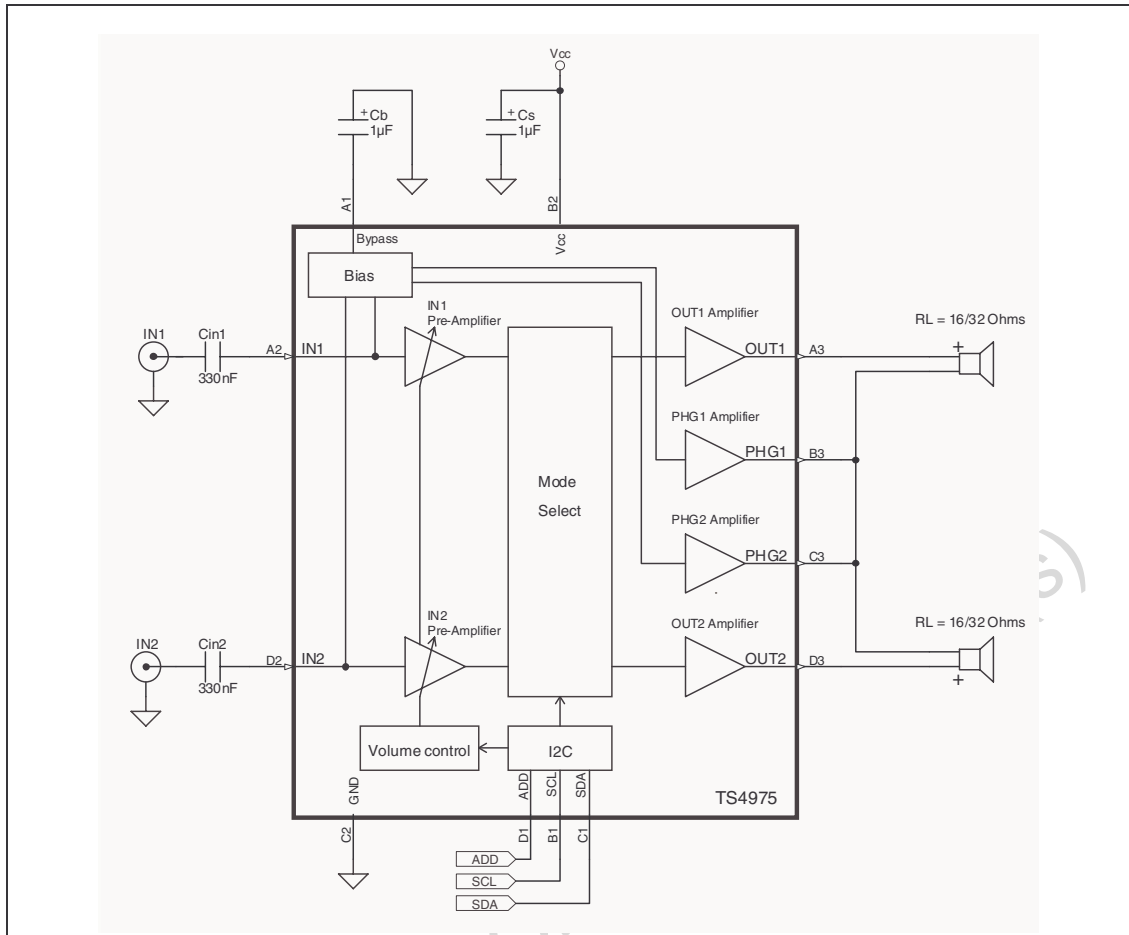
Typical application schematics for the TS4975 are show in *Figure 1*, for a single-ended output configuration and in *Figure 2*, for a phantom ground output configuration.

**Figure 1. Single-ended configuration**



Obsolete Product

Figure 2. Phantom ground output configuration



Obsolete Product(s) - C

### 3 Electrical Characteristics

**Table 3. Electrical characteristics for the I<sup>2</sup>C interface**

Symbol	Parameter	Value	Unit
$V_{IL}$	Maximum Low level Input Voltage on pins SDA, SCL, VADD	$0.3 V_{CC}$	V
$V_{IH}$	Minimum High Level Input Voltage on pins SDA, SCL, VADD	$0.7 V_{CC}$	V
$F_{SCL}$	SCL Maximum clock Frequency	400	kHz
$V_{ol}$	Max Low Level Output Voltage, SDA pin, $I_{sink} = 3mA$	0.4	V
$I_i$	Max Input current on SDA, SCL <sup>(1)</sup> from $0.1 V_{CC}$ to $0.9 V_{CC}$	10	$\mu A$

1. SCL and SDA are CMOS inputs. The nominal input current is about few pA and not 10uA. 10 $\mu A$  refer to the I2C bus specification.

**Table 4. Output noise (all inputs grounded)**

	Unweighted Filter from $V_{CC} = 2.5V$ to $5V$	Weighted Filter (A) from $V_{CC} = 2.5V$ to $5V$
SE, G = +2dB	34 $\mu V_{rms}$	23 $\mu V_{rms}$
SE, G = +18dB	67 $\mu V_{rms}$	45 $\mu V_{rms}$
PHG, G = +2dB	34 $\mu V_{rms}$	23 $\mu V_{rms}$
PHG, G = +18dB	67 $\mu V_{rms}$	45 $\mu V_{rms}$

Table 5.  $V_{CC} = +2.5\text{ V}$ ,  $GND = 0\text{V}$ ,  $T_{amb} = 25^\circ\text{C}$  (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_{CC}$	Supply Current	No input signal, no load, Single-ended, Mode 1-4		3	4.2	mA
		No input signal, no load, Single-ended, Mode 5-8		2	2.8	
		No input signal, no load, Phantom Ground, Mode 1-4		4.6	6.5	
		No input signal, no load, Phantom Ground, Mode 5-8		3.6	5.3	
$I_{STBY}$	Standby Current	SCL and SDA at $V_{CC}$ level, No input signal		0.6	2	$\mu\text{A}$
$V_{oo}$	Output Offset Voltage	No input signal, $R_L = 32\Omega$ , Phantom Ground		5	50	mV
$P_{out}$	Output Power (per channel)	Single-ended, THD+N = 1% Max, $F = 1\text{kHz}$ , $R_L = 16\Omega$	15	21		mW
		Single-ended, THD+N = 1% Max, $F = 1\text{kHz}$ , $R_L = 32\Omega$	11	13		
		Phantom Ground, THD+N = 1% Max, $F = 1\text{kHz}$ , $R_L = 16\Omega$	15	21		
		Phantom Ground, THD+N = 1% Max, $F = 1\text{kHz}$ , $R_L = 32\Omega$	11	13		
THD + N	Total Harmonic Distortion + Noise	Single-ended, $A_V = 2\text{dB}$ , $R_L = 32\Omega$ , $P_{out} = 10\text{ mW}$ , $20\text{Hz} < F < 20\text{kHz}$		0.3		%
		Single-ended, $A_V = 2\text{dB}$ , $R_L = 16\Omega$ , $P_{out} = 15\text{ mW}$ , $20\text{Hz} < F < 20\text{kHz}$		0.3		
		Phantom Ground, $A_V = 2\text{dB}$ , $R_L = 32\Omega$ , $P_{out} = 10\text{ mW}$ , $20\text{Hz} < F < 20\text{kHz}$		0.3		
		Phantom Ground, $A_V = 2\text{dB}$ , $R_L = 16\Omega$ , $P_{out} = 15\text{ mW}$ , $20\text{Hz} < F < 20\text{kHz}$		0.3		
PSRR	Power Supply Rejection Ratio <sup>(1)</sup>	<b>Single-ended Output referenced to Phantom Ground</b> $F = 217\text{Hz}$ , $R_L = 16\Omega$ , $A_V = 2\text{dB}$ $V_{ripple} = 200\text{mV}_{pp}$ , Input Grounded, $C_b = 1\mu\text{F}$		60		
		<b>Single-ended Output referenced to Ground,</b> $F = 217\text{Hz}$ , $R_L = 16\Omega$ , $A_V = 2\text{dB}$ $V_{ripple} = 200\text{mV}_{pp}$ , Input Grounded, $C_b = 1\mu\text{F}$		60		dB

Table 5.  $V_{CC} = +2.5\text{ V}$ ,  $GND = 0\text{V}$ ,  $T_{amb} = 25^\circ\text{C}$  (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Crosstalk	Channel Separation	$R_L = 32\Omega$ , $A_V = 2\text{dB}$ with Single-ended $F = 1\text{kHz}$ , $P_{out} = 10\text{mW}$		103		dB
		$R_L = 32\Omega$ , $A_V = 2\text{dB}$ with Single-ended $F = 20\text{Hz}$ to $20\text{kHz}$ , $P_{out} = 10\text{mW}$		75		
		$R_L = 32\Omega$ , $A_V = 2\text{dB}$ with Phantom Ground, $F = 1\text{kHz}$ , $P_{out} = 10\text{mW}$		69		
		$R_L = 32\Omega$ , $A_V = 2\text{dB}$ with Phantom Ground, $F = 20\text{Hz}$ to $20\text{kHz}$ , $P_{out} = 10\text{mW}$		69		
SNR	Signal to Noise Ratio A-Weighted	$A_V = 2\text{dB}$ , $R_L = 32\Omega$ , $P_{out} = 12\text{mW}$ Single-Ended		88		dB
		$A_V = 2\text{dB}$ , $R_L = 32\Omega$ , $P_{out} = 12\text{mW}$ Phantom Ground		88		
ONoise	Output Noise Voltage, A-Weighted	$A_V = 2\text{dB}$ , Single-ended		23		$\mu\text{Vrms}$
		$A_V = 2\text{dB}$ , Phantom Ground		23		
G	Digital Gain Range	In1 & In2 to Out1 & Out2	-34		+18	dB
	Digital Gain Stepsize			4		dB
	Gain Error Tolerance		-1		+1	dB
$Z_{in}$	In1 & In2 Input Impedance	All gain settings	25.5	30	34.5	$\text{k}\Omega$
$t_{wu}$	Wake up time	$C_b = 1\mu\text{F}$		110	180	ms
$t_{ws}$	Standby time			1		$\mu\text{s}$

1. Dynamic measurements -  $20 \cdot \log(\text{rms}(V_{out})/\text{rms}(V_{ripple}))$ .  $V_{ripple}$  is an added sinus signal to  $V_{CC}$  @  $F = 217\text{Hz}$

Table 6.  $V_{CC} = +3.3V$ ,  $GND = 0V$ ,  $T_{amb} = 25^{\circ}C$  (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_{CC}$	Supply Current	No input signal, no load, Single-ended, Mode 1-4		3	4.2	mA
		No input signal, no load, Single-ended, Mode 5-8		2	2.8	
		No input signal, no load, Phantom Ground, Mode 1-4		4.6	6.5	
		No input signal, no load, Phantom Ground, Mode 5-8		3.6	5.3	
$I_{STBY}$	Standby Current	SCL and SDA at $V_{CC}$ level, No input signal		0.6	2	$\mu A$
$V_{oo}$	Output Offset Voltage	No input signal, $R_L = 32\Omega$ , Phantom Ground		5	50	mV
$P_{out}$	Output Power (per channel)	Single-ended, THD+N = 1% Max, $F = 1kHz$ , $R_L = 16\Omega$	34	40		mW
		Single-ended, THD+N = 1% Max, $F = 1kHz$ , $R_L = 32\Omega$	24	26		
		Phantom Ground, THD+N = 1% Max, $F = 1kHz$ , $R_L = 16\Omega$	34	40		
		Phantom Ground, THD+N = 1% Max, $F = 1kHz$ , $R_L = 32\Omega$	24	26		
THD + N	Total Harmonic Distortion + Noise	Single-ended, $A_V = 2dB$ , $R_L = 32\Omega$ , $P_{out} = 20\text{ mW}$ , $20Hz < F < 20kHz$		0.3		%
		Single-ended, $A_V = 2dB$ , $R_L = 16\Omega$ , $P_{out} = 30\text{ mW}$ , $20Hz < F < 20kHz$		0.3		
		Phantom Ground, $A_V = 2dB$ , $R_L = 32\Omega$ , $P_{out} = 20\text{ mW}$ , $20Hz < F < 20kHz$		0.3		
		Phantom Ground, $A_V = 2dB$ , $R_L = 16\Omega$ , $P_{out} = 30\text{ mW}$ , $20Hz < F < 20kHz$		0.3		
PSRR	Power Supply Rejection Ratio <sup>(1)</sup>	<b>Single-ended Output referenced to Phantom Ground</b> $F = 217Hz$ , $R_L = 16\Omega$ , $A_V = 2dB$ $V_{ripple} = 200mV_{pp}$ , Input Grounded, $C_b = 1\mu F$		61		dB
		<b>Single-ended Output referenced to Ground,</b> $F = 217Hz$ , $R_L = 16\Omega$ , $A_V = 2dB$ $V_{ripple} = 200mV_{pp}$ , Input Grounded, $C_b = 1\mu F$		61		



Table 6.  $V_{CC} = +3.3V$ ,  $GND = 0V$ ,  $T_{amb} = 25^{\circ}C$  (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Crosstalk	Channel Separation	$R_L = 32\Omega$ , $A_V = 2dB$ with Single-ended $F = 1kHz$ , $P_{out} = 20mW$		103		dB
		$R_L = 32\Omega$ , $A_V = 2dB$ with Single-ended $F = 20Hz$ to $20kHz$ , $P_{out} = 20mW$		75		
		$R_L = 32\Omega$ , $A_V = 2dB$ with Phantom Ground, $F = 1kHz$ , $P_{out} = 20mW$		69		
		$R_L = 32\Omega$ , $A_V = 2dB$ with Phantom Ground, $F = 20Hz$ to $20kHz$ , $P_{out} = 20mW$		69		
SNR	Signal To Noise Ratio	$A_V = 2dB$ , $R_L = 32\Omega$ , $P_{out} = 25mW$ Single-Ended		90		dB
		$A_V = 2dB$ , $R_L = 32\Omega$ , $P_{out} = 25mW$ Phantom Ground		90		
ONoise	Output Noise Voltage, A-Weighted	$A_V = 2dB$ , Single-ended		23		$\mu V_{rms}$
		$A_V = 2dB$ , Phantom Ground		23		
G	Digital Gain Range	In1 & In2 to Out1 & Out2	-34		+18	dB
	Digital Gain Step size			4		dB
	Gain Error Tolerance		-1		+1	dB
$Z_{in}$	In1 & In2 Input Impedance	All gain settings	25.5	30	34.5	$k\Omega$
$t_{wu}$	Wake up time	$C_b = 1\mu F$		90	156	ms
$t_{ws}$	Standby time			1		$\mu s$

1. Dynamic measurements -  $20 \cdot \log(\text{rms}(V_{out})/\text{rms}(V_{ripple}))$ .  $V_{ripple}$  is an added sinus signal to  $V_{CC}$  @  $F = 217Hz$

Table 7.  $V_{CC} = +5V$ ,  $GND = 0V$ ,  $T_{amb} = 25^{\circ}C$  (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_{CC}$	Supply Current	No input signal, no load, Single-ended, Mode 1-4		3	4.2	mA
		No input signal, no load, Single-ended, Mode 5-8		2	2.8	
		No input signal, no load, Phantom Ground, Mode 1-4		4.6	6.5	
		No input signal, no load, Phantom Ground, Mode 5-8		3.6	5.3	
$I_{STBY}$	Standby Current	SCL and SDA at $V_{CC}$ level, No input signal		0.6	2	$\mu A$
$V_{oo}$	Output Offset Voltage	No input signal, $R_L = 32\Omega$ , Phantom Ground		5	50	mV
$P_{out}$	Output Power (per channel)	Single-ended, THD+N = 1% Max, F = 1kHz, $R_L = 16\Omega$	92	102		mW
		Single-ended, THD+N = 1% Max, F = 1kHz, $R_L = 32\Omega$	59	64		
		Phantom Ground, THD+N = 1% Max, F = 1kHz, $R_L = 16\Omega$	92	98		
		Phantom Ground, THD+N = 1% Max, F = 1kHz, $R_L = 32\Omega$	59	63		
THD + N	Total Harmonic Distortion + Noise	Single-ended, $A_V = 2dB$ , $R_L = 32\Omega$ , $P_{out} = 50$ mW, $20Hz < F < 20kHz$ ,		0.3		%
		Single-ended, $A_V = 2dB$ , $R_L = 16\Omega$ , $P_{out} = 80$ mW, $20Hz < F < 20kHz$		0.3		
		Phantom Ground, $A_V = 2dB$ , $R_L = 32\Omega$ , $P_{out} = 50$ mW, $20Hz < F < 20kHz$		0.3		
		Phantom Ground $A_V = 2dB$ , $R_L = 16\Omega$ , $P_{out} = 80$ mW, $20Hz < F < 20kHz$		0.3		
PSRR	Power Supply Rejection Ratio <sup>(1)</sup>	<b>Single-ended Output referenced to Phantom Ground</b> F = 217Hz, $R_L = 16\Omega$ , $A_V = 2dB$ $V_{ripple} = 200mV_{pp}$ , Input Grounded, $C_b = 1\mu F$		63		dB
		<b>Single-ended Output referenced to Ground</b> F = 217Hz, $R_L = 16\Omega$ , $A_V = 2dB$ $V_{ripple} = 200mV_{pp}$ , Input Grounded, $C_b = 1\mu F$		63		

Table 7.  $V_{CC} = +5V$ ,  $GND = 0V$ ,  $T_{amb} = 25^{\circ}C$  (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Crosstalk	Channel Separation	$R_L = 32\Omega$ , $A_V = 2dB$ with Single-ended $F = 1kHz$ , $P_{out} = 50mW$		103		dB
		$R_L = 32\Omega$ , $A_V = 2dB$ with Single-ended $F = 20Hz$ to $20kHz$ , $P_{out} = 50mW$		75		
		$R_L = 32\Omega$ , $A_V = 2dB$ with Phantom Ground, $F = 1kHz$ , $P_{out} = 50mW$		69		
		$R_L = 32\Omega$ , $A_V = 2dB$ with Phantom Ground, $F = 20Hz$ to $20kHz$ , $P_{out} = 50mW$		69		
SNR	Signal To Noise Ratio, A-Weighted	$A_V = 2dB$ , $R_L = 32\Omega$ , $P_{out} = 62mW$ Single-Ended		95		dB
		$A_V = 2dB$ , $R_L = 32\Omega$ , $P_{out} = 62mW$ Phantom Ground		95		
ONoise	Output Noise Voltage, A-Weighted	$A_V = 2dB$ , Single-ended		23		$\mu V_{rms}$
		$A_V = 2dB$ , Phantom Ground		23		
G	Digital Gain Range	In1 & In2 to Out1 & Out2	-34		+18	dB
	Digital Gain Step size			4		dB
	Gain Error Tolerance		-1		+1	dB
$Z_{in}$	In1 & In2 Input Impedance	All gain settings	25.5	30	34.5	$k\Omega$
$t_{wu}$	Wake up time	$C_b = 1\mu F$		80	144	ms
$t_{ws}$	Standby time			1		$\mu s$

1. Dynamic measurements -  $20 \cdot \log(rms(V_{out})/rms(V_{ripple}))$ ,  $V_{ripple}$  is an added sinus signal to  $V_{CC}$  @  $F = 217Hz$

Figure 3. THD+N vs. output power

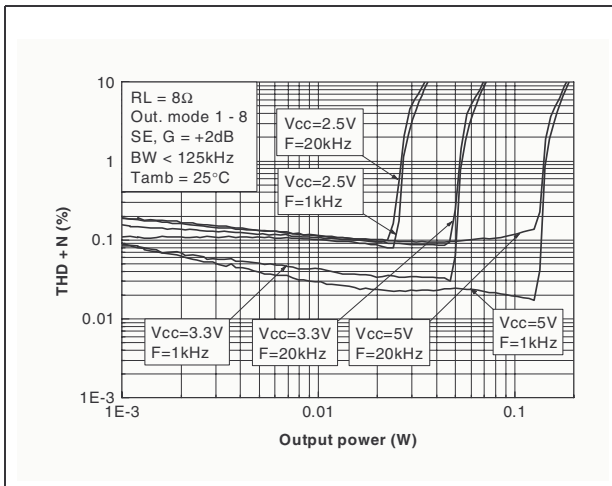


Figure 4. THD+N vs. output power

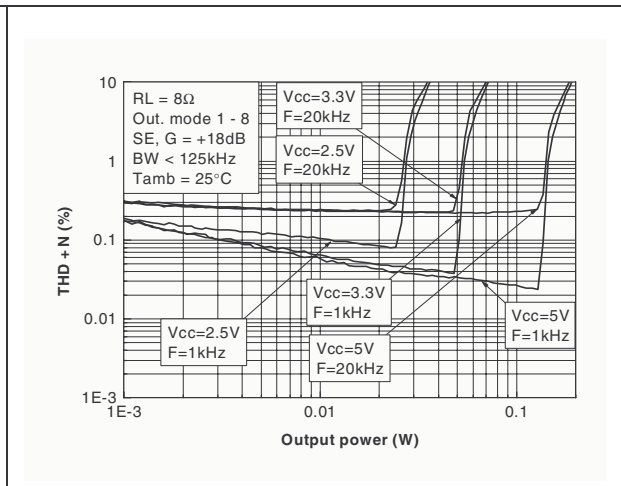


Figure 5. THD+N vs. output power

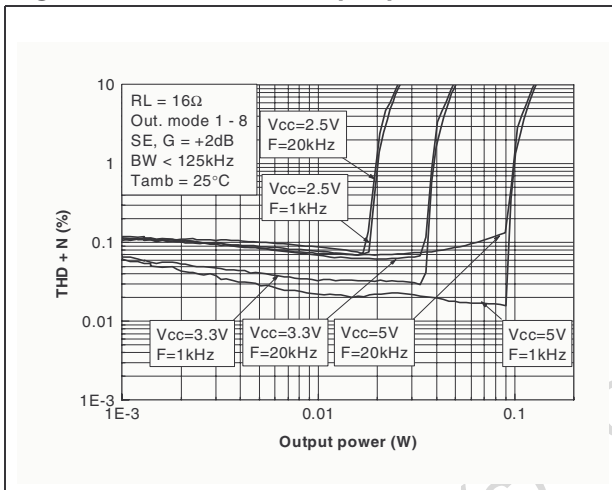


Figure 6. THD+N vs. output power

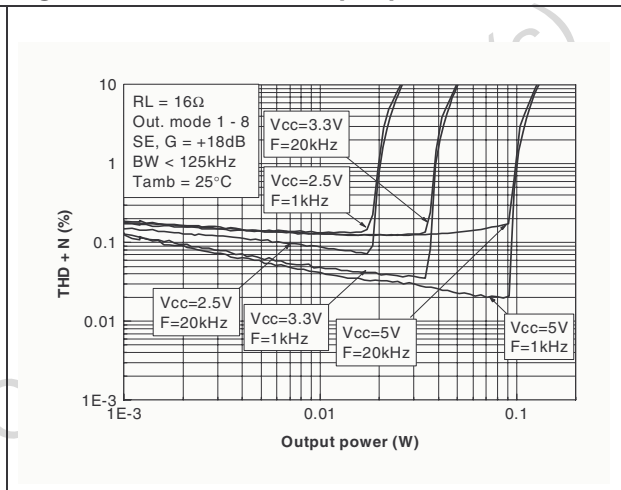


Figure 7. THD+N vs. output power

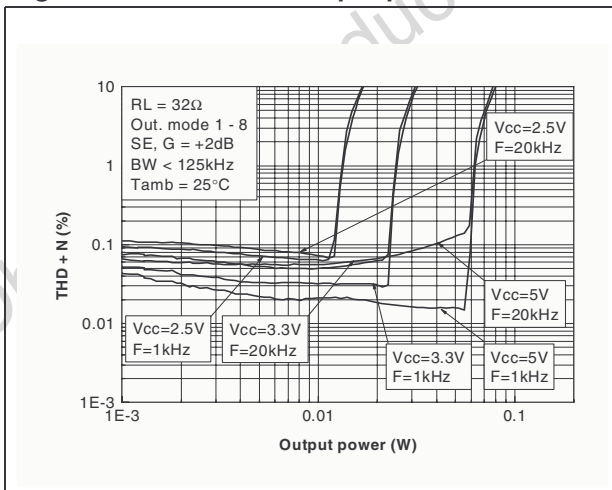


Figure 8. THD+N vs. output power

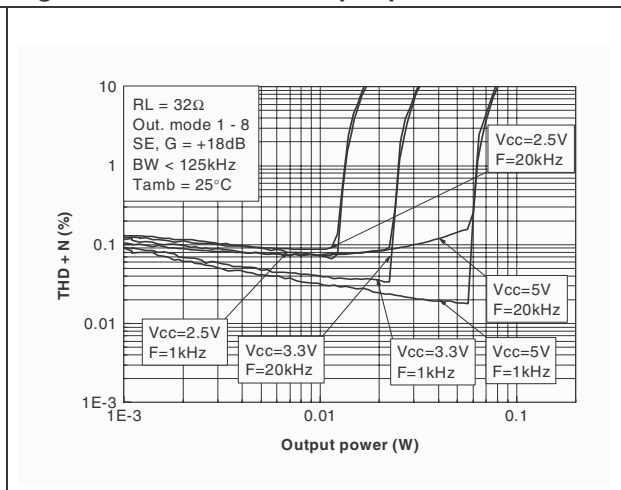


Figure 9. THD+N vs. output power

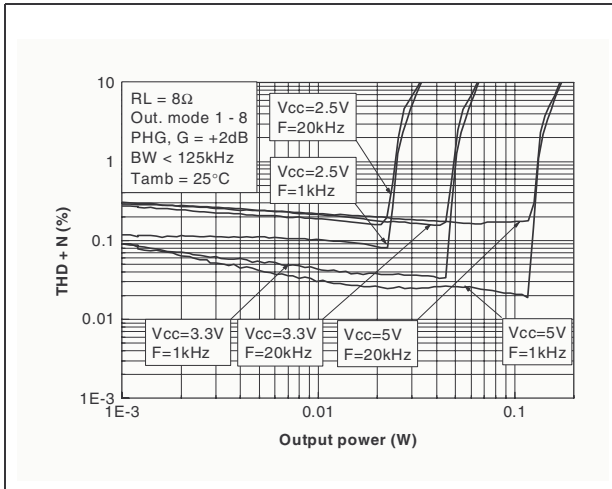


Figure 10. THD+N vs. output power

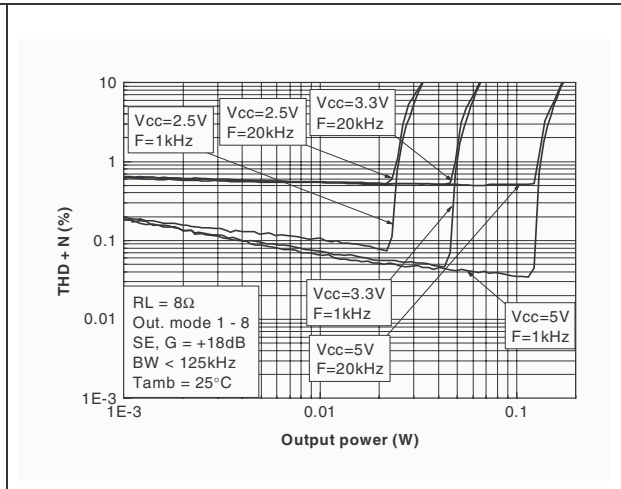


Figure 11. THD+N vs. output power

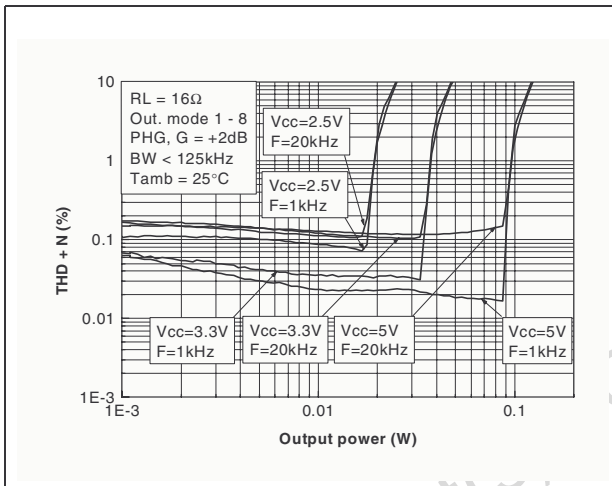


Figure 12. THD+N vs. output power

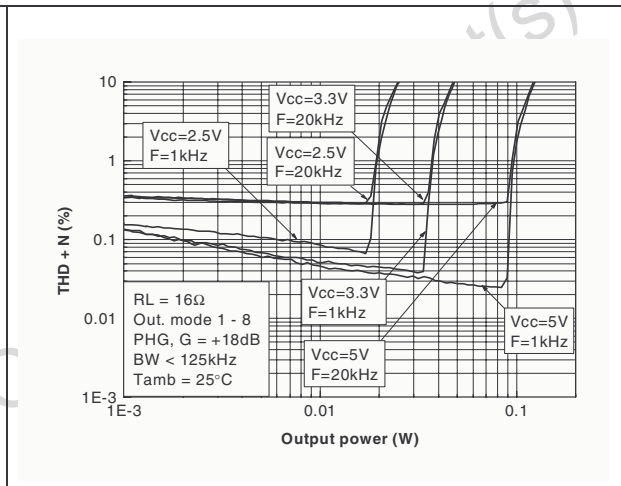


Figure 13. THD+N vs. output power

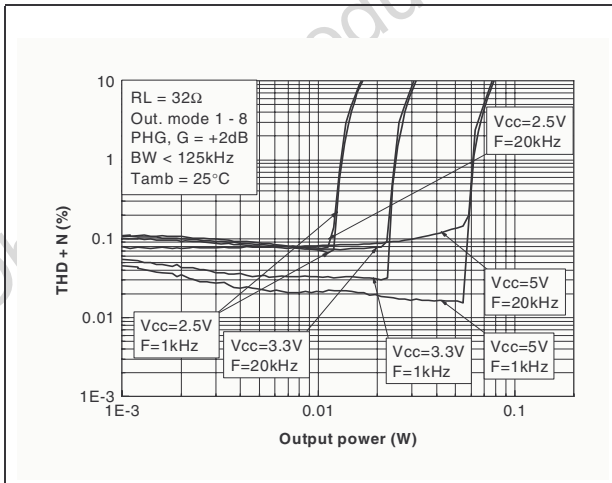


Figure 14. THD+N vs. output power

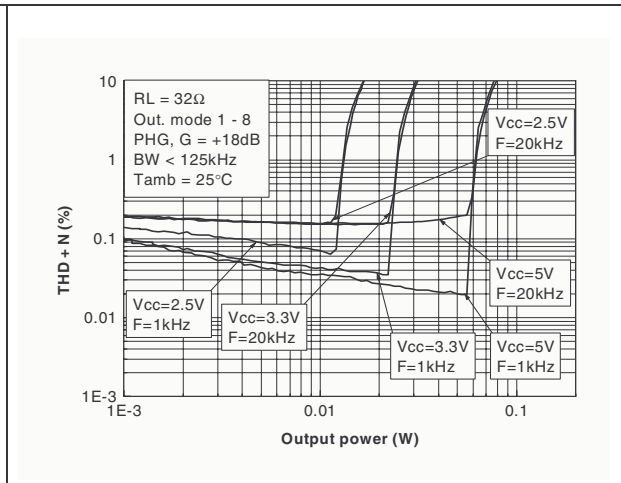


Figure 15. THD+N vs. frequency

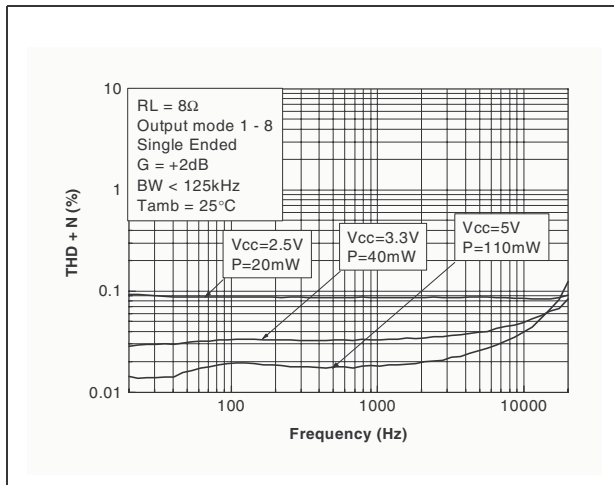


Figure 16. THD+N vs. frequency

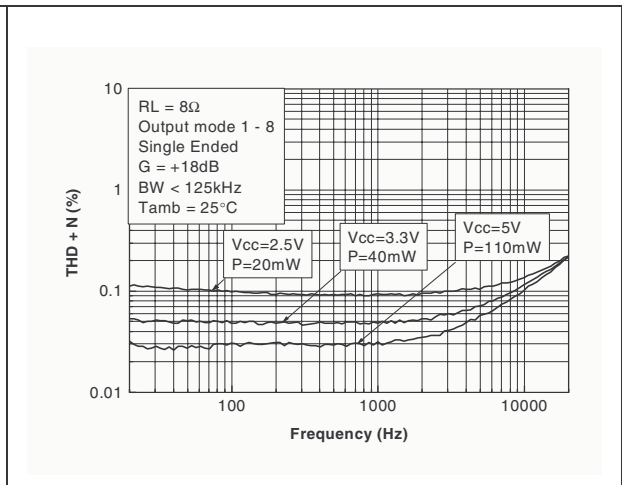


Figure 17. THD+N vs. frequency

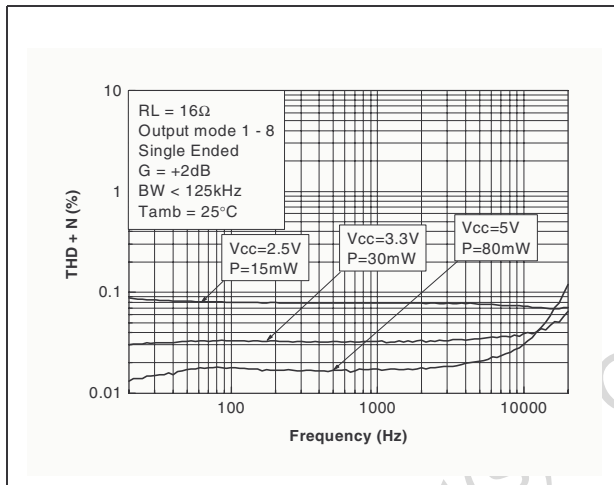


Figure 18. THD+N vs. frequency

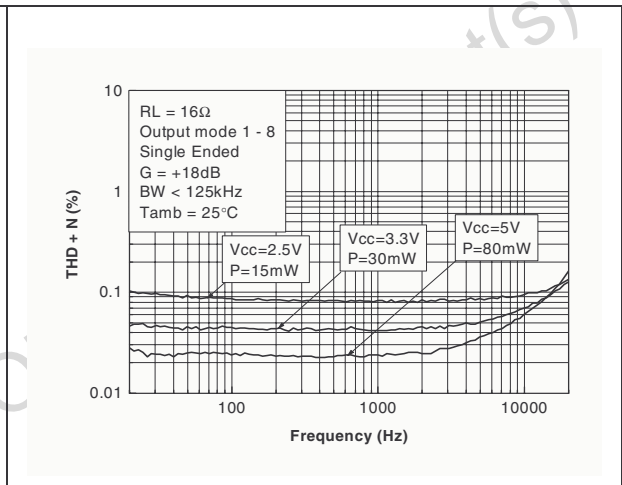


Figure 19. THD+N vs. frequency

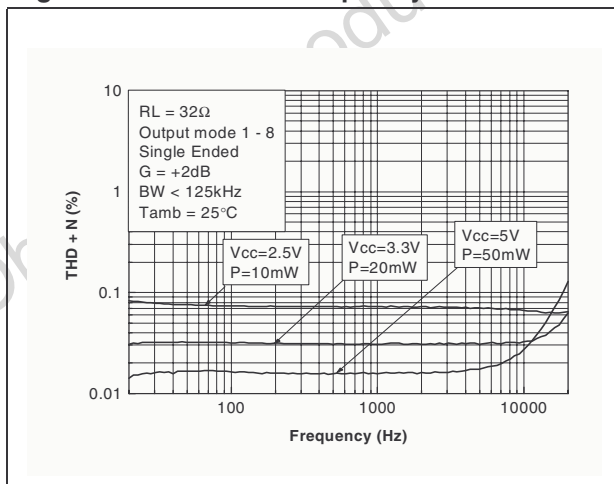


Figure 20. THD+N vs. frequency

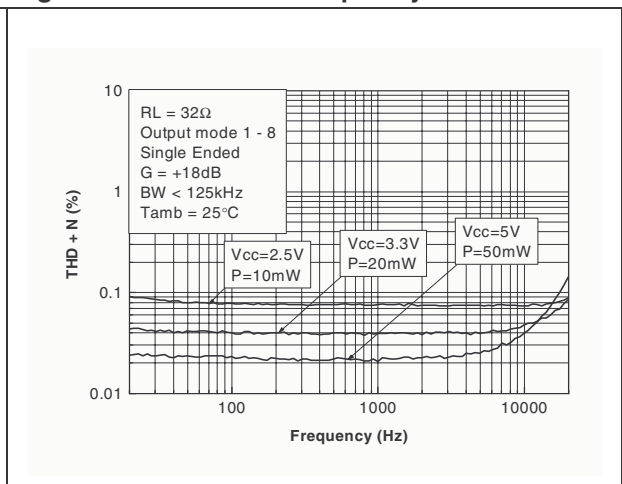


Figure 21. THD+N vs. frequency

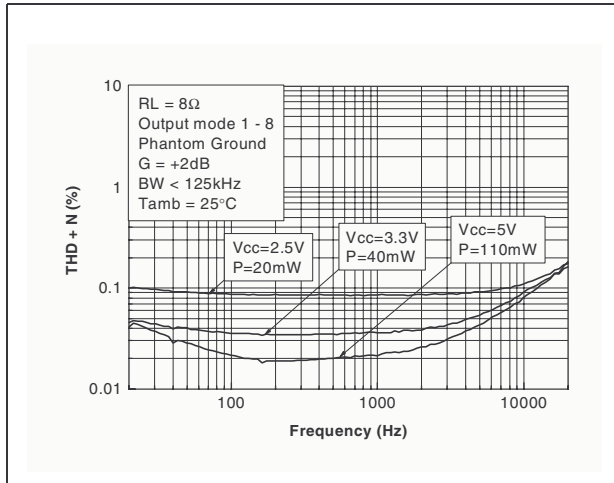


Figure 22. THD+N vs. frequency

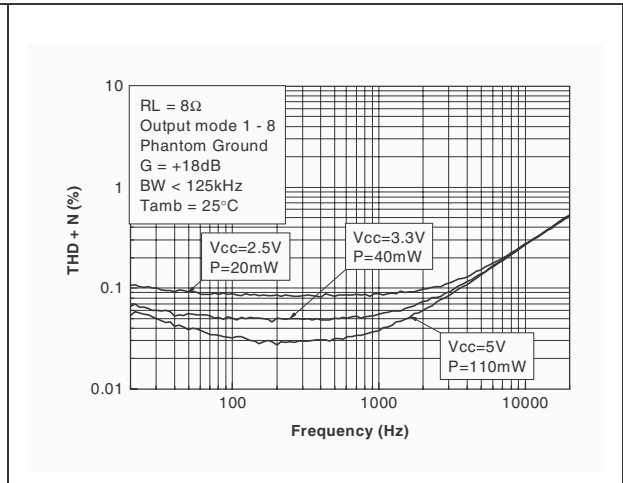


Figure 23. THD+N vs. frequency

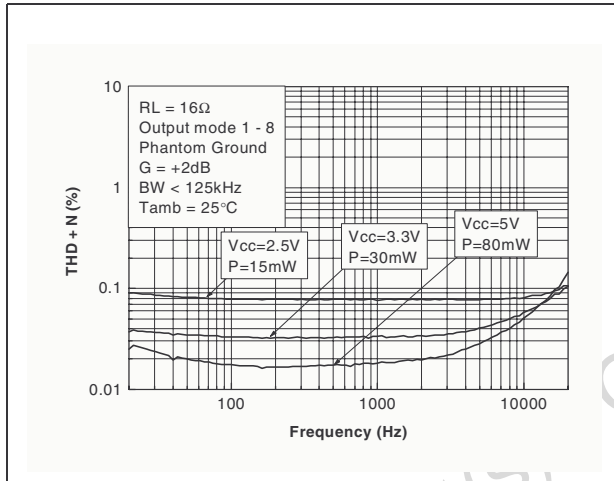


Figure 24. THD+N vs. frequency

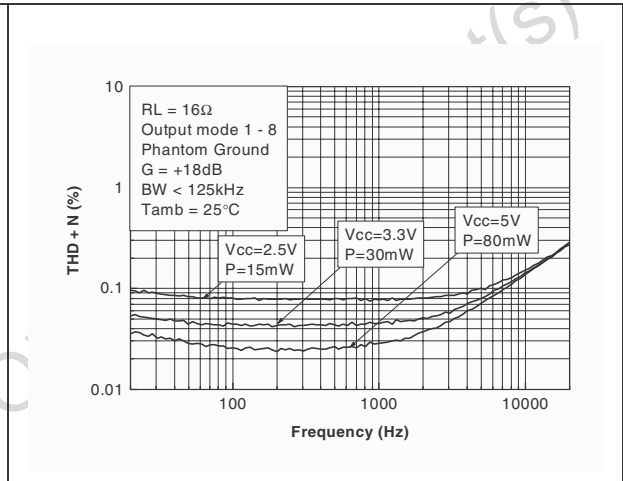


Figure 25. THD+N vs. frequency

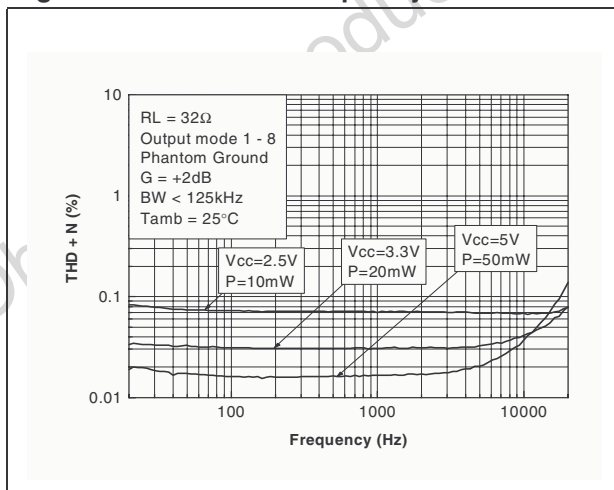


Figure 26. THD+N vs. frequency

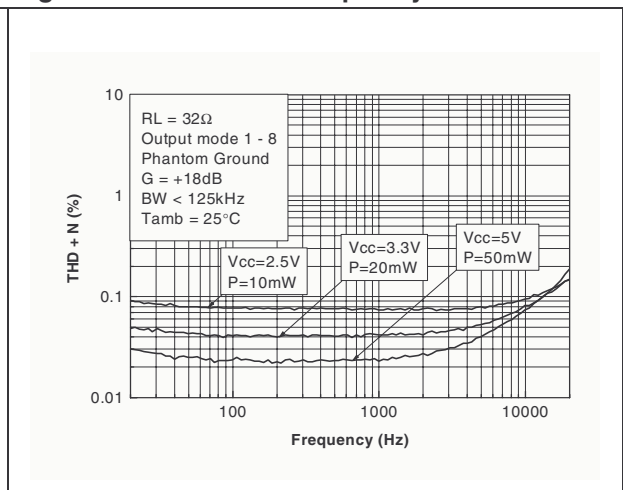


Figure 27. Output power vs. power supply voltage (each channel)

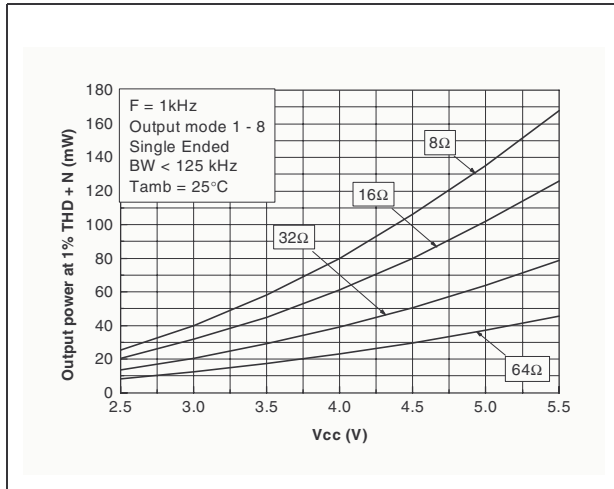


Figure 28. Output power vs. power supply voltage (each channel)

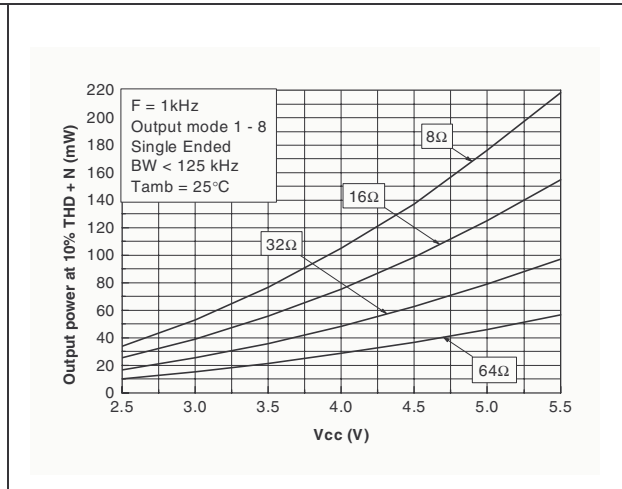


Figure 29. Output power vs. power supply voltage (each channel)

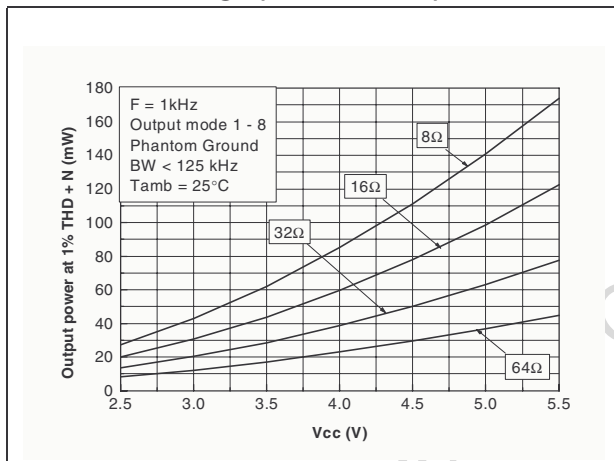
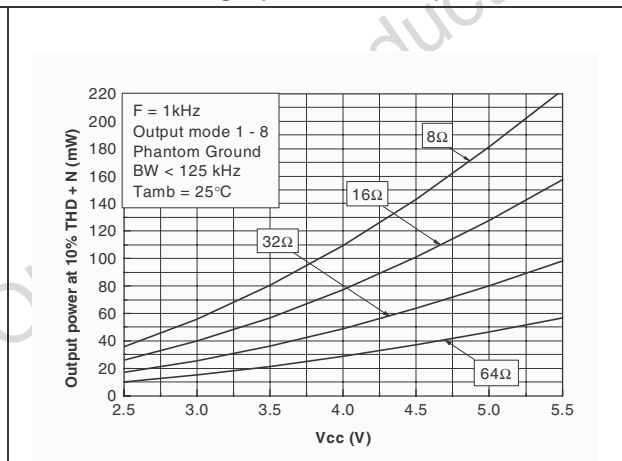


Figure 30. Output power vs. power supply voltage (each channel)



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Figure 31. PSSR vs. frequency

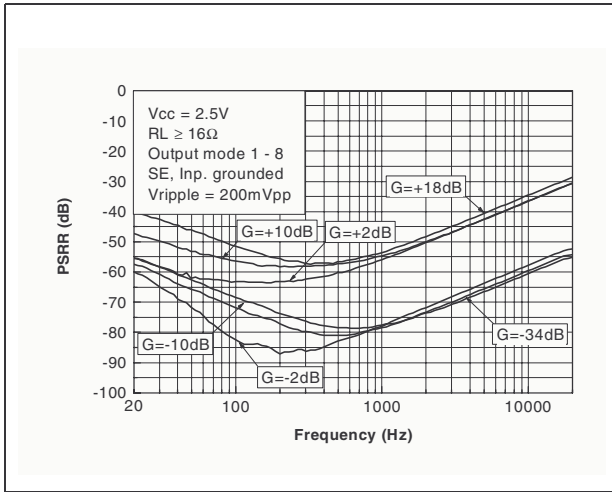


Figure 32. PSSR vs. frequency

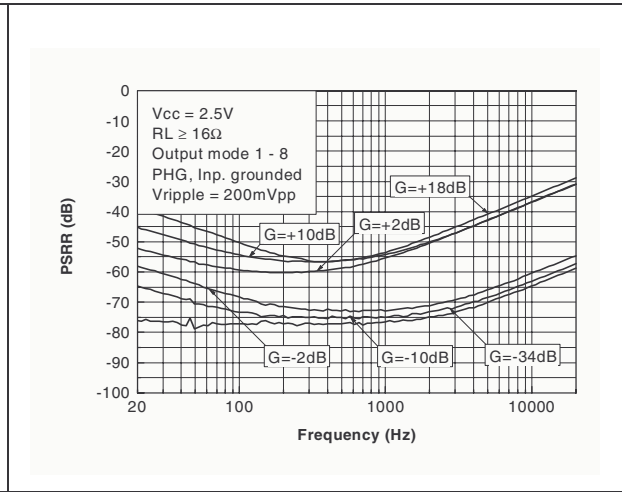


Figure 33. PSSR vs. frequency

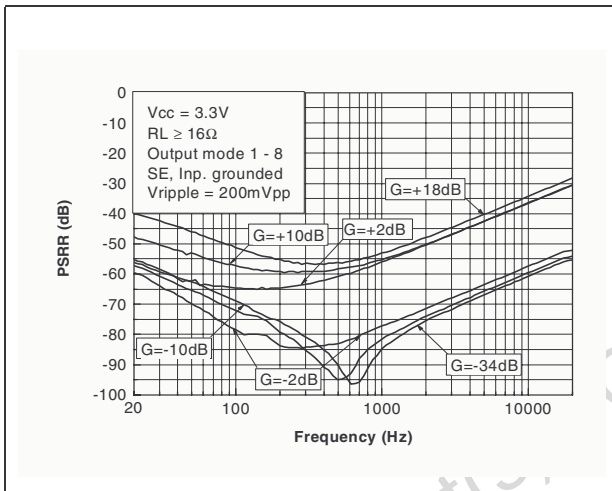


Figure 34. PSSR vs. frequency

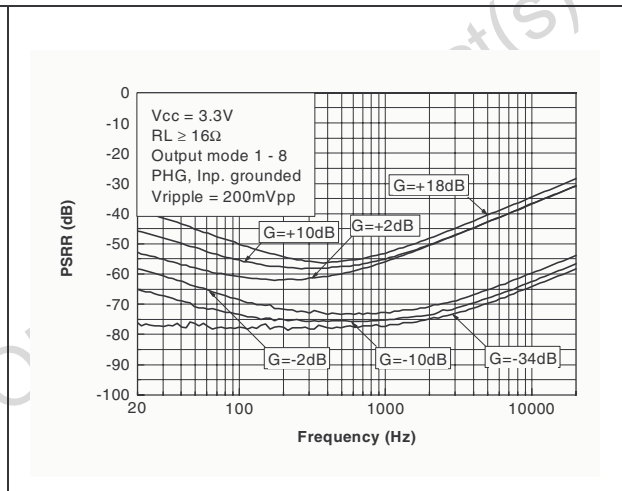


Figure 35. PSSR vs. frequency

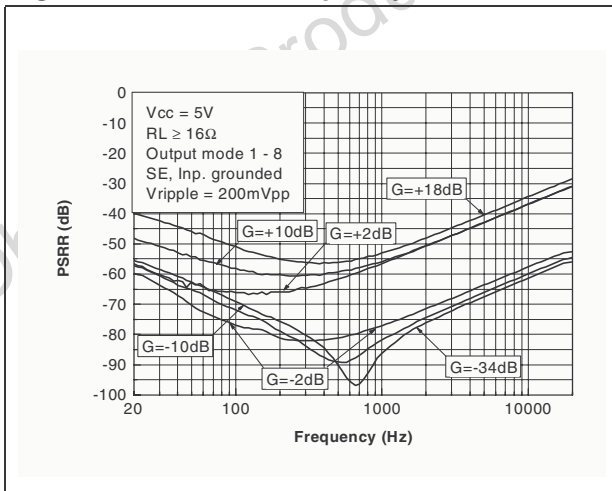


Figure 36. PSSR vs. frequency

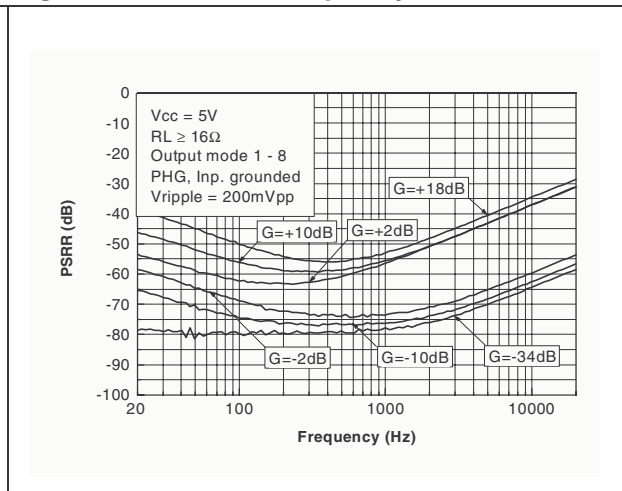


Figure 37. Crosstalk vs. frequency

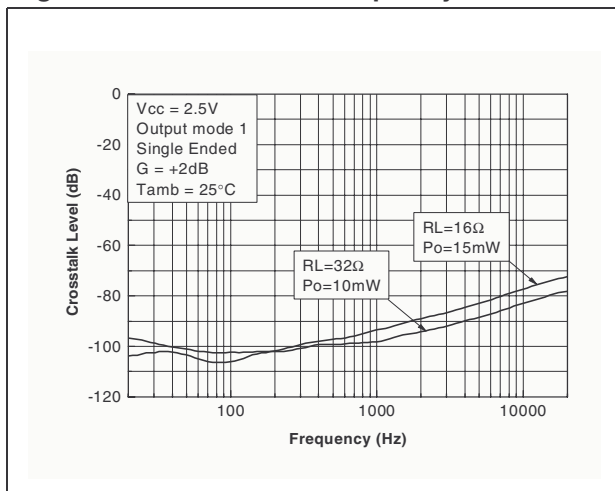


Figure 38. Crosstalk vs. frequency

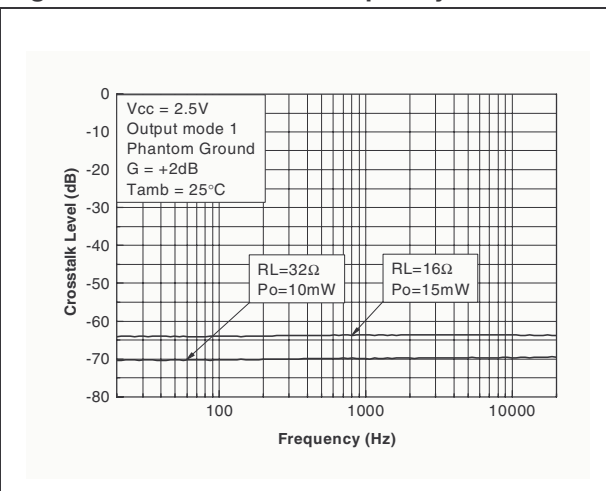


Figure 39. Crosstalk vs. frequency

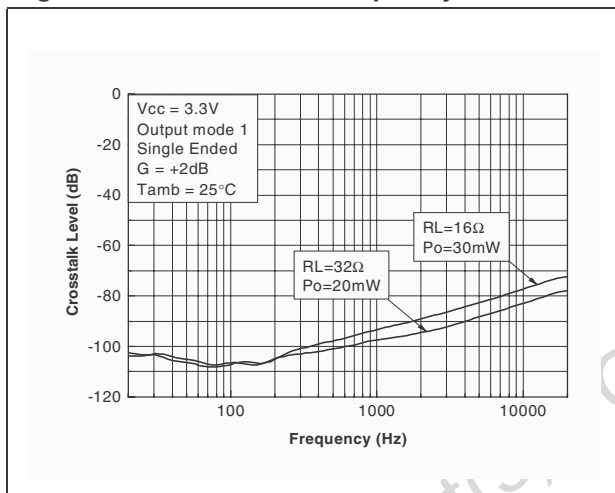


Figure 40. Crosstalk vs. frequency

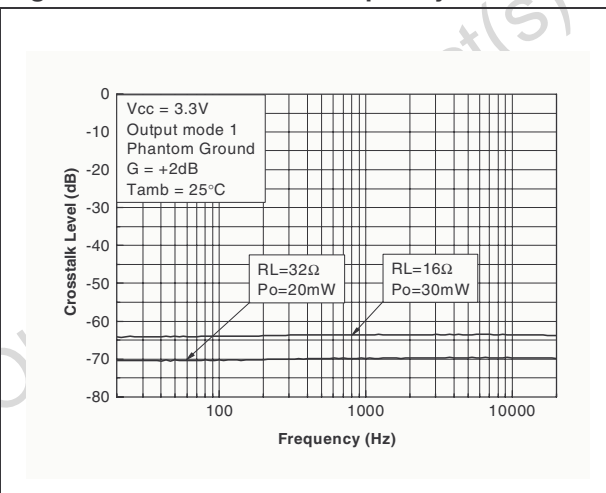


Figure 41. Crosstalk vs. frequency

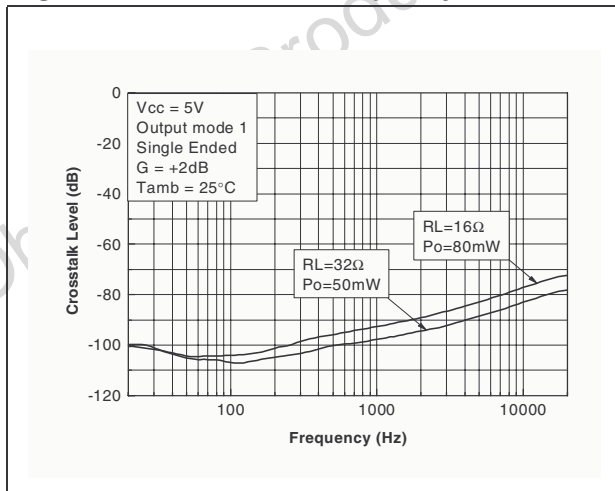


Figure 42. Crosstalk vs. frequency

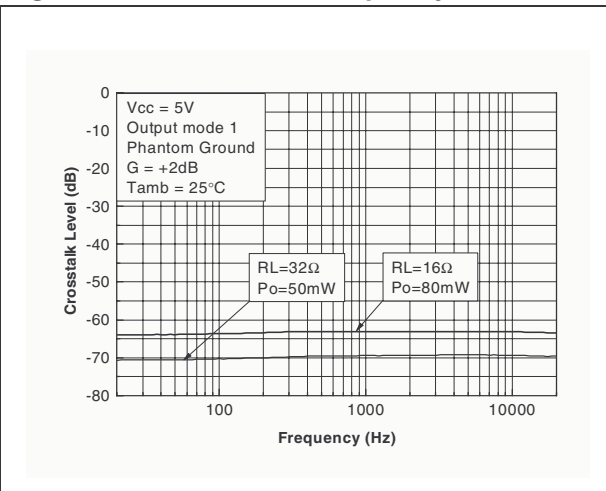


Figure 43. SNR vs. power supply voltage

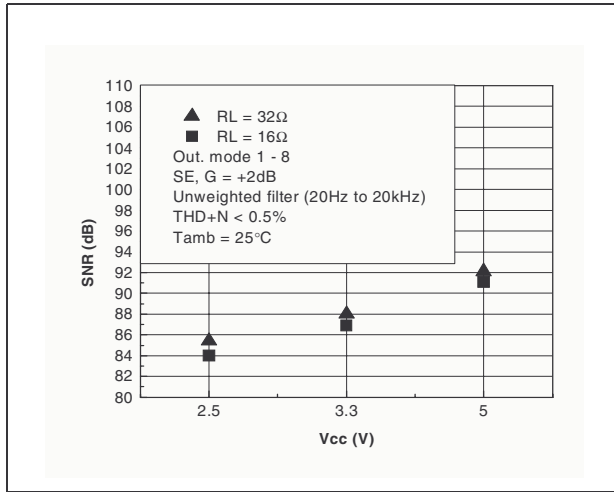


Figure 44. SNR vs. power supply voltage

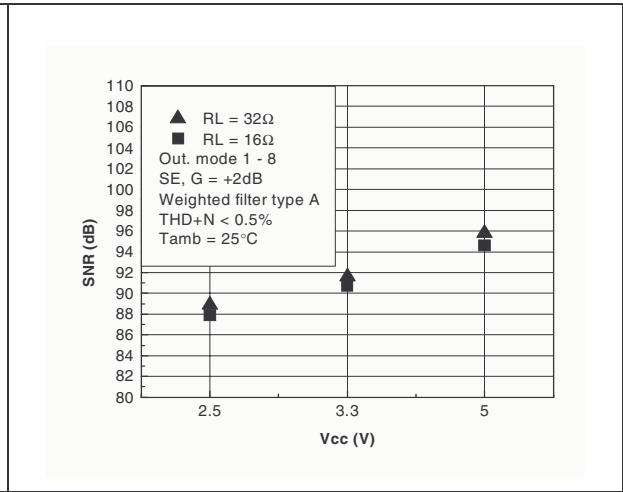


Figure 45. SNR vs. power supply voltage

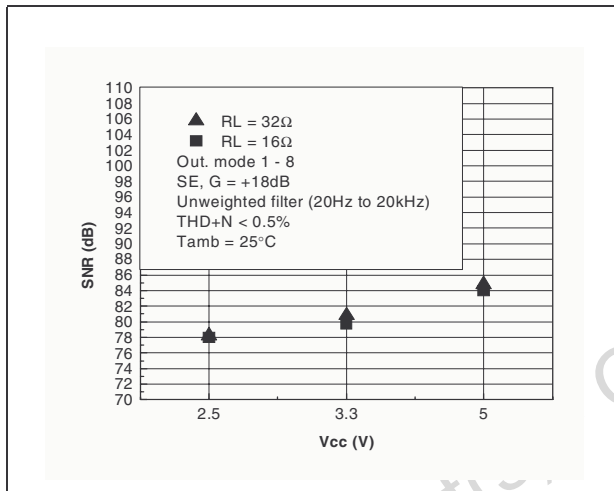


Figure 46. SNR vs. power supply voltage

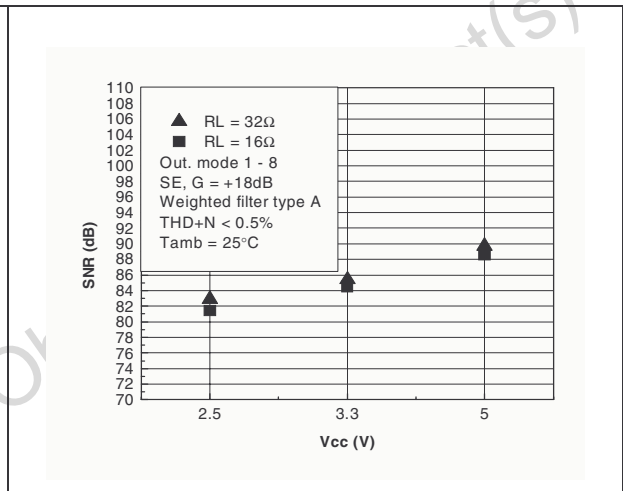


Figure 47. SNR vs. power supply voltage

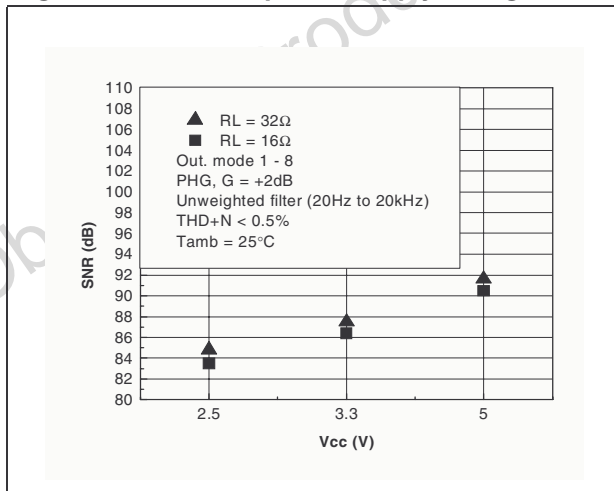


Figure 48. SNR vs. power supply voltage

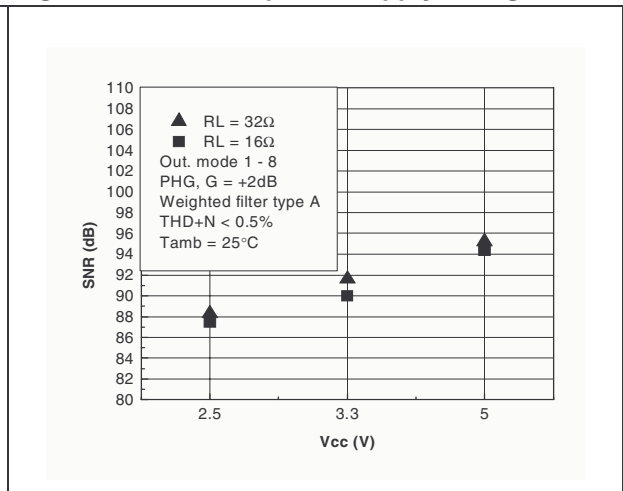


Figure 49. SNR vs. power supply voltage

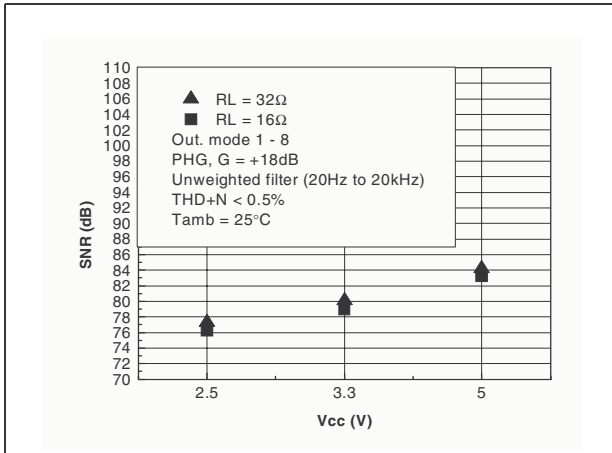


Figure 50. SNR vs. power supply voltage

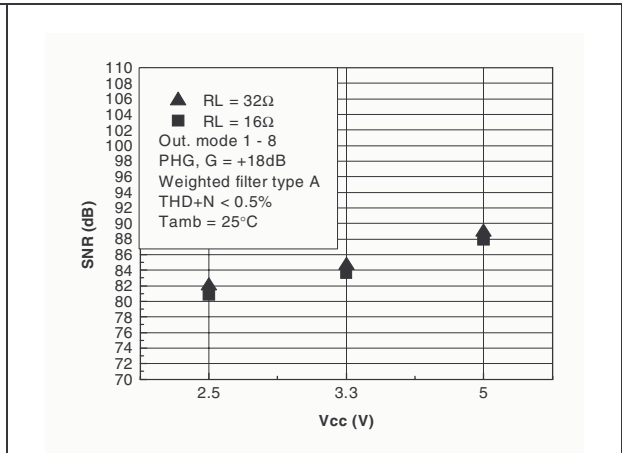


Figure 51. Frequency response

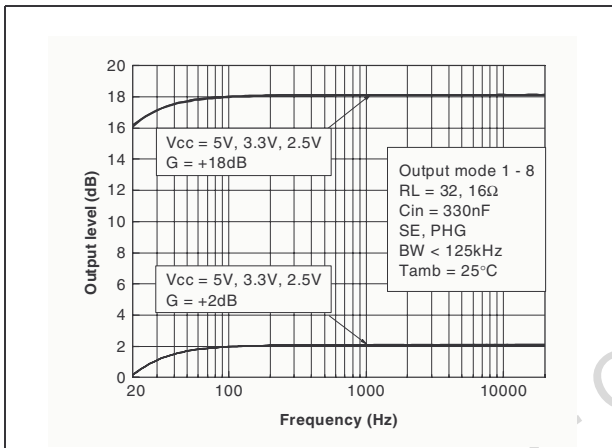


Figure 52. Current consumption vs. power supply voltage

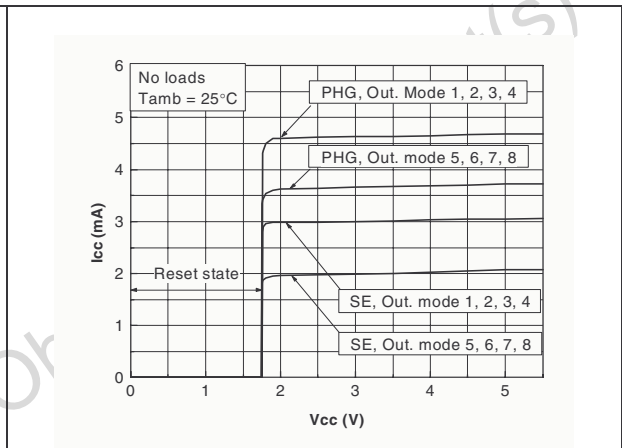


Figure 53. 3dB lower cut off frequency vs. input capacitance

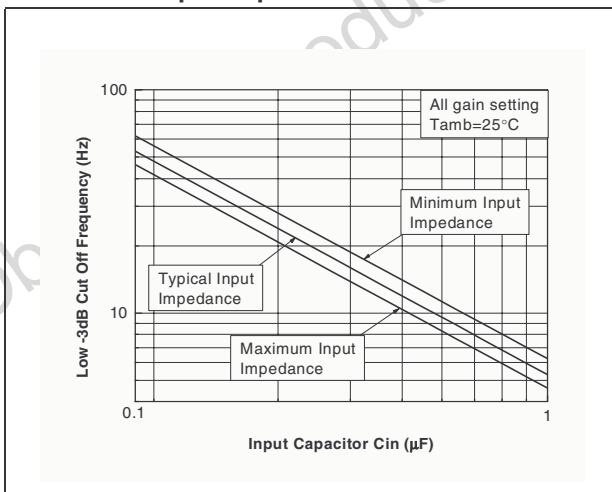


Figure 54. 3dB lower cut off frequency vs. output capacitance

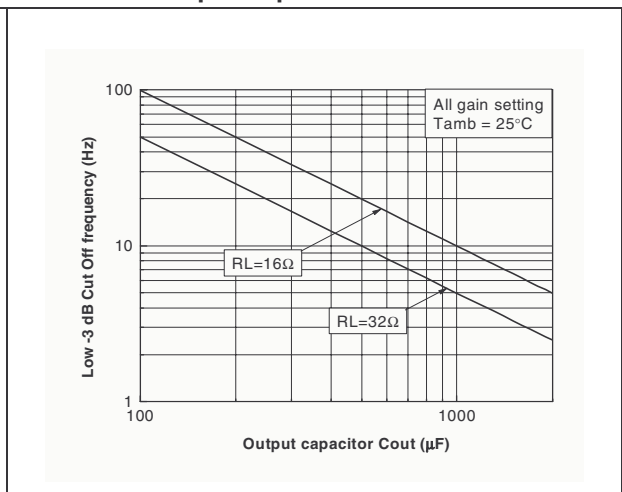


Figure 55. Power dissipation vs. output power (one channel)

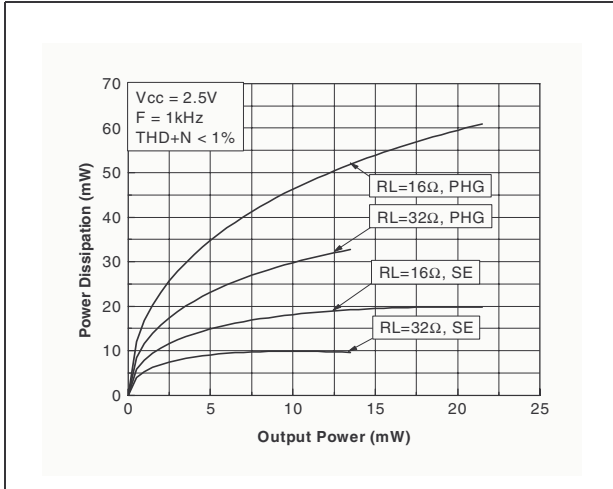


Figure 56. Power dissipation vs. output power (one channel)

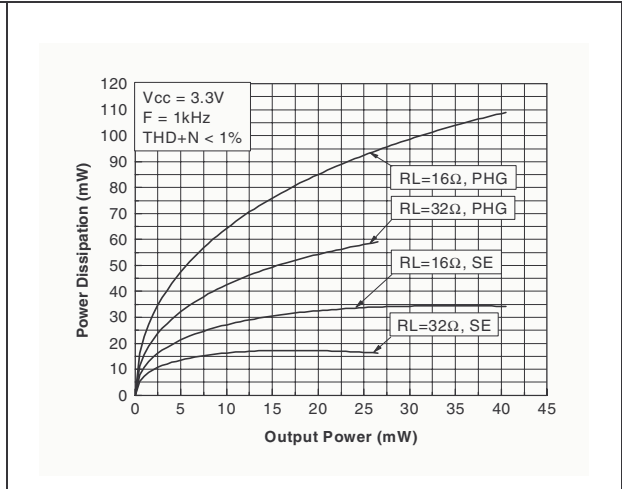


Figure 57. Power dissipation vs. output power (one channel)

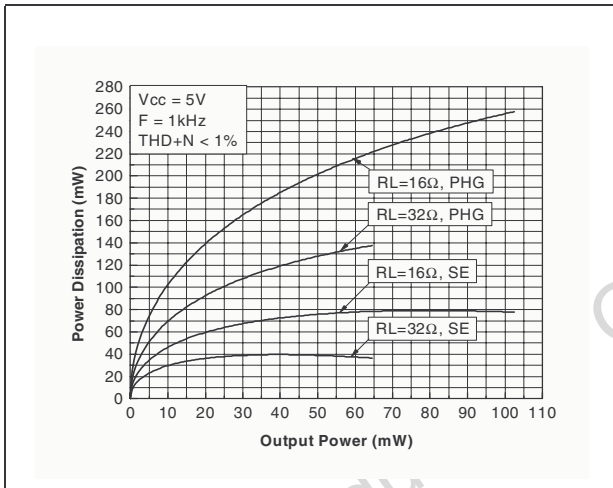
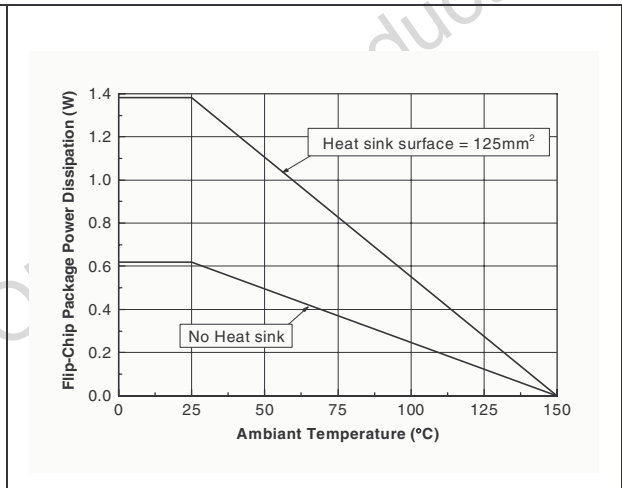


Figure 58. Power derating curves



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## 4 Application Information

The TS4975 integrates 2 monolithic power amplifiers. The amplifier output can be configured as either SE (single-ended) capacitively-coupled output or PHG (phantom ground) output. *Figure 1 on page 3* and *Figure 2 on page 4* show schemes of these two configurations and *Section 4.2: Output configuration* describes these configurations.

This chapter gives information on how to configure the TS4975 in application.

### 4.1 I<sup>2</sup>C bus interface

The TS4975 uses a serial bus, which conforms to the I<sup>2</sup>C protocol (the TS4975 must be powered when it is connected to I<sup>2</sup>C bus), to control the chip's functions with two wires: Clock and Data. The Clock line and the Data line are bi-directional (open-collector) with an external chip pull-up resistor (typically 10 kOhm). The maximum clock frequency in Fast-mode specified by the I<sup>2</sup>C standard is 400kHz, which TS4975 supports. In this application, the TS4975 is always the slave device and the controlling micro controller MCU is the master device.

The ADD pin is allows one to set one of two possible 7-bit device addresses. This setting is needed for when a number of chips are connected to the same bus (for example two TS4975 devices), to avoid address conflicts. The two possible TS4975 addresses are:

- \$CCh when the ADD pin is connected to logic low voltage,
- \$CEh when ADD pin is connected to logic high voltage.

*Table 8* summarizes the pin descriptions for the I<sup>2</sup>C bus interface.

**Table 8. I<sup>2</sup>C bus interface pin descriptions**

Pin	Functional Description
SDA	This is the serial data pin
SCL	This is the clock input pin
ADD	User-setable portion of device's I2C address

#### 4.1.1 I<sup>2</sup>C bus operation

The host MCU can write into the TS4975 control register to control the TS4975, and read from the control register to get a configuration from the TS4975. The TS4975 is addressed by the byte consisting of 7-bit slave address and R/W bit.

**Table 9. The first byte after the START message for addressing the device**

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	0	1	1	A0	X

In order to write data into the TS4975, after the "start" message, the MCU must send the following data:

- send byte with the I<sup>2</sup>C 7-bit slave address and with a low level for the R/W bit
- send the data (control register setting)

All bytes are sent with MSB bit first. The transfer of written data ends with a “stop” message. When transmitting several data, the data can be written with no need to repeat the “start” message and addressing byte with the slave address.

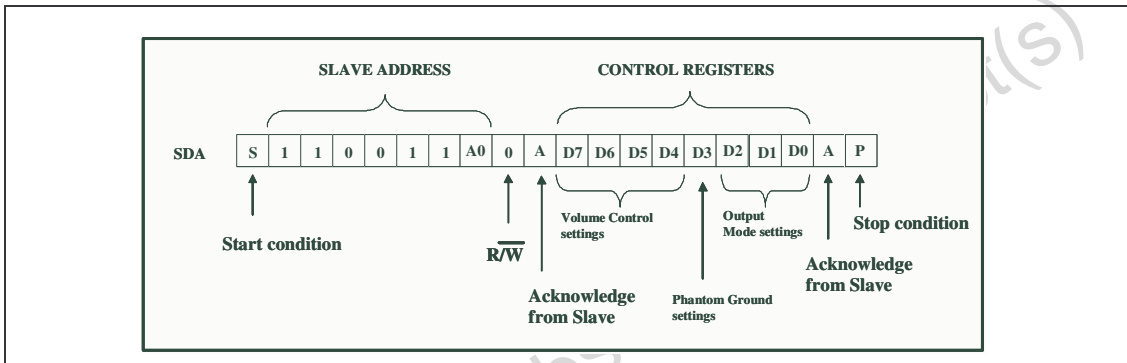
In order to read data from the TS4975, after the “start” message, the MCU must send and receive the following data:

- send byte with the I<sup>2</sup>C 7-bit slave address and with a high level for the R/W bit
- receive the data (control register value)

All bytes are read with MSB bit first. The transfer of read data is ended with “stop” message. When transmitting several data, the data can be read with no need to repeat the “start” message and the byte with slave address. In this case the value of control register is read repeatedly.

When the thermo shutdown or pop and click reduction is active, specific values are read from the TS4975 (see *Section 4.9: Pop and click performance on page 31* and *Section 4.10: Thermo shutdown on page 32*).

**Figure 59. I<sup>2</sup>C write/read operations**



**Table 10. Output mode selection: G from -34 dB to + 18dB (by steps of 4dB)<sup>(1)</sup>**

Output Mode #	Headphone Output 1	Headphone Output 2
0	SD	SD
1	G x In1	G x In2
2	G x In2	G x In1
3	G x In1	G x In1
4	G x In2	G x In2
5	SD	G x In1
6	SD	G x In2
7	G x In1	SD
8	G x In2	SD

1. SD = Shutdown Mode  
 In1 = Audio Input 1  
 In2= Audio Input2  
 G = Gain from Audio Input 1and Input 2 to Output1 and Output2

### 4.1.2 Gain setting operation

The gain of the TS4975 ranges from -34dB to +18 dB. At Power-up, both the right and left channels are set in Standby mode.

**Table 11. Gain settings truth table**

G: Gain (dB) #	D7 (MSB)	D6	D5	D4
-34	0	0	0	1
-30	0	0	1	0
-26	0	0	1	1
-22	0	1	0	0
-18	0	1	0	1
-14	0	1	1	0
-10	0	1	1	1
-6	1	0	0	0
-2	1	0	0	1
+2	1	0	1	0
+6	1	0	1	1
+10	1	1	0	0
+14	1	1	0	1
+18	1	1	1	0

**Table 12. Output mode settings truth table**

D3: PHG on / off	D2	D1	D0	COMMENTS
0	X	X	X	PHG off
1	x	x	x	PHG on
x	0	0	0	MODE 1
X	0	0	1	MODE 2
X	0	1	0	MODE 3
X	0	1	1	MODE4
X	1	0	0	MODE 5
X	1	0	1	MODE 6
X	1	1	0	MODE 7
X	1	1	1	MODE 8

**Table 13. Stand-by mode I<sup>2</sup>C condition**

D7 (MSB)	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	X	X	X	X



Table 14. I<sup>2</sup>C control byte states

D7 (MSB)	D6	D5	D4	D3	D2	D1	D0	
1	1	1	1	x	X	X	X	Undefined State

### 4.1.3 Acknowledge

The number of data bytes transferred between the start and the stop conditions from the CPU master to the TS4975 slave is not limited. Each byte of eight bits is followed by one acknowledge bit.

The TS4975 which is addressed, generates an acknowledge after the reception of each byte that has been clocked out.

## 4.2 Output configuration

When the device is switched to Mode 5,6,7 or 8, where one channel is in shutdown, it means that corresponding output is in a high impedance state.

### 4.2.1 Single-ended configuration

When the device is woken-up or switched via I<sup>2</sup>C interface to SE configuration, output amplifiers are biased to the  $V_{CC}/2$  voltage and this voltage is present on OUT1 and OUT2 pins. Pins PHG1 and PHG2 are in high impedance state. In this configuration an output capacitor,  $C_{out}$ , on each output is needed to block the  $V_{CC}/2$  voltage and couples the audio signal to the load.

### 4.2.2 Phantom ground configuration

In a PHG configuration the internal buffers are connected to PHG1 and PHG2 pins and biased to the  $V_{CC}/2$  voltage. Output amplifiers (pins OUT1 and OUT2) are also biased to the  $V_{CC}/2$  voltage. Therefore, no output capacitors are needed. The advantage of the PHG configuration is the need for fewer external components as compared with a SE configuration. However, note that the device has higher power dissipation (see [Section 4.3: Power dissipation and efficiency on page 26](#)).

In this configuration, PHG1 and PHG2 pins must be shorted and the connection between these pins should be as short as possible. For best crosstalk results, in this case, each speaker should be connected with a separate PHG wire (2 speakers connected with 4 wires) as shown in [Figure 2: Phantom ground output configuration on page 4](#). You should avoid using only one common PHG wire for both speakers (i.e. 2 speakers connected with 3 wires), which would give much poorer crosstalk results.

### 4.2.3 Shutdown

When the device goes to shutdown from SE or PHG mode, PHG1 and PHG2 outputs are in a high impedance state and OUT1 and OUT2 outputs are shorted together and connected to bias voltage. This voltage steadily decreases as the bypass capacitor  $C_b$  discharges, and reaches GND voltage when  $C_{bypass}$  is fully discharged. This output configuration is implemented to reach the best pop performance during chip wake-up.

### 4.3 Power dissipation and efficiency

**Hypotheses:**

- Voltage and current in the load are sinusoidal ( $V_{out}$  and  $I_{out}$ ).
- Supply voltage is a pure DC source ( $V_{CC}$ ).

Regarding the load we have:

$$V_{out} = V_{PEAK} \sin \omega t \text{ (V)}$$

and

$$I_{out} = \frac{V_{out}}{R_L} \text{ (A)}$$

and

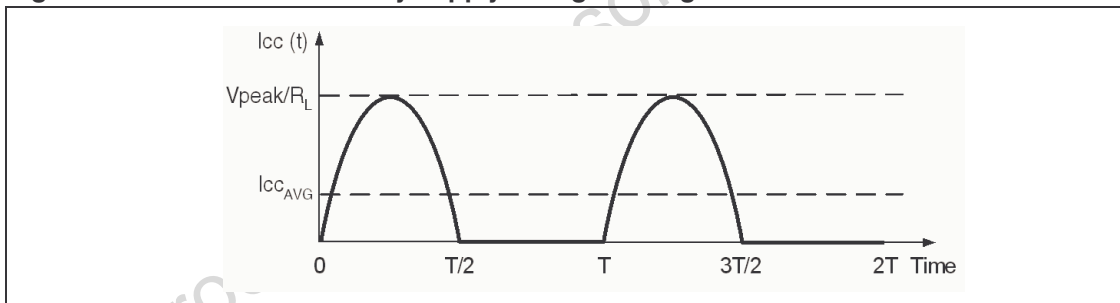
$$P_{out} = \frac{V_{PEAK}^2}{2R_L} \text{ (A)}$$

**Single-ended configuration:**

The average current delivered by the supply voltage is:

$$I_{CC_{AVG}} = \frac{1}{2\pi} \int_0^\pi \frac{V_{PEAK}}{R_L} \sin(t) dt = \frac{V_{PEAK}}{\pi R_L} \text{ (A)}$$

**Figure 60. Current delivered by supply voltage in single-ended model**



The power delivered by supply voltage is:

$$P_{supply} = V_{CC} I_{CC_{AVG}} \text{ (W)}$$

So, the **power dissipation by each amplifier** is

$$P_{diss} = P_{supply} - P_{out} \text{ (W)}$$

$$P_{diss} = \frac{\sqrt{2} V_{CC}}{\pi \sqrt{R_L}} \sqrt{P_{out}} - P_{out} \text{ (W)}$$

and the maximum value is obtained when:

$$\frac{\partial P_{diss}}{\partial P_{out}} = 0$$

and its value is:

$$P_{diss_{MAX}} = \frac{V_{CC}^2}{\pi^2 R_L} \quad (W)$$

*Note:* This maximum value depends only on power supply voltage and load values.

The **efficiency** is the ratio between the output power and the power supply:

$$\eta = \frac{P_{out}}{P_{supply}} = \frac{\pi V_{PEAK}}{2V_{CC}}$$

The maximum theoretical value is reached when  $V_{PEAK} = V_{CC}/2$ , so

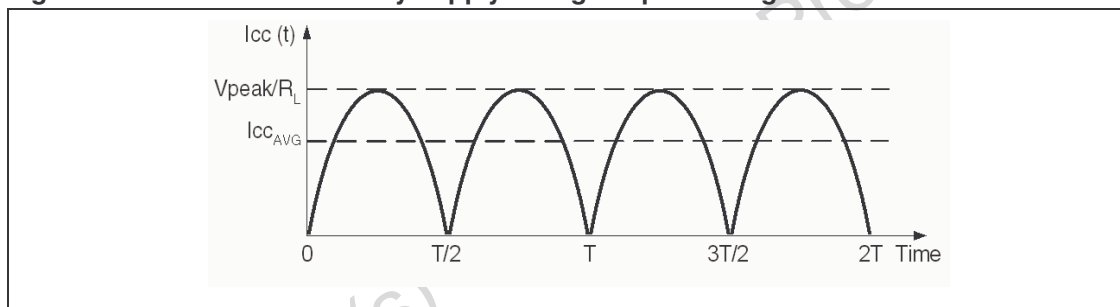
$$\eta = \frac{\pi}{4} = 78.5\%$$

**Phantom ground configuration:**

The average current delivered by the supply voltage is:

$$I_{CC_{AVG}} = \frac{1}{\pi} \int_0^{\pi} \frac{V_{PEAK}}{R_L} \sin(t) dt = \frac{2V_{PEAK}}{\pi R_L} \quad (A)$$

**Figure 61. Current delivered by supply voltage in phantom ground mode**



The power delivered by supply voltage is:

$$P_{supply} = V_{CC} I_{CC_{AVG}} \quad (W)$$

Then, the power dissipation by each amplifier is

$$P_{diss} = \frac{2\sqrt{2}V_{CC}}{\pi\sqrt{R_L}} \sqrt{P_{out}} - P_{out} \quad (W)$$

and the maximum value is obtained when:

$$\frac{\partial P_{diss}}{\partial P_{out}} = 0$$

and its value is:

$$P_{diss_{MAX}} = \frac{2V_{CC}^2}{\pi^2 R_L} \quad (W)$$

*Note:* This maximum value depends only on power supply voltage and load values.

The efficiency is the ratio between the output power and the power supply:

$$\eta = \frac{P_{\text{out}}}{P_{\text{supply}}} = \frac{\pi V_{\text{PEAK}}}{4V_{\text{CC}}}$$

The maximum theoretical value is reached when  $V_{\text{PEAK}} = V_{\text{CC}}/2$ , so

$$\eta = \frac{\pi}{8} = 39.25\%$$

The TS4975 is a stereo amplifier so it has two independent power amplifiers. Each amplifier produces heat due to its power dissipation. Therefore the maximum die temperature is the sum of each amplifier's maximum power dissipation. It is calculated as follows:

$P_{\text{diss } 1}$  = Power dissipation due to the first channel power amplifier.

$P_{\text{diss } 2}$  = Power dissipation due to the second channel power amplifier.

$$\text{Total } P_{\text{diss}} = P_{\text{diss } 1} + P_{\text{diss } 2} \text{ (W)}$$

In most cases,  $P_{\text{diss } 1} = P_{\text{diss } 2}$ , giving:

$$\text{Total } P_{\text{diss}} = 2P_{\text{diss } 1}$$

**Single ended configuration:**

$$\text{Total } P_{\text{diss}} = \frac{2\sqrt{2}V_{\text{CC}}}{\pi\sqrt{R_L}}\sqrt{P_{\text{out}}} - 2P_{\text{out}} \text{ (W)}$$

**Phantom ground configuration:**

$$\text{Total } P_{\text{diss}} = \frac{4\sqrt{2}V_{\text{CC}}}{\pi\sqrt{R_L}}\sqrt{P_{\text{out}}} - 2P_{\text{out}} \text{ (W)}$$

## 4.4 Low frequency response

### Input capacitor $C_{\text{in}}$

The input coupling capacitor blocks the DC part of the input signal at the amplifier input. In the low-frequency region,  $C_{\text{in}}$  starts to have an effect.  $C_{\text{in}}$  with  $Z_{\text{in}}$  forms a first-order, high-pass filter with -3 dB cut-off frequency.

$$F_{\text{CL}} = \frac{1}{2\pi Z_{\text{in}} C_{\text{in}}} \text{ (Hz)}$$

$Z_{\text{in}}$  is the input impedance of the corresponding input (30 k $\Omega$  for In1 & In2).

**Note:** For all inputs, the impedance value remains for all gain settings. This means that the lower cut-off frequency doesn't change with gain setting. Note also that 30 k $\Omega$  is a typical value and there is tolerance around this value (see Chapter 3: Electrical Characteristics on page 5).

From Figure 53 you could easily establish the  $C_{\text{in}}$  value for a -3dB cut-off frequency required.

### Output capacitor $C_{out}$

In single-ended mode the external output coupling capacitors  $C_{out}$  are needed. This coupling capacitor  $C_{out}$  with the output load  $R_L$  also forms a first-order high-pass filter with -3 dB cut off frequency.

$$F_{CL} = \frac{1}{2\pi R_L C_{out}} \text{ (Hz)}$$

See *Figure 54* to establish the  $C_{out}$  value for a -3dB cut-off frequency required.

These two first-order filters form a second-order high-pass filter. The -3 dB cut-off frequency of these two filters should be the same, so the following formula should be respected:

$$\frac{1}{2\pi Z_{in} C_{in}} \cong \frac{1}{2\pi R_L C_{out}}$$

## 4.5 Decoupling of the circuit

Two capacitors are needed to properly bypass the TS4975 — a power supply capacitor  $C_s$  and a bias voltage bypass capacitor  $C_b$ .

$C_s$  has a strong influence on the THD+N in high frequency (above 7kHz) and indirectly on the power supply disturbances.

With 1  $\mu\text{F}$ , you could expect similar THD+N performances like shown in the datasheet.

If  $C_s$  is lower than 1  $\mu\text{F}$ , THD+N increases in high frequency and disturbances on power supply rail are less filtered.

To the contrary, if  $C_s$  is higher than 1  $\mu\text{F}$ , those disturbances on the power supply rail are more filtered.

$C_b$  has an influence on THD+N in lower frequency, but its value is critical on the final result of PSRR with input grounded in lower frequency:

- If  $C_b$  is lower than 1  $\mu\text{F}$ , THD+N increases at lower frequencies and the PSRR worsens upwards.
- If  $C_b$  is higher than 1  $\mu\text{F}$ , the benefit on THD+N and PSRR in the lower frequency range is small.

The value of  $C_b$  also has an influence on startup time.

## 4.6 Power-on reset

When power is applied to  $V_{CC}$ , an internal Power On Reset holds the TS4975 in a reset state (shutdown) until the supply voltage reaches its nominal value. The Power On Reset has a typical threshold of 1.75V.

During this reset state the outputs configuration is the same like in the shutdown mode (see *Section 4.2: Output configuration on page 25*).

## 4.7 Notes on PSRR measurement

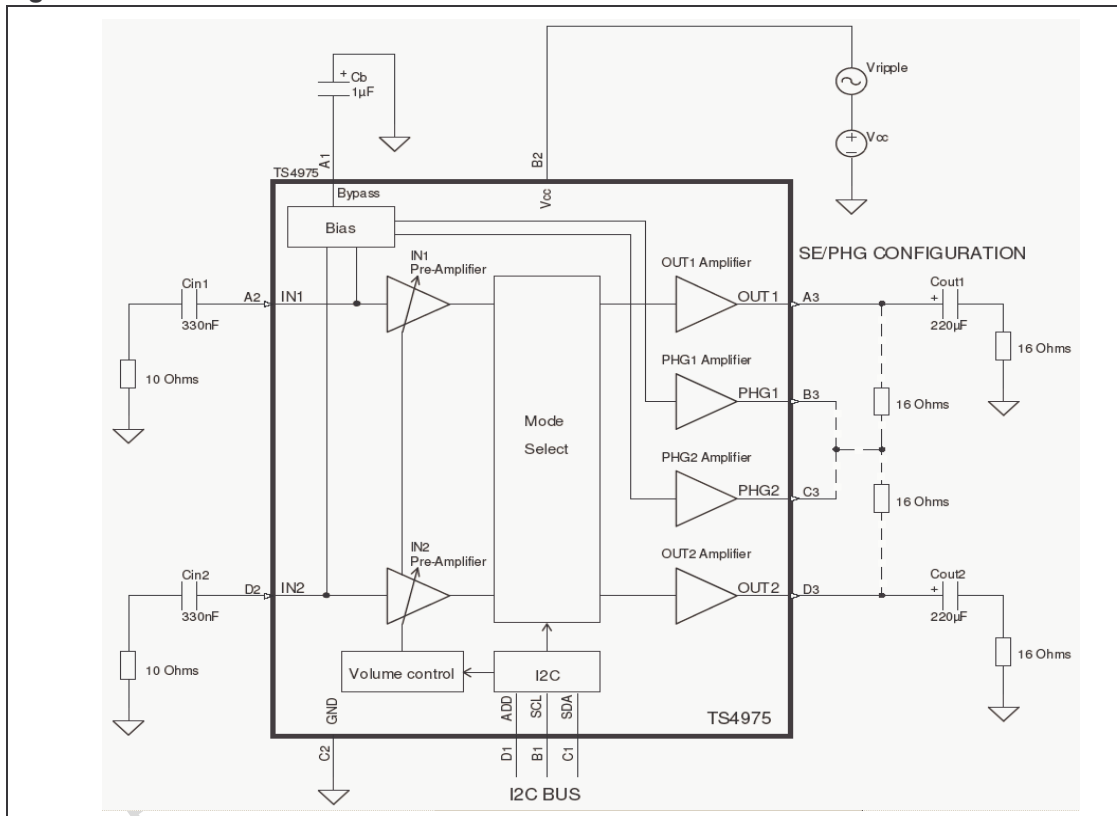
### What is PSRR?

The PSRR is the Power Supply Rejection Ratio. The PSRR of a device is the ratio between a power supply disturbance and the result on the output. In other words, the PSRR is the ability of a device to minimize the impact of power supply disturbance to the output.

### How we measure the PSRR?

The PSRR was measured according to the schematic shown in *Figure 62*.

**Figure 62. PSRR measurement schematic**



### Principles of operation

- The DC voltage supply ( $V_{CC}$ ) is fixed
- The AC sinusoidal ripple voltage ( $V_{ripple}$ ) is fixed
- No bypass capacitor  $C_s$  is used

The PSRR value for each frequency is calculated as:

$$PSRR = 20 \log \left[ \frac{RMS_{(Output)}}{RMS_{(V_{ripple})}} \right] (dB)$$

RMS is a rms selective measurement.

### 4.8 Startup time

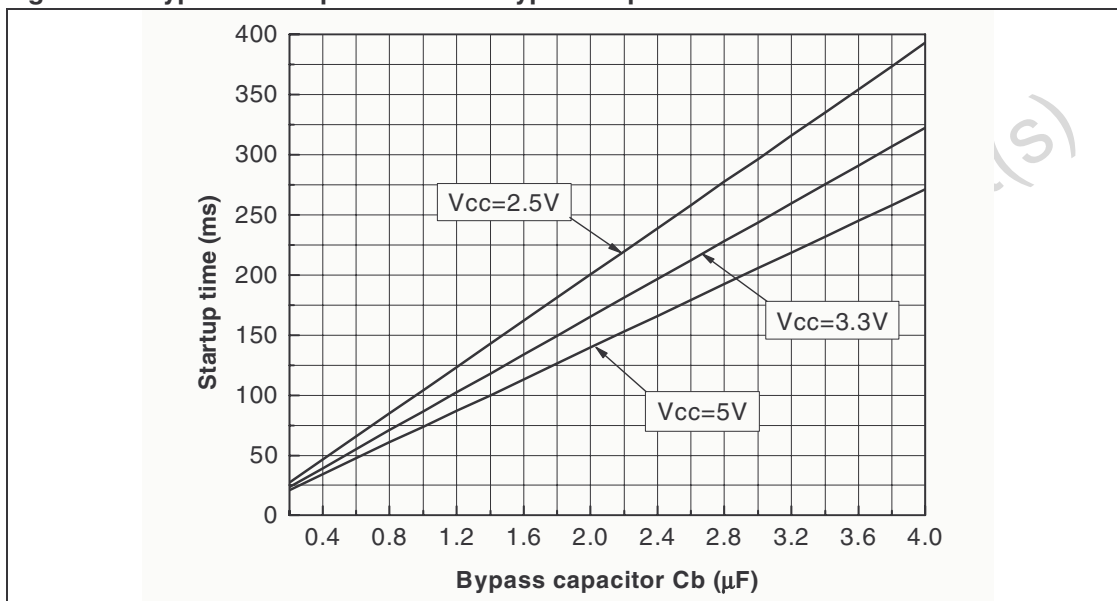
When the TS4975 is controlled to switch from full standby (output mode 0) to another output mode, a delay is necessary to stabilize the DC bias. This length of this delay depends on the  $C_b$  and  $V_{CC}$  values. A typical value can be calculated by following formula:

$$t_{wu} = C_b \times \frac{V_{CC}}{V_{CC} - 1.2} \times 50000 + 0.008(s)$$

This formula assumes that  $C_b$  voltage is equal to 0 V. If the  $C_b$  voltage is not equal 0 V, the startup time will be always lower.

In *Figure 63* you could easily establish typical startup time for given supply voltage and bypass capacitor  $C_b$ .

**Figure 63. Typical startup time versus bypass capacitance**



### 4.9 Pop and click performance

The TS4975 has internal pop and click reduction circuitry which eliminates the output transients, for example during switch-on or switch-off phases, during a switch from an output mode to another or during change in volume. The performance of this circuitry is closely linked to the values of the input capacitor  $C_{in}$ , the output capacitor  $C_{out}$  (for Single-Ended configuration) and the bias voltage bypass capacitor  $C_b$ .

The value of  $C_{in}$  and  $C_{out}$  is determined by the lower cut-off frequency value requested. The value of  $C_b$  will affect the THD+N and PSRR values in lower frequencies.

The TS4975 is optimized to have a low pop and click in the typical schematic configuration (see *Figure 1 on page 3* and *Figure 2 on page 4*).

During the device start-up period when the pop and click reduction is active, the value \$F<sub>xh</sub> (1111xxxx binary) can be read from the internal device registry.

Once the device is fully operational and the pop and click is inactive, the last value of control register can be read.

### 4.10 Thermo shutdown

The TS4975 device has internal protection in case of over temperature by thermal shutdown. Thermal shutdown is active when the device reaches temperature 150°C.

When thermo shutdown protection is active, value \$F<sub>xh</sub> (1111xxxx binary) can be read from the internal device registry.

When thermo shutdown protection state disappears, the last value of control register can be read.

### 4.11 Demoboard

A demoboard for the TS4975 is available.

For more information about this demoboard, please refer to **Application Note AN2151**, which can be found on [www.st.com](http://www.st.com).

Figure 67 on page 33 shows the schematic of the demoboard. Figure 64, Figure 65 and Figure 66, show bottom layer, top layer and the component locations, respectively.

Figure 64. Bottom layer

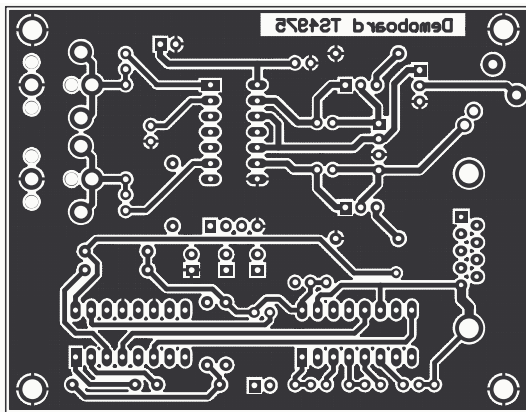


Figure 65. Top layer

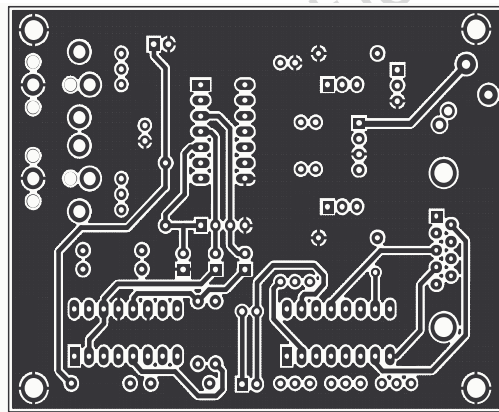


Figure 66. Component location

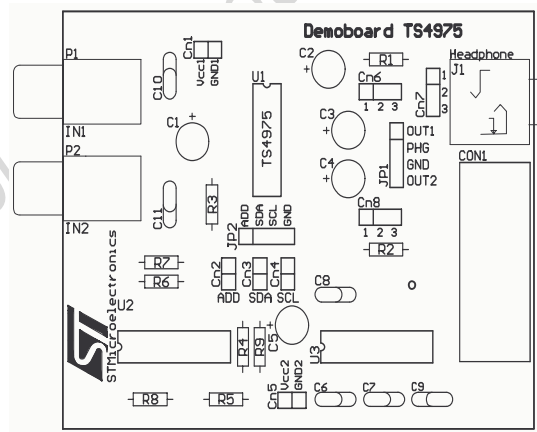
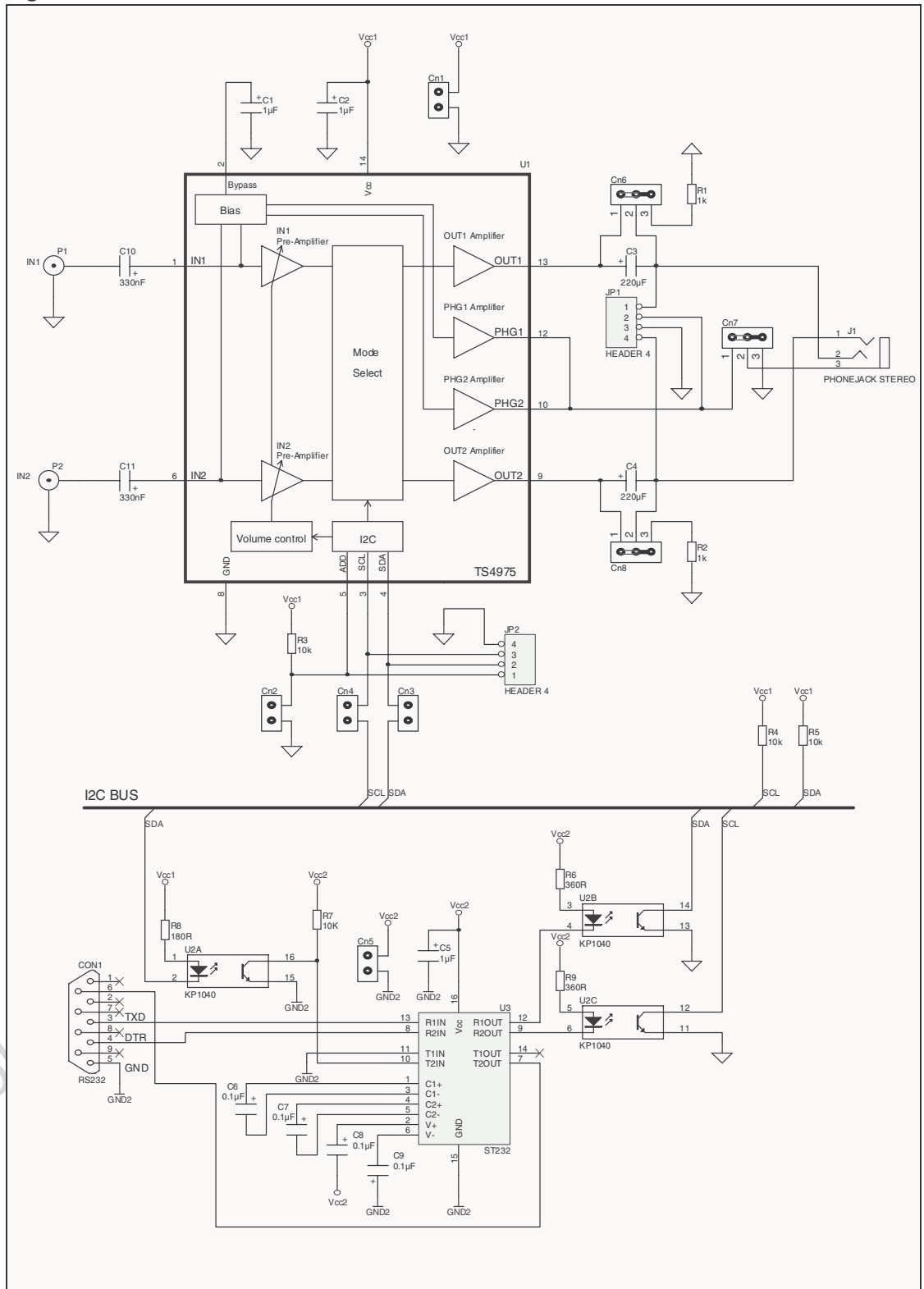




Figure 67. Demoboard schematic



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## 5 Package Mechanical Data

Figure 68. TS4975 footprint recommendation

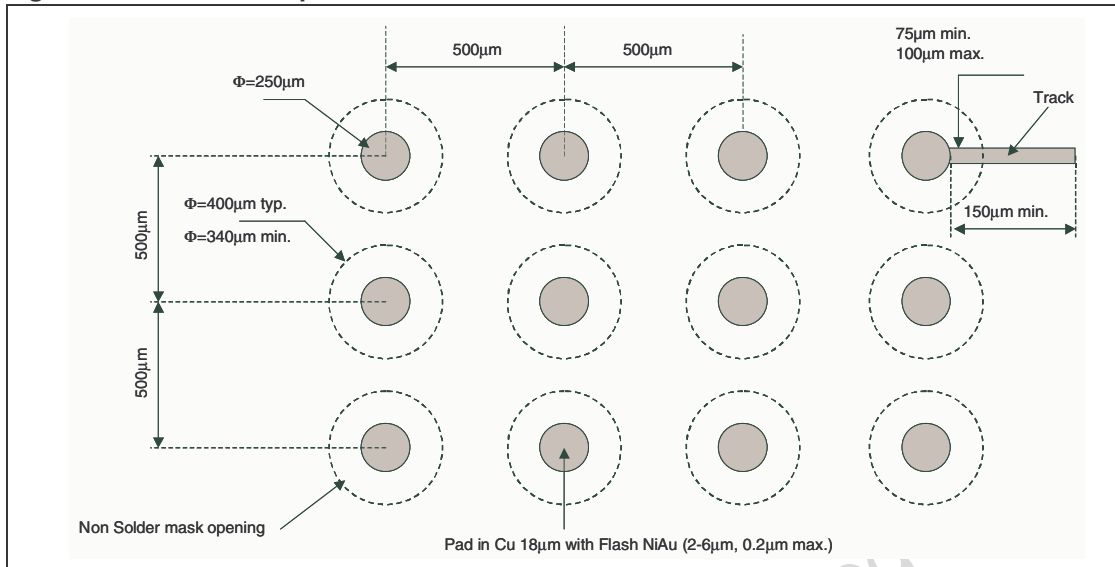


Figure 69. Pin out (top view)

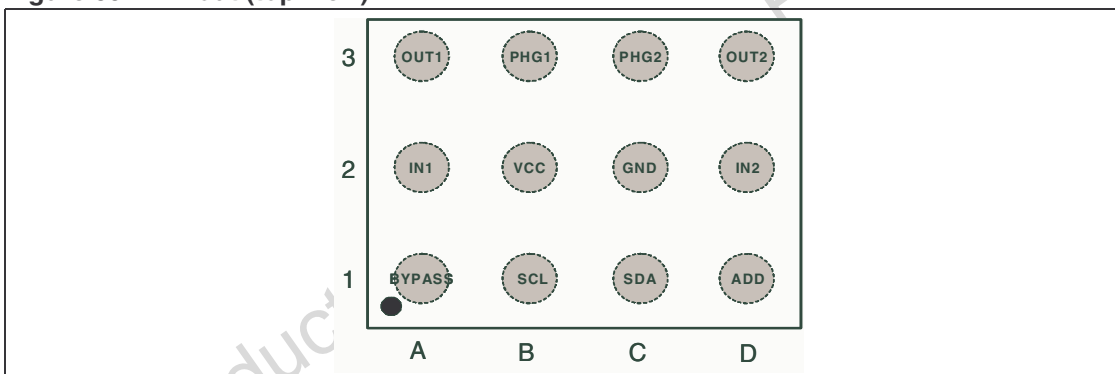


Figure 70. Marking (top view)

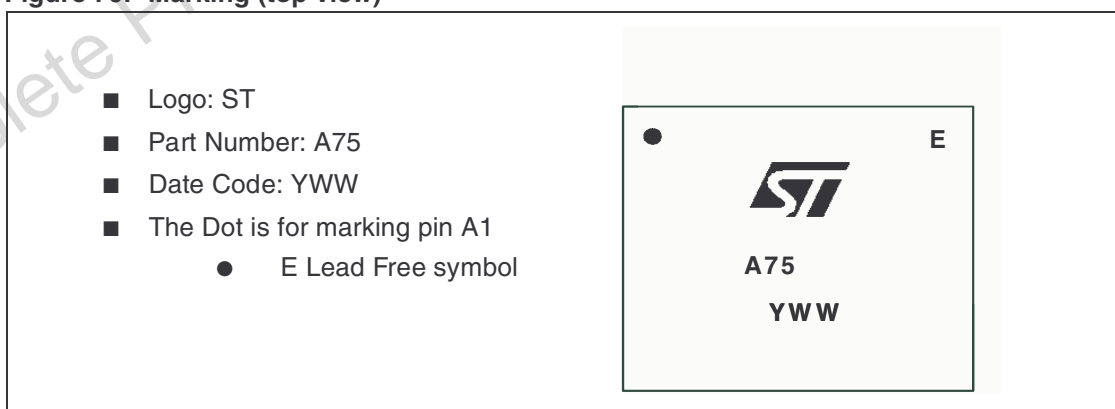


Figure 71. Flip-chip - 12 bumps

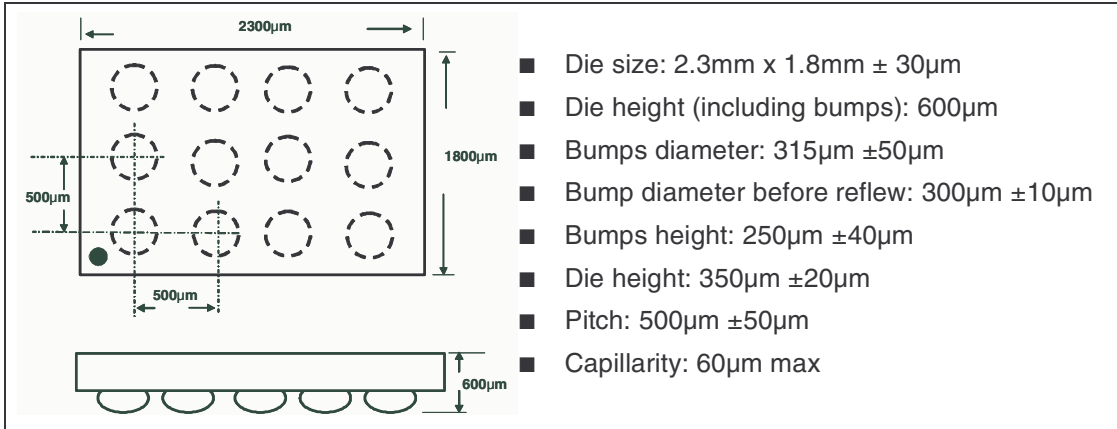
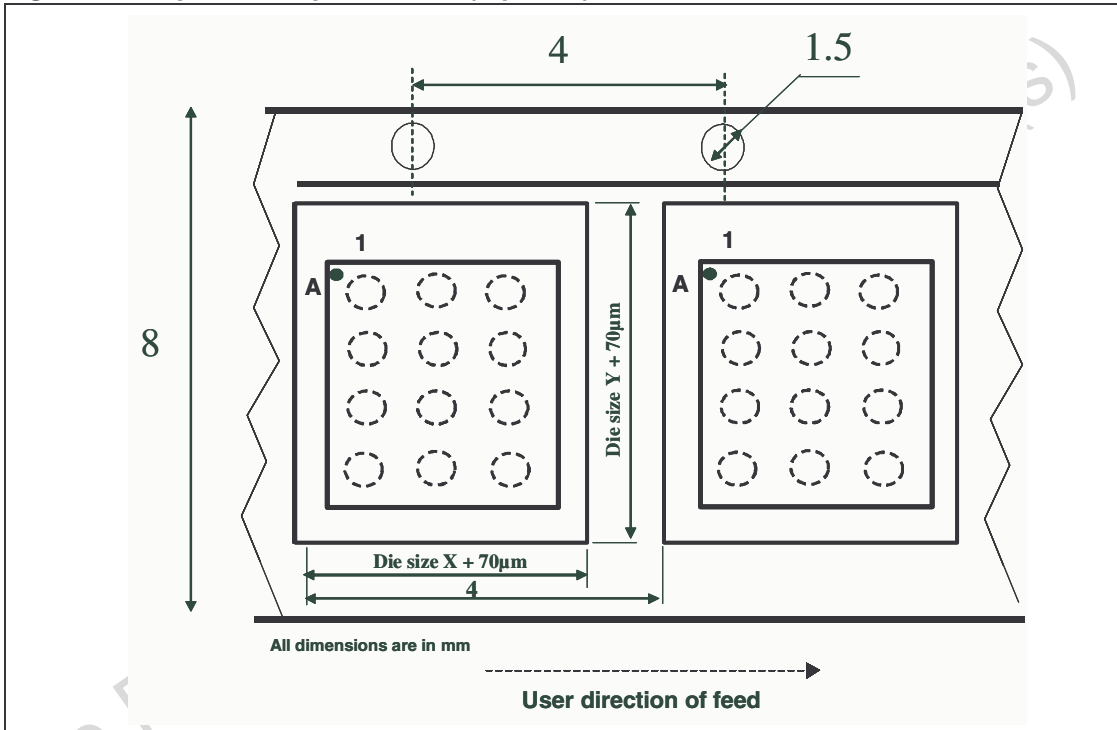


Figure 72. Tape & reel specification (top view)



Obsolete

## 6 Revision History

Date	Revision	Changes
Nov. 2004	1	Initial release.
July 2005	2	Product in full production
Nov. 2005	3	The following changes were made in this revision: <ul style="list-style-type: none"><li>- Application notes updated</li><li>- Formatting changes throughout</li></ul>

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