



## Radiation Hardened P-Channel MOSFET

**Qualified per MIL-PRF-19500/630**

*Qualified Levels:*  
**JANSR and JANSF**

### DESCRIPTION

Microsemi's first generation Rad- Hard MOSFET's are designed for Space and Military applications. The devices have been characterized for Total Dose (TID) and Single Event environments (SEE). These products may be used for satellite Power Supplies, Motor Controls and any miscellaneous power applications needed for Space. Microsemi's Rad- hard MOSFET's are qualified to MIL-PRF- 19500 slash sheet specifications. The 2N7389 is qualified to meet Slash Sheet /630 of MIL-PRF-19500.

**Important:** For the latest information, visit our website <http://www.microsemi.com>.

### FEATURES

- JEDEC registered 2N7389 number
- Hermetically sealed package
- Internal metallurgical bonds
- RHA level JANS qualifications available per MIL-PRF-19500/630.  
(See [part nomenclature](#) for all available options.)
- RoHS compliant

### APPLICATIONS / BENEFITS

- Low profile surface mount for crowded areas
- Lightweight package
- Military and other high-reliability rad-hard applications

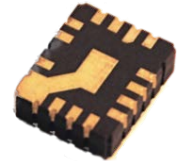
### MAXIMUM RATINGS @ T<sub>C</sub> = +25 °C unless otherwise stated

Parameters / Test Conditions	Symbol	Value	Unit
Operating & Storage Junction Temperature Range	T <sub>J</sub> & T <sub>stg</sub>	-55 to +150	°C
Thermal Resistance Junction-to-Case (see <a href="#">Figure 4</a> )	R <sub>θJC</sub>	5	°C/W
Total Power Dissipation	P <sub>T</sub>	0.8 25	W
		@ T <sub>A</sub> = +25 °C	
		@ T <sub>C</sub> = +25 °C <sup>(1)</sup>	
Gate-Source Voltage, dc	V <sub>GS</sub>	± 20	V
Drain Current, dc @ T <sub>C</sub> = +25 °C <sup>(2)</sup> <sup>(3)</sup>	I <sub>D1</sub>	-6.5	A
Drain Current, dc @ T <sub>C</sub> = +100 °C <sup>(2)</sup> <sup>(3)</sup>	I <sub>D2</sub>	-4.1	A
Off-State Current (Peak Total Value) <sup>(4)</sup>	I <sub>DM</sub>	-26	A
Source Current	I <sub>S</sub>	-6.5	A

- NOTES:**
1. Derated linearly 0.2 W/°C for T<sub>C</sub> > +25 °C
  2. The following formula derives the maximum theoretical I<sub>D</sub> limit. I<sub>D</sub> is limited by package and internal wires and may also be limited by pin diameter

$$I_D = \sqrt{\frac{T_J(\text{max}) - T_C}{R_{\theta JC} \times r_{DS(on)} @ T_J(\text{max})}}$$

3. See [Figure 3](#) for maximum drain current graphs
4. I<sub>DM</sub> = 4 X I<sub>D1</sub> as calculated in note (2)



### U-18 LCC Package

Also available in:

**TO-205AF (TO-39)  
Package**

(leaded top-hat)

 [JANS 2N7389](#)

#### **MSC – Lawrence**

6 Lake Street,  
Lawrence, MA 01841  
Tel: 1-800-446-1158 or  
(978) 620-2600  
Fax: (978) 689-0803

#### **MSC – Ireland**

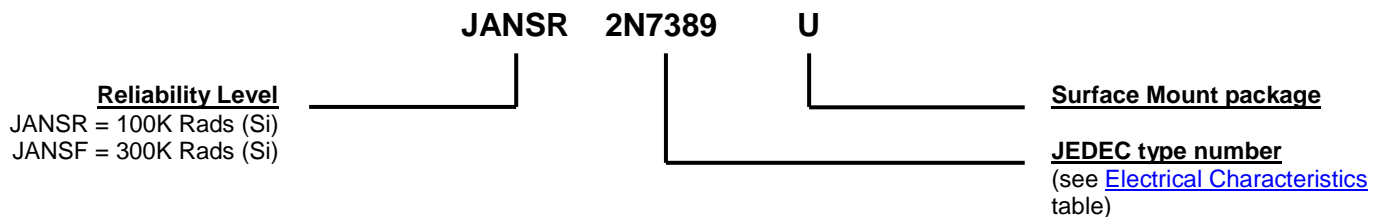
Gort Road Business Park,  
Ennis, Co. Clare, Ireland  
Tel: +353 (0) 65 6840044  
Fax: +353 (0) 65 6822298

**Website:**

[www.microsemi.com](http://www.microsemi.com)

**MECHANICAL and PACKAGING**

- CASE: Ceramic LCC-18 with kovar gold plated lid
- TERMINALS: Gold plating over nickel
- MARKING: Manufacturer's ID, part number, date code, ESD symbol at pin 1 location
- TAPE & REEL option: Standard per EIA-481-D. Consult factory for quantities
- See [Package Dimensions](#) on last page.

**PART NOMENCLATURE**

**SYMBOLS & DEFINITIONS**

Symbol	Definition
di/dt	Rate of change of diode current while in reverse-recovery mode, recorded as maximum value.
$I_D$	Drain Current, dc: The direct current into the drain terminal.
$I_{DSS}$	Zero-Gate-Voltage Drain Current: The direct current into the gate terminal when the gate-source voltage is zero.
$I_F$	Forward Current: The current flowing from the p-type region to the n-type region.
$I_{GSS}$	Reverse-Gate Current, Drain Short-Circuited to Source: The direct current into the gate terminal with a forward gate source voltage applied ( $I_{GSSF}$ ) or reverse gate source voltage applied ( $I_{GSSF}$ ) and the drain terminal short-circuited to the source terminal.
$I_S$	Source Current, dc: The direct current into the source terminal.
$r_{DS(on)}$	Static Drain-Source On-State Resistance: The dc resistance between the drain and source terminals with a specified gate-source voltage applied to bias the device to the on state.
$R_G$	Gate Drive Impedance or Gate Resistance.
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage: Gate short-circuited to the source terminal.
$V_{DD}$	Drain-Supply Voltage, dc: The dc supply voltage applied to a circuit connected to the drain terminal.
$V_{DG}$	Drain-Gate Voltage, dc: The dc voltage between the drain and gate terminals.
$V_{DS}$	Drain-Source Voltage, dc: The dc voltage between the drain terminal and the source terminal.
$V_{DS(on)}$	Drain-Source On-State Voltage: The voltage between the drain and source terminals with a specified forward gate-source voltage supplied to bias the device to the on-state.
$V_{GS}$	Gate-Source Voltage, dc: The dc voltage between the gate terminal and the source terminal.

**ELECTRICAL CHARACTERISTICS @  $T_A = +25^\circ\text{C}$ , unless otherwise noted**

Parameters / Test Conditions	Symbol	Min.	Max.	Unit
<b>PRE-IRRADIATION CHARACTERISTICS</b>				
Drain-Source Breakdown Voltage $V_{GS} = 0\text{ V}, I_D = -1.0\text{ mA}$	$V_{(BR)DSS}$	-100		V
Gate-Source Voltage (Threshold) $V_{DS} \geq V_{GS}, I_D = -1\text{ mA}$ $V_{DS} \geq V_{GS}, I_D = -1\text{ mA}, T_J = +125^\circ\text{C}$ $V_{DS} \geq V_{GS}, I_D = -1\text{ mA}, T_J = -55^\circ\text{C}$	$V_{GS(th)1}$ $V_{GS(th)2}$ $V_{GS(th)3}$	-2.0 -1.0	-4.0 -5.0	V
Gate Current $V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$ $V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}, T_J = +125^\circ\text{C}$	$I_{GSS1}$ $I_{GSS2}$		$\pm 100$ $\pm 200$	nA
Drain Current $V_{GS} = 0\text{ V}, V_{DS} = -80\text{ V}$	$I_{DSS1}$		-25	$\mu\text{A}$
Drain Current $V_{GS} = 0\text{ V}, V_{DS} = -80\text{ V}, T_J = +125^\circ\text{C}$	$I_{DSS2}$		-0.25	mA
Static Drain-Source On-State Resistance $V_{GS} = -12\text{ V}, I_D = -4.1\text{ A pulsed}$	$r_{DS(on)1}$		0.30	$\Omega$
Static Drain-Source On-State Resistance $V_{GS} = -12\text{ V}, I_D = -6.5\text{ A pulsed}$	$r_{DS(on)2}$		0.35	$\Omega$
Static Drain-Source On-State Resistance $T_J = +125^\circ\text{C}$ $V_{GS} = -12\text{ V}, I_D = -4.1\text{ A pulsed}$	$r_{DS(on)3}$		0.54	$\Omega$
Diode Forward Voltage $V_{GS} = 0\text{ V}, I_D = -6.5\text{ A pulsed}$	$V_{SD}$		-3.0	V

**DYNAMIC CHARACTERISTICS**

Parameters / Test Conditions	Symbol	Min.	Max.	Unit
Gate Charge:				
On-State Gate Charge $V_{GS} = -12\text{ V}, I_D = -6.5\text{ A}, V_{DS} = -50\text{ V}$	$Q_{g(on)}$		45	nC
Gate to Source Charge $V_{GS} = -12\text{ V}, I_D = -6.5\text{ A}, V_{DS} = -50\text{ V}$	$Q_{gs}$		10	nC
Gate to Drain Charge $V_{GS} = -12\text{ V}, I_D = -6.5\text{ A}, V_{DS} = -50\text{ V}$	$Q_{gd}$		25	nC

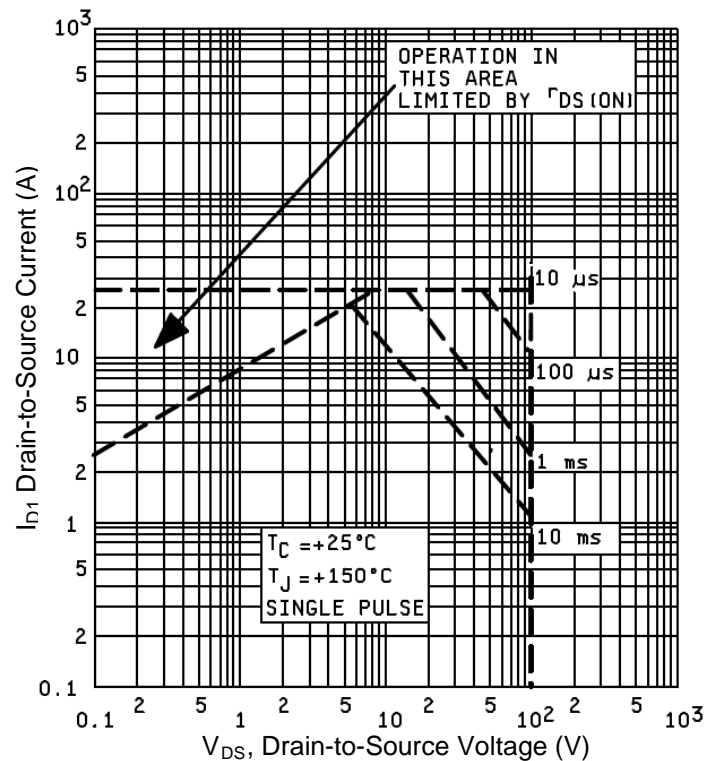
**SWITCHING CHARACTERISTICS**

Parameters / Test Conditions	Symbol	Min.	Max.	Unit
Turn-on delay time $I_D = -6.5\text{ A}, V_{GS} = -12\text{ V}, R_G = 7.5\ \Omega, V_{DD} = -50\text{ V}$	$t_{d(on)}$		30	ns
Rise time $I_D = -6.5\text{ A}, V_{GS} = -12\text{ V}, R_G = 7.5\ \Omega, V_{DD} = -50\text{ V}$	$t_r$		50	ns
Turn-off delay time $I_D = -6.5\text{ A}, V_{GS} = -12\text{ V}, R_G = 7.5\ \Omega, V_{DD} = -50\text{ V}$	$t_{d(off)}$		70	ns
Fall time $I_D = -6.5\text{ A}, V_{GS} = -12\text{ V}, R_G = 7.5\ \Omega, V_{DD} = -50\text{ V}$	$t_f$		70	ns
Diode Reverse Recovery Time $di/dt \leq -100\text{ A}/\mu\text{s}, V_{DD} \leq -50\text{ V}, I_F = -6.5\text{ A}$	$t_{rr}$		250	ns

**ELECTRICAL CHARACTERISTICS @  $T_A = +25^\circ\text{C}$ , unless otherwise noted (continued)**
**POST-IRRADIATION <sup>(1)</sup>**

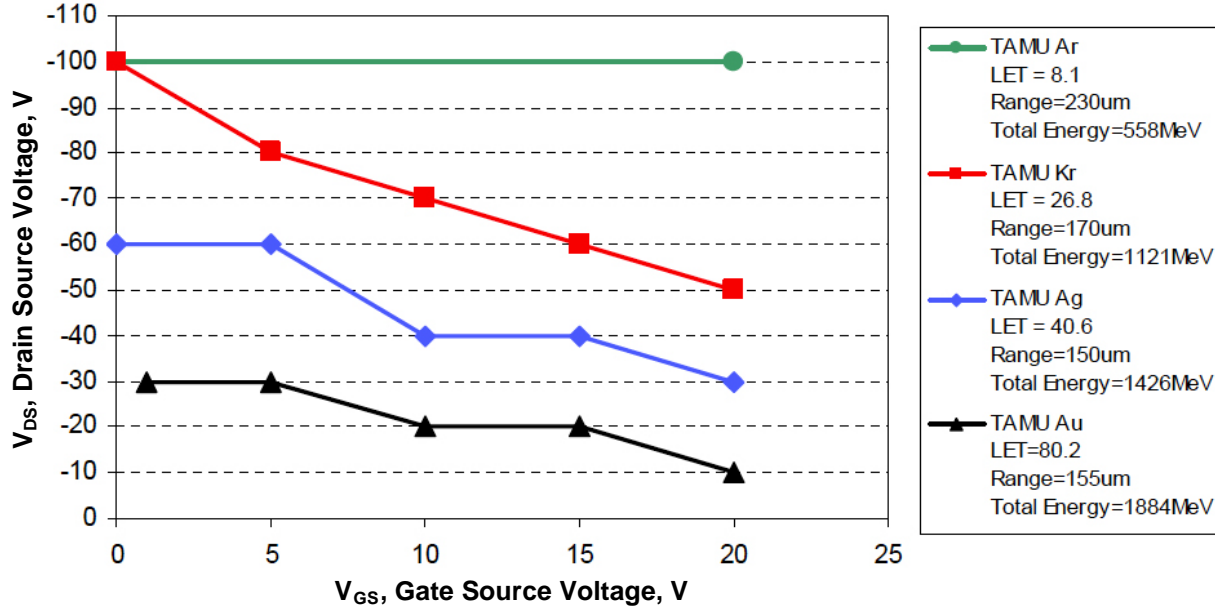
Parameters / Test Conditions	Symbol	Min.	Max.	Unit
Drain-Source Breakdown Voltage $V_{GS} = 0\text{ V}, I_D = -1\text{ mA}$	$V_{(BR)DSS}$	-100		V
Gate-Source Voltage (Threshold) $V_{DS} \geq V_{GS}, I_D = -1.0\text{ mA}$ JANSR $V_{DS} \geq V_{GS}, I_D = -1.0\text{ mA}$ JANSF	$V_{GS(th)1}$ $V_{GS(th)1}$	-2.0 -2.0	-4.0 -5.0	V
Gate Current $V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	$I_{GSS1}$		$\pm 100$	nA
Drain Current $V_{GS} = 0\text{ V}, V_{DS} = -80\text{ V}$ of $V_{DS}$ (pre-irradiated)	$I_{DSS1}$		-25	$\mu\text{A}$
Static Drain-Source On-State Voltage $V_{GS} = -12\text{ V}, I_D = -4.1\text{ pulsed}$	$r_{DS(on)}$		1.23	V
Diode Forward Voltage $V_{GS} = 0\text{ V}, I_D = -6.5\text{ pulsed}$	$V_{SD}$		-3.0	V

**NOTE:** 1. Post-irradiation electrical characteristics apply to devices subjected to steady state total dose irradiation testing in accordance with MIL-STD-750, method 1019. Separate samples are tested for  $V_{GS}$  bias (12V), and  $V_{DS}$  bias (80V) conditions.

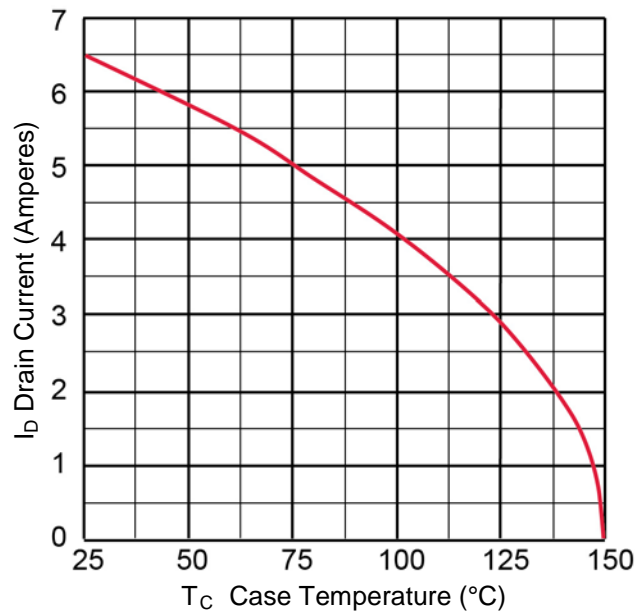
**SAFE OPERATING AREA**

**FIGURE 1**

**GRAPHS**
**SEE (Single Event Effect) Typical Response:**

Heavy Ion testing of the 2N7389U device has been characterized at the Texas A&M cyclotron. The following SEE curve has been established using the elements, LET, range, and Total Energy conditions as shown:

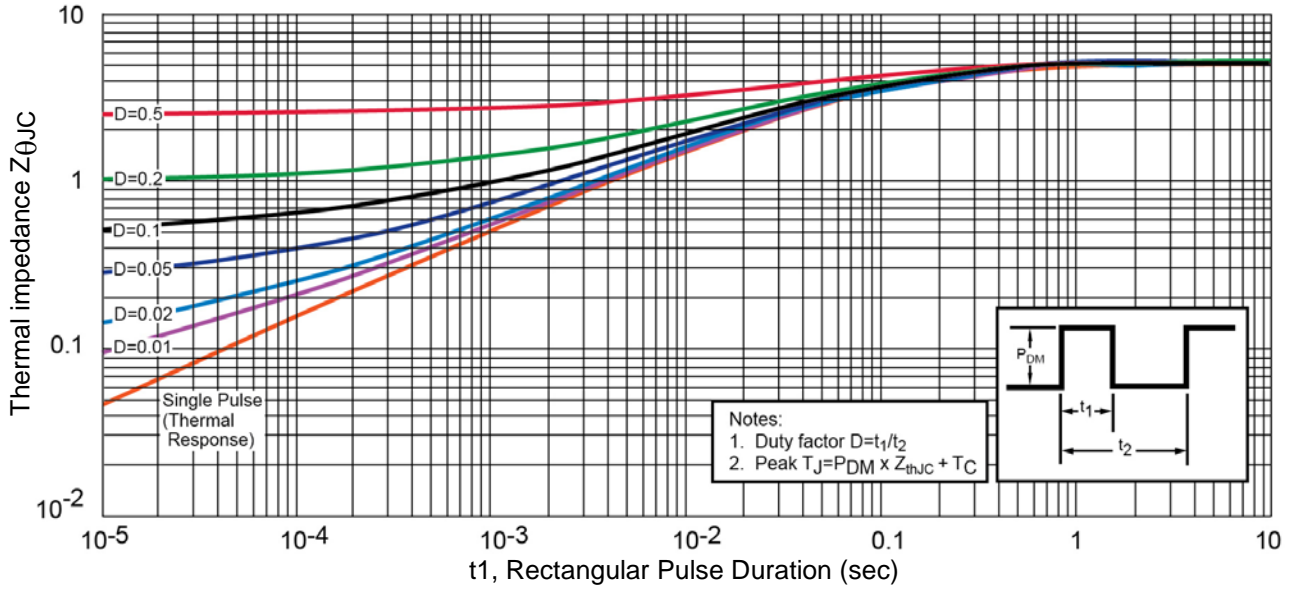
**FIGURE 2**


It should be noted that total energy levels are considered to be a factor in SEE characterization. Comparisons to other datasets should not be based on LET alone. Please consult factory for more information.


**FIGURE 3**

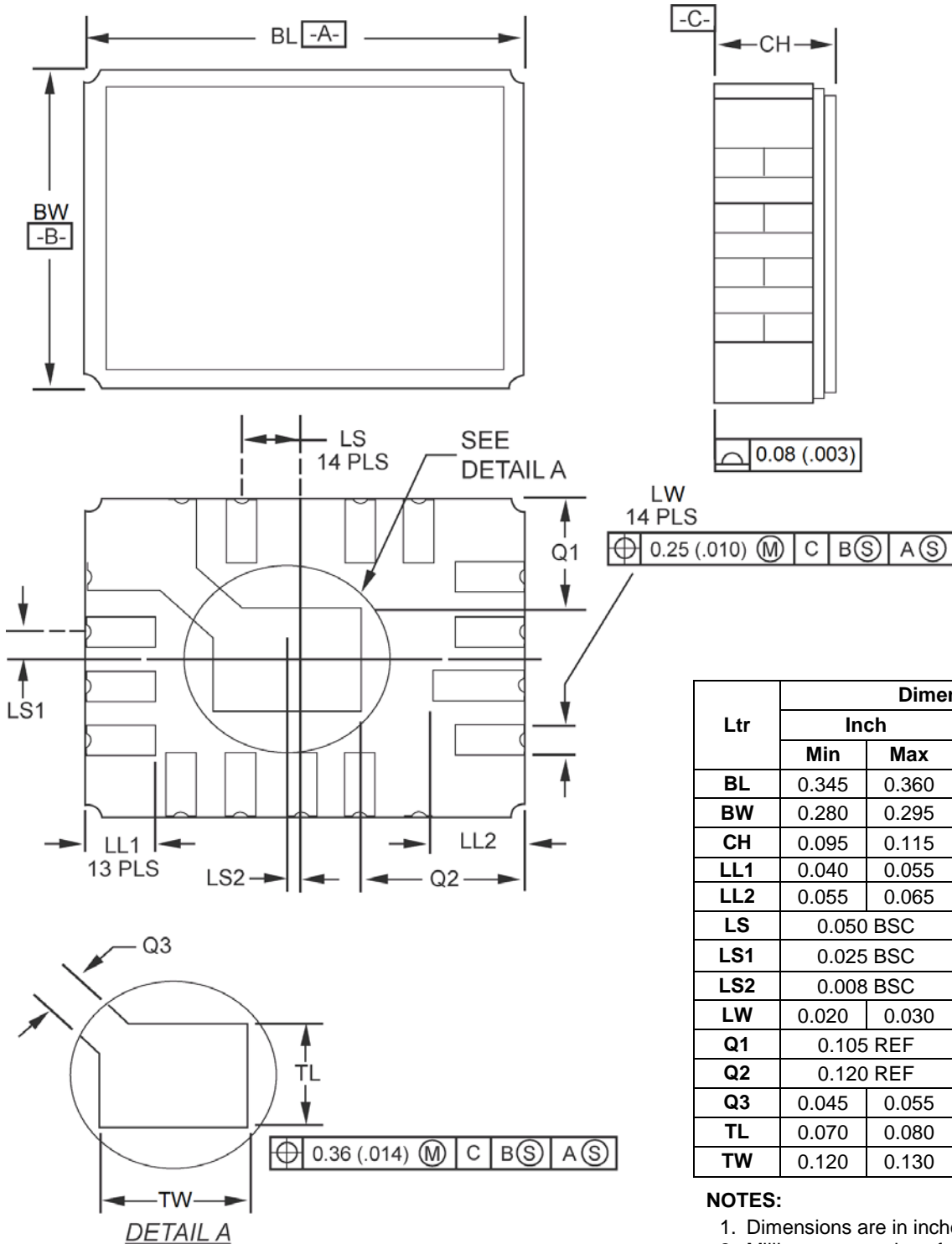
Maximum Drain Current vs Case Temperature

GRAPHS (continued)



**FIGURE 4**  
 Thermal Impedance Curves

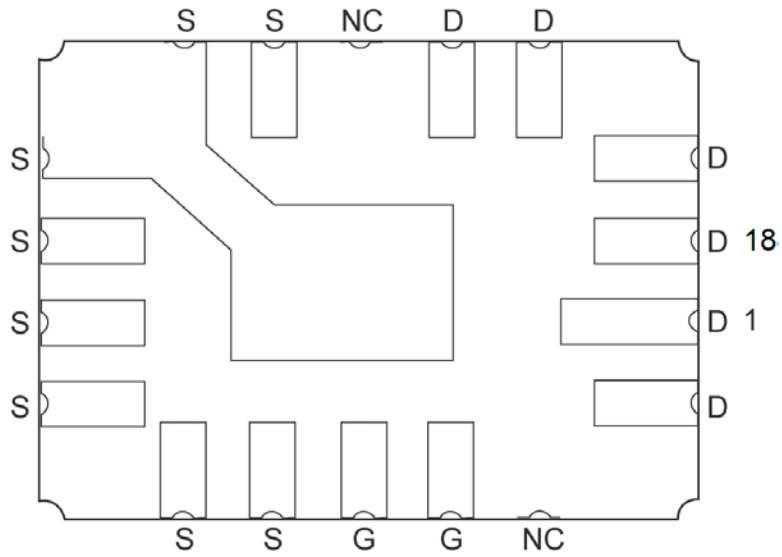
PACKAGE DIMENSIONS



NOTES:

1. Dimensions are in inches.
2. Millimeters are given for information only.
3. In accordance with ASME Y14.5M, diameters are equivalent to  $\Phi$  symbology.

**PAD LAYOUT**



**PAD ASSIGNMENTS**

**SCHEMATIC**

