

## Dual High-Speed CAN Transceiver with Standby Mode

### Features

- Fully ISO 11898-2, ISO 11898-5, ISO 11898-2: 2016 and SAE J2962-2 Compliant
- CAN FD Ready
- Communication Speed up to 5 Mbps
- Low Electromagnetic Emission (EME) and High Electromagnetic Immunity (EMI)
- Differential Receiver with Wide Common-Mode Range
- Remote Wake-up Capability via CAN Bus – Wake-up on Pattern (WUP) as Specified in ISO 11898-2: 2016, 3.8  $\mu$ s Activity Filter Time
- Functional Behavior Predictable Under All Supply Conditions
- Transceiver Disengages from the Bus when Not Powered Up
- RXD Recessive Clamping Detection
- High Electrostatic Discharge (ESD) Handling Capability on the Bus Pins
- Bus Pins Protected Against Transients in Automotive Environments
- Transmit Data (TXD) Dominant Time-out Function
- Undervoltage Detection on VCC Pin
- Bus Pins Short-Circuit and Overtemperature Protected
- Fulfills the OEM “*Hardware Requirements for LIN, CAN and FlexRay™ Interfaces in Automotive Applications*”, Rev. 1.3
- Qualified According to AEC-Q100
- Two Ambient Temperature Grades Available:
  - ATA6565-GCQW1 and ATA6565-GNQW1 up to  $T_{amb} = +125^{\circ}C$
  - ATA6565-GCQW0 and ATA6565-GNQW0 up to  $T_{amb} = +150^{\circ}C$
- 14-Lead SOIC Package and 14-Lead VDFN Package with Wettable Flanks (Moisture Sensitivity Level 1)

### Applications

Classical CAN and CAN FD networks in Automotive, Industrial, Aerospace, Medical and Consumer applications.

### General Description

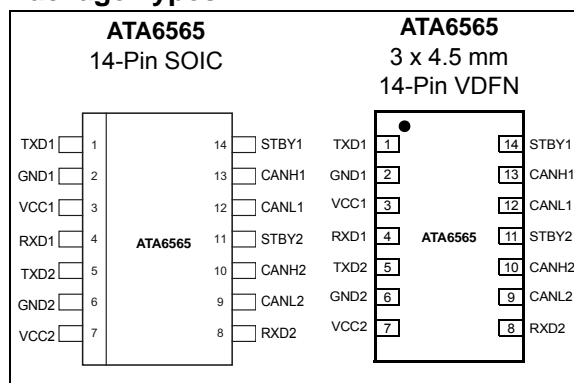
The ATA6565 is a fully integrated, dual high-speed CAN transceiver with two completely independent and separated high-speed CAN transceivers integrated in one package (only the GND pins, GND1 and GND2, are internally connected). Each of the two identical transceivers provides an interface between a Controller Area Network (CAN) protocol controller and a physical two-wire CAN bus.

The device is designed for high-speed (up to 5 Mbps) CAN applications in the automotive industry, providing differential transmit and receive capability to (a microcontroller with) a CAN protocol controller. It offers improved Electromagnetic Compatibility (EMC) and Electrostatic Discharge (ESD) performance, as well as features such as:

- Ideal passive behavior to the CAN bus when the supply voltage is off
- Very low current consumption in Standby mode with bus wake-up capability

Two operating modes, together with the dedicated fail-safe features, make the ATA6565 an excellent choice for all types of high-speed CAN networks. The ATA6565 includes more than one high-speed CAN interface which requires a Low-Power mode with wake-up capability via the CAN bus. These features are especially valuable for body control units and gateways.

### Package Types



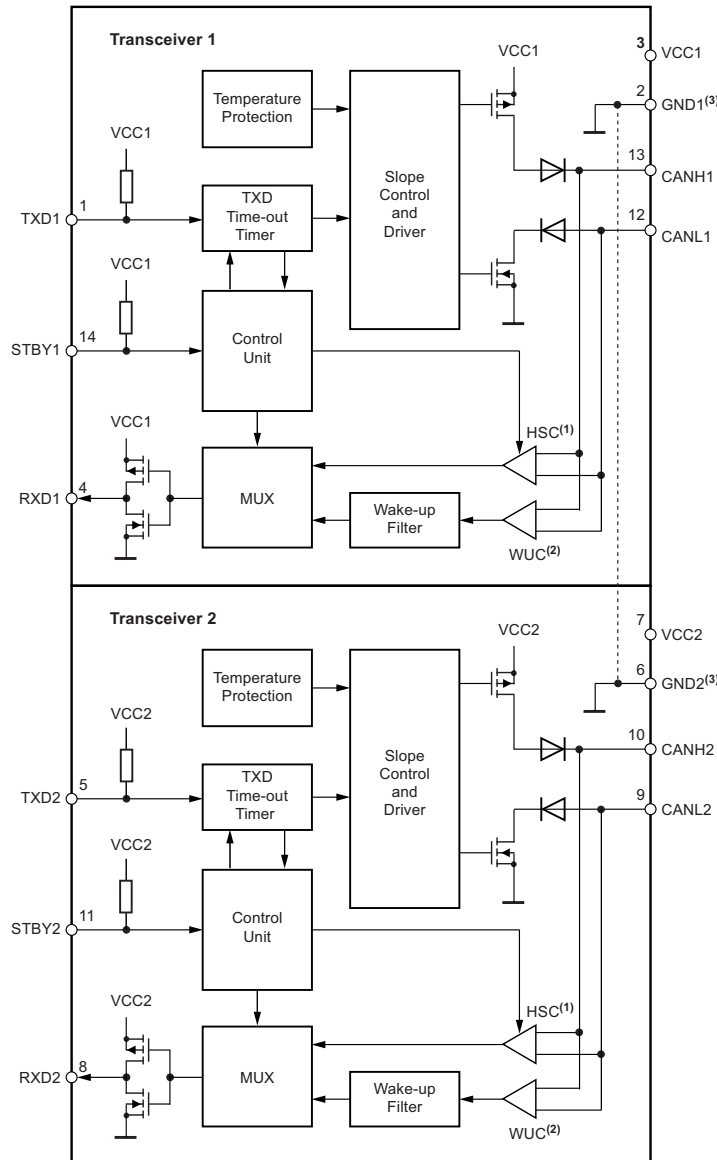
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## ATA6565 Family Members

Device	Grade 0	Grade 1	SOIC14	VDFN14
ATA6565-GNQW1		X	X	
ATA6565-GNQW0	X		X	
ATA6565-GCQW1		X		X
ATA6565-GCQW0	X			X

**Note:** For ordering information, see the “[Product Identification System](#)” section.

## Block Diagram



## 1.0 FUNCTIONAL DESCRIPTION

The ATA6565 is a stand-alone, dual high-speed CAN transceiver, compliant with the ISO 11898-2, ISO 11898-5, ISO 11898-2: 2016 and SAE J2962-2 standards. Each of the two transceivers provides a very low current consumption in Standby mode and wake-up capability via the CAN bus.

The functions described in the following text apply to each of the two identical high-speed CAN transceivers integrated in the ATA6565. Therefore, if for example, the CANH pin is stated, this applies to each of the two transceivers, meaning CANH1 and CANH2. The two transceivers are identical and there is no internal

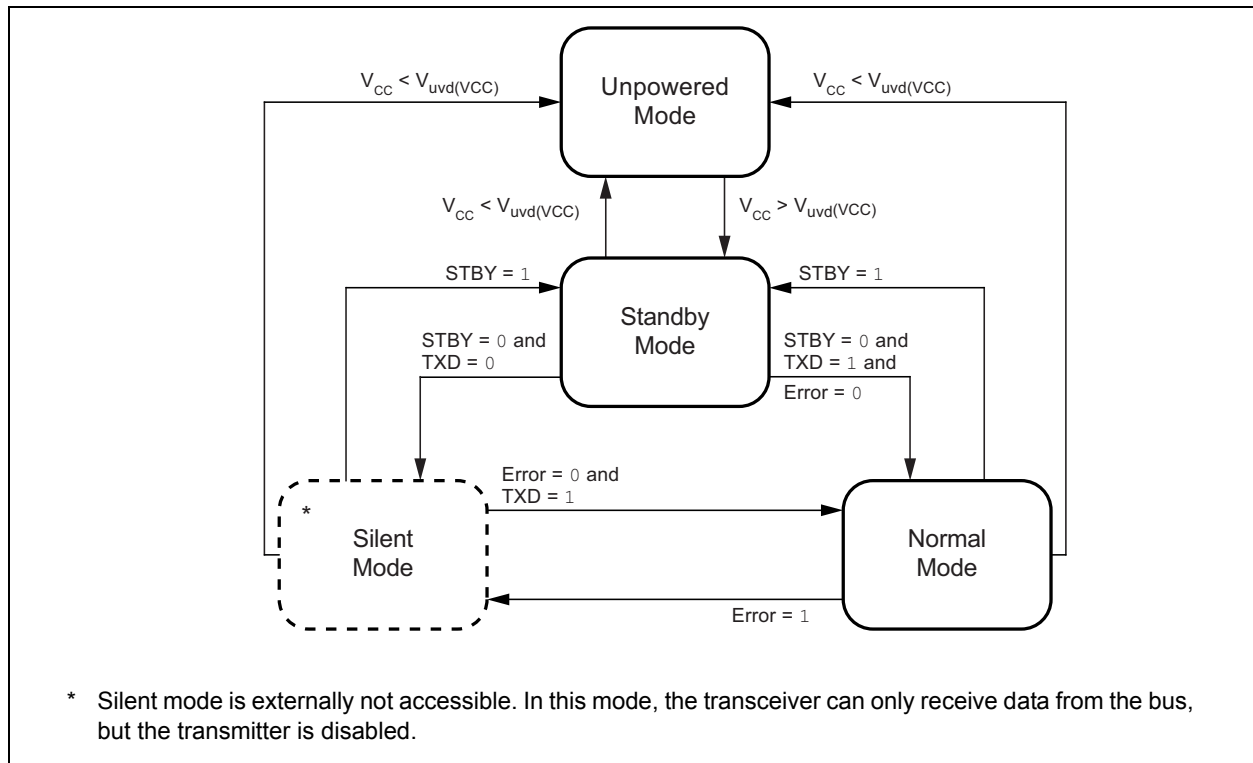
connection between them (with the exception of the GND pins, GND1 and GND2), so they work completely independently.

## 1.1 Operating Modes

Each of the transceivers supports three operating modes: Unpowered, Standby and Normal. Additionally, there is the internal Silent mode, which is not externally accessible. This mode is a Receive Only mode, which means the CAN drivers are deactivated and only data from the bus can be received.

The operating modes can be selected via the STBY pins (STBY1 and STBY2). See [Figure 1-1](#) and [Table 1-1](#) for a description of the operating modes.

**FIGURE 1-1: OPERATING MODES**



**TABLE 1-1: OPERATING MODES**

Mode	Inputs		Outputs	
	STBY	Pin TXD	CAN Driver	Pin RXD
Unpowered	X <sup>(1)</sup>	X <sup>(1)</sup>	Recessive	Recessive
Standby	High	X <sup>(1)</sup>	Recessive	Active <sup>(2)</sup>
Normal	Low	Low	Dominant	Low
	Low	High	Recessive	High

**Note 1:** Irrelevant.

**2:** Reflects the bus only for wake-up.

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## 1.1.1 NORMAL MODE

A low level on the STBY pin, together with a high level on the TXD pin, selects the Normal mode. In this mode, the transceiver is able to transmit and receive data via the CANH and CANL bus lines (see the [Block Diagram](#)). The output driver stage is active and drives data from the TXD input to the CAN bus. The High-Speed Comparator (HSC) converts the analog data on the bus lines into digital data, which is output to pin RXD. The bus biasing is set to  $V_{VCC}/2$  and the undervoltage monitoring of  $V_{VCC}$  is active.

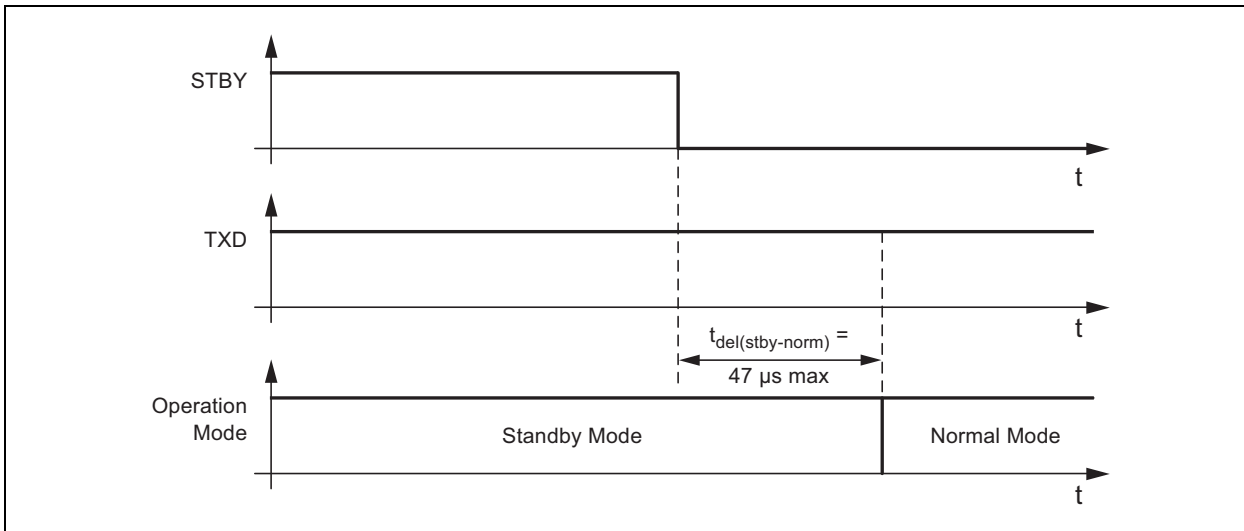
The slope of the output signals on the bus lines is controlled and optimized in a way that ensures the lowest possible Electromagnetic Emission (EME).

To switch the device to Normal Operating mode, set the STBY pin to low and the TXD pin to high (see [Table 1-1](#) and [Figure 1-2](#)). The STBY pin provides a pull-up resistor to VCC, thus ensuring a defined level if the pin is open.

Please note that the device cannot enter Normal mode as long as TXD is at ground level.

The switching into Normal mode is depicted in [Figure 1-2](#).

**FIGURE 1-2: SWITCHING FROM STANDBY MODE TO NORMAL MODE**



### 1.1.2 STANDBY MODE

A high level on the STBY pin selects Standby mode. In this mode, the transceiver is not able to transmit or correctly receive data via the bus lines. The transmitter and the High-Speed Comparator (HSC) are switched off to reduce current consumption.

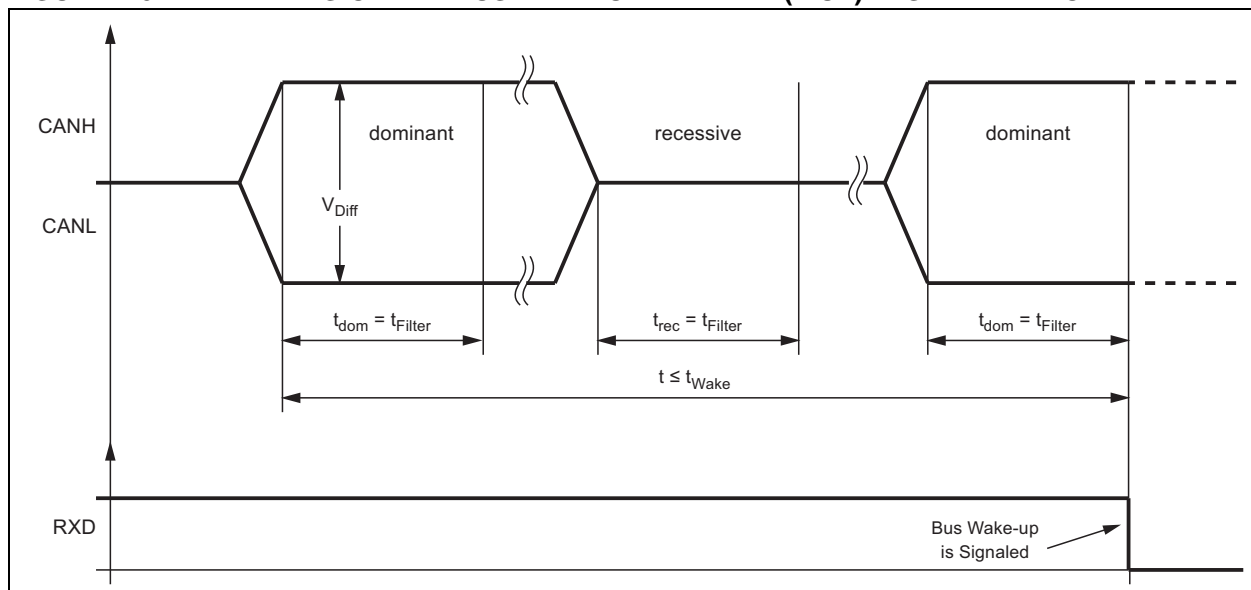
#### 1.1.2.1 Remote Wake-up via the CAN Bus

In Standby mode, the bus lines are biased to ground to reduce current consumption to a minimum. The device monitors the bus lines for a valid wake-up pattern, as specified in the ISO 11898-2: 2016. This filtering helps to avoid spurious wake-up events which would be triggered by scenarios, such as a dominant clamped bus or by a dominant phase due to noise, spikes on the bus, automotive transients or EMI.

The wake-up pattern consists of at least two consecutive dominant bus levels for a duration of at least  $t_{Filter}$ , each separated by a recessive bus level with a duration of at least  $t_{Filter}$ . Dominant or recessive bus levels shorter than  $t_{Filter}$  are always ignored. The complete dominant-recessive-dominant pattern, as shown in Figure 1-3, must be received within the bus wake-up time-out time,  $t_{Wake}$ , to be recognized as a valid wake-up pattern. Otherwise, the internal wake-up logic is reset and then the complete wake-up pattern must be retransmitted to trigger a wake-up event. The RXD pin remains at a high level until a valid wake-up event has been detected.

During Normal mode, at a VCC undervoltage condition or when the complete wake-up pattern is not received within  $t_{Wake}$ , no wake-up is signaled at the RXD pin.

**FIGURE 1-3: TIMING OF THE BUS WAKE-UP PATTERN (WUP) IN STANDBY MODE**



When a valid CAN wake-up pattern is detected on the bus, the RXD pin switches to low to signal a wake-up request. A transition to Normal mode is not triggered until the STBY pin is forced back to low by the microcontroller.

## 1.2 Fail-Safe Features

### 1.2.1 TXD DOMINANT TIME-OUT FUNCTION

A TXD dominant time-out timer is started when the TXD pin is set to low. If the low state on the TXD pin persists for longer than  $t_{to(dom)TXD}$ , the transmitter is disabled, releasing the bus lines to the recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when the TXD pin

is set to high. If the low state on the TXD pin was longer than  $t_{to(dom)TXD}$ , then the TXD pin has to be set to high  $\geq 4 \mu s$  in order to reset the TXD dominant time-out timer.

### 1.2.2 INTERNAL PULL-UP STRUCTURE AT THE TXD AND STBY INPUT PINS

The TXD and STBY pins have an internal pull-up to VCC. This ensures a safe, defined state in case one or both pins are left floating. Pull-up currents flow in these pins in all states, meaning all pins should be in a high state during Standby mode to minimize the current consumption.

### 1.2.3 UNDERVOLTAGE DETECTION ON PIN VCC

If  $V_{VCC}$  drops below its undervoltage detection level,  $V_{Uvd(VCC)}$  (see Section 2.0 "Electrical Characteristics"), the transceiver switches off and disengages from the bus until  $V_{VCC}$  has recovered. The low-power

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wake-up comparator is only switched off during a VCC undervoltage. The logic state of the STBY pin is ignored until the VCC voltage has recovered.

## 1.2.4 BUS WAKE-UP ONLY AT DEDICATED WAKE-UP PATTERN

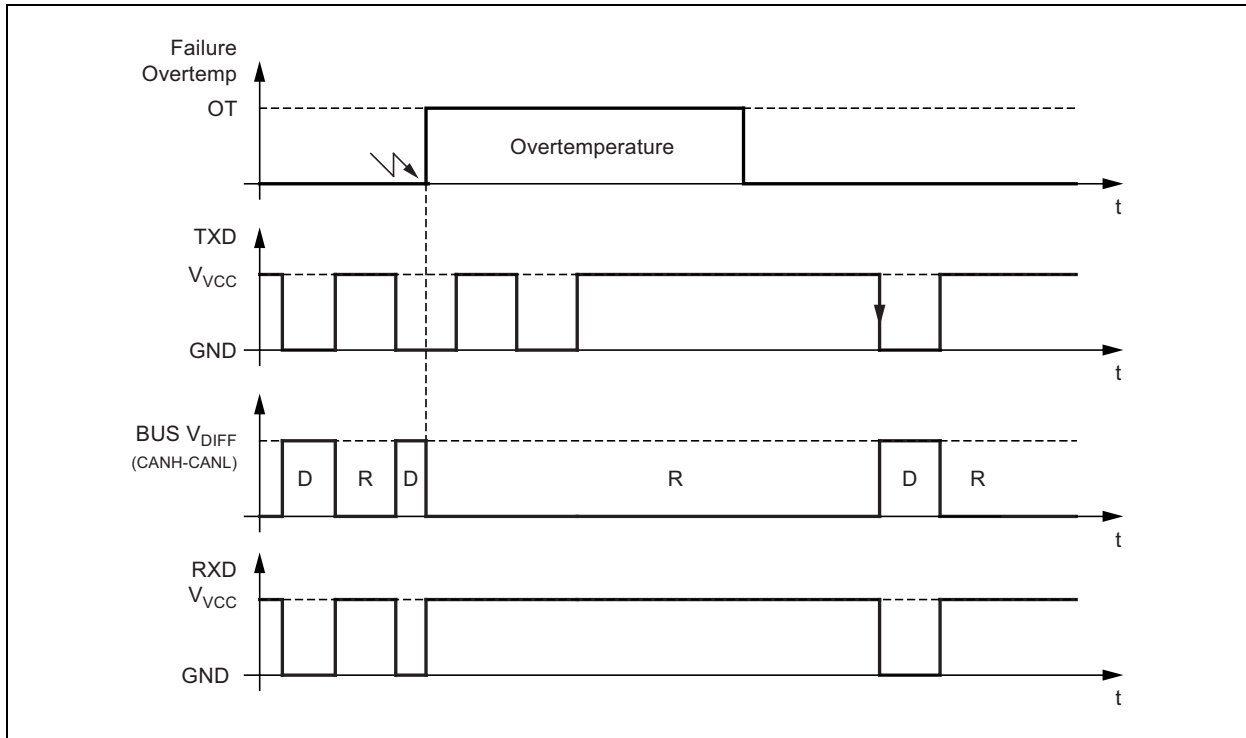
Due to the implementation of the wake-up filtering, the transceiver does not wake-up when the bus is in a long dominant phase; it only wakes up at a dedicated wake-up pattern, as specified in the ISO 11898-2: 2016. This means for a valid wake-up, at least two consecutive dominant bus levels for a duration of at least,  $t_{Filter}$ , each separated by a recessive bus level with a duration of at least,  $t_{Filter}$ , must be received via the bus. Dominant or recessive bus levels shorter than  $t_{Filter}$  are always ignored. The complete dominant-recessive-dominant

pattern, as shown in [Figure 1-3](#), must be received within the bus wake-up time-out time,  $t_{Wake}$ , to be recognized as a valid wake-up pattern. This filtering leads to a higher robustness against EMI and transients, and therefore, significantly reduces the risk of an unwanted bus wake-up.

## 1.2.5 OVERTEMPERATURE PROTECTION

The output drivers are protected against overtemperature conditions. If the junction temperature exceeds the shut-down junction temperature,  $T_{Jsd}$ , the output drivers are disabled until the junction temperature drops below  $T_{Jsd}$  and pin TXD is at a high level again. This TXD condition ensures that output driver oscillations, due to temperature drift, are avoided.

**FIGURE 1-4: RELEASE OF TRANSMISSION AFTER OVERTEMPERATURE CONDITION**



## 1.2.6 SHORT-CIRCUIT PROTECTION OF THE BUS PINS

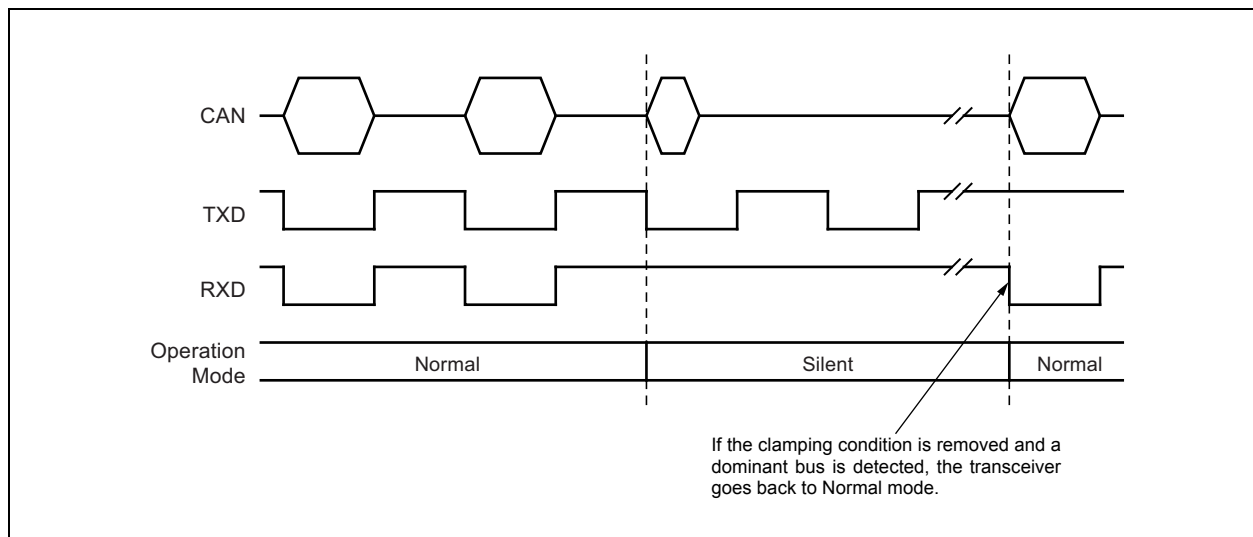
The CANH and CANL bus outputs are short-circuit protected, either against GND or a positive supply voltage. A current-limiting circuit protects the transceiver against damage. If the device is heating up due to a continuous short on CANH or CANL, the internal overtemperature protection switches the bus transmitter off.

## 1.2.7 RXD RECESSIVE CLAMPING

This fail-safe feature prevents the controller from sending data on the bus if its RXD is clamped to high (e.g., recessive). That is, if the RXD pin cannot signalize a dominant

bus condition (e.g., because it is shorted to VCC), the transmitter is disabled to avoid possible data collisions on the bus. In Normal mode, the device permanently compares the state of the High-Speed Comparator (HSC) with the state of the RXD pin. If the HSC indicates a dominant bus state for more than  $t_{RC\_det}$ , without the RXD pin doing the same, a recessive clamping situation is detected and the transceiver is forced into Silent mode. This Fail-Safe mode is released by either entering Standby or Unpowered mode, or if the RXD pin is showing a dominant (e.g., low) level again.

**FIGURE 1-5: RXD RECESSIVE CLAMPING DETECTION**



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## 1.3 Pin Description

The descriptions of the pins are listed in [Table 1-2](#).

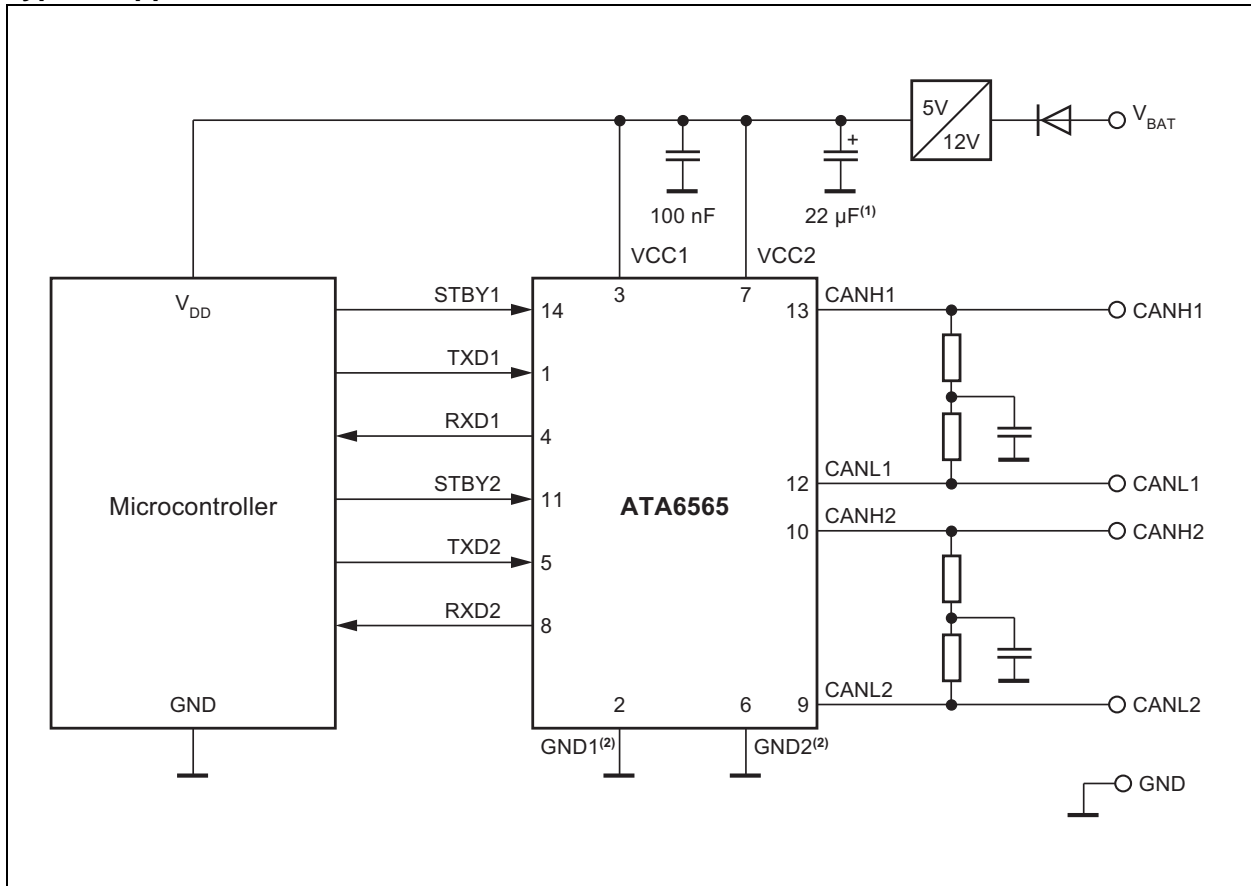
**TABLE 1-2: PIN FUNCTION TABLE**

Pin Number	Pin Name	Description
1	TXD1	Transmit Data Input 1
2	GND1	Ground 1, Internally Connected to GND2
3	VCC1	Supply Voltage of Transceiver 1
4	RXD1	Receive Data Output 1; Reads out Data from the Bus Lines of Transceiver 1
5	TXD2	Transmit Data Input 2
6	GND2	Ground 2, Internally Connected to GND1
7	VCC2	Supply Voltage of Transceiver 2
8	RXD2	Receive Data Output 2; Reads out Data from the Bus Lines of Transceiver 2
9	CANL2	Low-Level CAN Bus Line 2
10	CANH2	High-Level CAN Bus Line 2
11	STBY2	Standby Mode Control Input of Transceiver 2
12	CANL1	Low-Level CAN Bus Line 1
13	CANH1	High-Level CAN Bus Line 1
14	STBY1	Standby Mode Control Input of Transceiver 1
15	EP <sup>(1)</sup>	Exposed Thermal Pad: Heat Slug, Internally Connected to the GND Pins

**Note 1:** Only for the VDFN package



## Typical Application



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NOTES:

## 2.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings<sup>(†)</sup>

DC Voltage at CANH1, CANL1, CANH2, CANL2 ( $V_{CANH}, V_{CANL}$ ) .....	-27 to +42V
Transient Voltage at CANH, CANL (according to ISO 7637, Part 2) ( $V_{CANH}, V_{CANL}$ ).....	-150 to +100V
Max. Differential Bus Voltage ( $V_{Diff}$ ).....	-5 to +18V
DC Voltage on All Other Pins ( $V_X$ ) .....	-0.3 to +5.5V
ESD according to IBEE CAN EMC – Test Specification following IEC 61000-4-2 – Pins CANH1, CANL1, CANH2, CANL2 .....	±8 kV
ESD (HBM following STM5.1 with 1.5 kΩ/100 pF) – Pins CANH1, CANL1, CANH2, CANL2 to GND .....	±6 kV
Component Level ESD (HBM according to ANSI/ESD STM5.1, JESD22-A114, AEC-Q100 (002) .....	±4 kV
CDM ESD STM 5.3.1 .....	±750V
ESD Machine Model AEC-Q100-RevF(003).....	±200V
Virtual Junction Temperature ( $T_{vj}$ ).....	-40 to +175°C
Storage Temperature Range ( $T_{stg}$ ) .....	-55°C to +150°C

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**TABLE 2-1: ELECTRICAL CHARACTERISTICS**

<b>Electrical Specifications:</b> The values below are valid for each of the two identical integrated CAN transceivers. Grade 1: $T_{amb} = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ and Grade 0: $T_{amb} = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$ ; $V_{VCC} = 4.5\text{V}$ to $5.5\text{V}$ ; $R_L = 60\Omega$ , $C_L = 100\text{ pF}$ unless specified otherwise; all voltages are defined in relation to ground; positive currents flow into the IC.						
Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply, Pin VCC						
Supply Voltage	$V_{VCC}$	4.5	—	5.5	V	
Supply Current in Silent Mode	$I_{VCC\_sil}$	1.9	2.5	3.0	mA	Silent mode, $V_{TXD} = V_{VCC}$
Supply Current in Normal Mode	$I_{VCC\_rec}$	2	—	5	mA	Recessive, $V_{TXD} = V_{VCC}$
	$I_{VCC\_dom}$	30	50	70	mA	Dominant, $V_{TXD} = 0\text{V}$
	$I_{VCC\_short}$	—	—	85	mA	Short between CANH and CANL ( <b>Note 1</b> )
Supply Current in Standby Mode	$I_{VCC\_STBY}$	—	—	12	μA	$V_{TXD} = V_{VCC}$
	$I_{VCC\_STBY}$	—	7	—	μA	$T_{amb} = +25^{\circ}\text{C}$ ( <b>Note 3</b> )
Undervoltage Detection Threshold on Pin VCC	$V_{uvd(VCC)}$	2.75	—	4.5	V	
Mode Control Input, Pin STBY						
High-Level Input Voltage	$V_{IH}$	$0.7 \times V_{VCC}$	—	$V_{VCC} + 0.3$	V	
Low-Level Input Voltage	$V_{IL}$	-0.3	—	$0.3 \times V_{VCC}$	V	
Pull-up Resistor to VCC	$R_{pu}$	75	125	175	kΩ	$V_{STBY} = 0\text{V}$
High-Level Leakage Current	$I_L$	-2	—	+2	μA	$V_{STBY} = V_{VCC}$

- Note 1:** 100% correlation tested.  
**2:** Characterized on samples.  
**3:** Design parameter.

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**TABLE 2-1: ELECTRICAL CHARACTERISTICS (CONTINUED)**

**Electrical Specifications:** The values below are valid for each of the two identical integrated CAN transceivers.  
 Grade 1:  $T_{amb} = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  and Grade 0:  $T_{amb} = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ;  $V_{VCC} = 4.5\text{V}$  to  $5.5\text{V}$ ;  $R_L = 60\Omega$ ,  $C_L = 100\text{pF}$  unless specified otherwise; all voltages are defined in relation to ground; positive currents flow into the IC.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
<b>CAN Transmit Data Input, Pin TXD</b>						
High-Level Input Voltage	$V_{IH}$	$0.7 \times V_{VCC}$	—	$V_{VCC} + 0.3$	V	
Low-Level Input Voltage	$V_{IL}$	-0.3	—	$0.3 \times V_{VCC}$	V	
Pull-up Resistor to VCC	$R_{TXD}$	20	35	50	k $\Omega$	$V_{TXD} = 0\text{V}$
High-Level Leakage Current	$I_{TXD}$	-2	—	+2	$\mu\text{A}$	Normal mode, $V_{TXD} = V_{VCC}$
Input Capacitance	$C_{TXD}$	—	5	10	pF	<b>(Note 3)</b>
<b>CAN Receive Data Output, Pin RXD</b>						
High-Level Output Current	$I_{OH}$	-8	—	-1	mA	Normal mode, $V_{RXD} = V_{VCC} - 0.4\text{V}$
Low-Level Output Current, Bus Dominant	$I_{OL}$	2	—	12	mA	Normal mode, $V_{RXD} = 0.4\text{V}$
<b>Bus Lines, Pins CANH and CANL</b>						
Single-Ended Dominant Output Voltage	$V_{O(dom)}$	2.75	3.5	4.5	V	$V_{TXD} = 0\text{V}$ , $t < t_{to(dom)TXD}$ , $R_L = 50\Omega$ to $65\Omega$ , CANH pin <b>(Note 1)</b>
		0.5	1.5	2.25	V	$V_{TXD} = 0\text{V}$ , $t < t_{to(dom)TXD}$ , $R_L = 50\Omega$ to $65\Omega$ , CANL pin <b>(Note 1)</b>
Transmitter Voltage Symmetry	$V_{Sym}$	0.9	1.0	1.1	—	$V_{Sym} = (V_{CANH} + V_{CANL})/V_{VCC}$ <b>(Note 3)</b>
Bus Differential Output Voltage	$V_{Diff}$	1.5	—	3	V	$V_{TXD} = 0\text{V}$ , $t < t_{to(dom)TXD}$ , $R_L = 45\Omega$ to $65\Omega$
		1.5	—	3.3	V	$R_L = 70\Omega$ <b>(Note 3)</b>
		1.5	—	5	V	$R_L = 2240\Omega$ <b>(Note 3)</b>
		-50	—	+50	mV	$V_{VCC} = 4.75\text{V}$ to $5.25\text{V}$ , $V_{TXD} = V_{VCC}$ , receive, no load
Recessive Output Voltage	$V_{O(rec)}$	2	$0.5 \times V_{VCC}$	3	V	Normal and Silent mode, $V_{TXD} = V_{VCC}$ , no load
	$V_{O(rec)}$	-0.1	—	+0.1	V	Standby mode, $V_{TXD} = V_{VCC}$ , no load
Differential Receiver Threshold Voltage	$V_{th(RX)dif}$	0.5	0.7	0.9	V	Normal and Silent mode (HSC), $V_{cm(CAN)} = -27\text{V}$ to $+27\text{V}$
	$V_{th(RX)dif}$	0.4	0.7	1.1	V	Standby mode (WUC), $V_{cm(CAN)} = -27\text{V}$ to $+27\text{V}$ <b>(Note 1)</b>
Differential Receiver Hysteresis Voltage	$V_{hys(RX)dif}$	50	120	200	mV	Normal and Silent mode (HSC), $V_{cm(CAN)} = -27\text{V}$ to $+27\text{V}$
Dominant Output Current	$I_{IO(dom)}$	-75	—	-35	mA	$V_{TXD} = 0\text{V}$ , $t < t_{to(dom)TXD}$ , $V_{VCC} = 5\text{V}$ , CANH pin, $V_{CANH} = -5\text{V}$
		35	—	75	mA	$V_{TXD} = 0\text{V}$ , $t < t_{to(dom)TXD}$ , $V_{VCC} = 5\text{V}$ , CANL pin, $V_{CANL} = +40\text{V}$

**Note 1:** 100% correlation tested.

**2:** Characterized on samples.

**3:** Design parameter.

**TABLE 2-1: ELECTRICAL CHARACTERISTICS (CONTINUED)**

**Electrical Specifications:** The values below are valid for each of the two identical integrated CAN transceivers.  
 Grade 1:  $T_{amb} = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  and Grade 0:  $T_{amb} = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ;  $V_{VCC} = 4.5\text{V}$  to  $5.5\text{V}$ ;  $R_L = 60\Omega$ ,  $C_L = 100\text{ pF}$  unless specified otherwise; all voltages are defined in relation to ground; positive currents flow into the IC.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Recessive Output Current	$I_{IO(rec)}$	-5	—	+5	mA	Normal and Silent mode, $V_{TXD} = V_{VCC}$ , no load, $V_{CANH} = V_{CANL} = -27\text{V}$ to $+32\text{V}$
Leakage Current	$I_{IO(leak)}$	-5	0	+5	$\mu\text{A}$	$V_{VCC} = 0\text{V}$ , $V_{CANH} = V_{CANL} = 5\text{V}$
	$I_{IO(leak)}$	-5	0	+5	$\mu\text{A}$	$V_{CC}$ is connected to GND with $R = 47\text{k}\Omega$ , $V_{CANH} = V_{CANL} = 5\text{V}$ (Note 3)
Input Resistance	$R_i$	9	15	28	$\text{k}\Omega$	$V_{CANH} = V_{CANL} = 4\text{V}$
	$R_i$	9	15	28	$\text{k}\Omega$	$-2\text{V} \leq V_{CANH} \leq +7\text{V}$ , $-2\text{V} \leq V_{CANL} \leq +7\text{V}$ (Note 3)
Input Resistance Deviation	$\Delta R_i$	-1	0	+1	%	Between CANH and CANL, $V_{CANH} = V_{CANL} = 4\text{V}$
	$\Delta R_i$	-1	0	+1	%	Between CANH and CANL, $-2\text{V} \leq V_{CANH} \leq +7\text{V}$ , $-2\text{V} \leq V_{CANL} \leq +7\text{V}$ (Note 3)
Differential Input Resistance	$R_{i(dif)}$	18	30	56	$\text{k}\Omega$	$V_{CANH} = V_{CANL} = 4\text{V}$
	$R_{i(dif)}$	18	30	56	$\text{k}\Omega$	$-2\text{V} \leq V_{CANH} \leq +7\text{V}$ , $-2\text{V} \leq V_{CANL} \leq +7\text{V}$ (Note 3)
Common-Mode Input Capacitance	$C_{i(cm)}$	—	—	20	pF	(Note 3)
Differential Input Capacitance	$C_{i(dif)}$	—	—	10	pF	(Note 3)
Differential Bus Voltage Range for Recessive State Detection	$V_{Diff\_rec}$	-3	—	+0.5	V	Normal and Silent mode (HSC), $-27\text{V} \leq V_{CANH} \leq +27\text{V}$ , $-27\text{V} \leq V_{CANL} \leq +27\text{V}$ (Note 3)
	$V_{Diff\_rec}$	-3	—	+0.4	V	Standby mode (WUC) $-27\text{V} \leq V_{CANH} \leq +27\text{V}$ , $-27\text{V} \leq V_{CANL} \leq +27\text{V}$ (Note 3)
Differential Bus Voltage Range for Dominant State Detection	$V_{Diff\_dom}$	0.9	—	8.0	V	Normal and Silent mode (HSC), $-27\text{V} \leq V_{CANH} \leq +27\text{V}$ , $-27\text{V} \leq V_{CANL} \leq +27\text{V}$ (Note 3)
	$V_{Diff\_dom}$	1.15	—	8.0	V	Standby mode (WUC), $-27\text{V} \leq V_{CANH} \leq +27\text{V}$ , $-27\text{V} \leq V_{CANL} \leq +27\text{V}$ (Note 3)

- Note 1:** 100% correlation tested.  
**Note 2:** Characterized on samples.  
**Note 3:** Design parameter.

# ATA6565

**TABLE 2-1: ELECTRICAL CHARACTERISTICS (CONTINUED)**

<b>Electrical Specifications:</b> The values below are valid for each of the two identical integrated CAN transceivers. Grade 1: $T_{amb} = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ and Grade 0: $T_{amb} = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$ ; $V_{VCC} = 4.5\text{V}$ to $5.5\text{V}$ ; $R_L = 60\Omega$ , $C_L = 100\text{ pF}$ unless specified otherwise; all voltages are defined in relation to ground; positive currents flow into the IC.						
Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Transceiver Timing, Pins CANH, CANL, TXD and RXD (see <a href="#">Figure 2-1</a> and <a href="#">Figure 2-3</a> )						
Delay Time from TXD to Bus Dominant	$t_{d(\text{TXD-busdom})}$	40	—	130	ns	Normal mode <b>(Note 2)</b>
Delay Time from TXD to Bus Recessive	$t_{d(\text{TXD-busrec})}$	40	—	130	ns	Normal mode <b>(Note 2)</b>
Delay Time from Bus Dominant to RXD	$t_{d(\text{busdom-RXD})}$	20	—	100	ns	Normal mode <b>(Note 2)</b>
Delay Time from Bus Recessive to RXD	$t_{d(\text{busrec-RXD})}$	20	—	100	ns	Normal mode <b>(Note 2)</b>
Propagation Delay from TXD to RXD	$t_{PD(\text{TXD-RXD})}$	40	—	210	ns	Normal mode, rising edge at TXD pin, $R_L = 60\Omega$ , $C_L = 100\text{ pF}$
		40	—	200	ns	Normal mode, falling edge at TXD pin, $R_L = 60\Omega$ , $C_L = 100\text{ pF}$
	$t_{PD(\text{TXD-RXD})}$	—	—	300	ns	Normal mode, rising edge at TXD pin, $R_L = 150\Omega$ , $C_L = 100\text{ pF}$ <b>(Note 3)</b>
		—	—	300	ns	Normal mode, falling edge at TXD pin, $R_L = 150\Omega$ , $C_L = 100\text{ pF}$ <b>(Note 3)</b>
TXD Dominant Time-out Time	$t_{to(\text{dom})\text{TXD}}$	0.8	—	3	ms	$V_{\text{TXD}} = 0\text{V}$ , Normal mode
Bus Wake-up Time-out Time	$t_{\text{Wake}}$	0.8	—	3	ms	Standby mode
Min. Dominant/Recessive Bus Wake-up Time	$t_{\text{Filter}}$	0.5	3	3.8	$\mu\text{s}$	Standby mode
Delay Time for Standby Mode to Normal Mode Transition	$t_{\text{del}(\text{stby-norm})}$	—	—	47	$\mu\text{s}$	Falling edge at STBY pin
Delay Time for Normal Mode to Standby Mode Transition	$t_{\text{del}(\text{norm-stby})}$	—	—	5	$\mu\text{s}$	Rising edge at STBY pin <b>(Note 3)</b>

- Note 1:** 100% correlation tested.  
**Note 2:** Characterized on samples.  
**Note 3:** Design parameter.

**TABLE 2-1: ELECTRICAL CHARACTERISTICS (CONTINUED)**

**Electrical Specifications:** The values below are valid for each of the two identical integrated CAN transceivers. Grade 1:  $T_{amb} = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  and Grade 0:  $T_{amb} = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ;  $V_{VCC} = 4.5\text{V}$  to  $5.5\text{V}$ ;  $R_L = 60\Omega$ ,  $C_L = 100\text{ pF}$  unless specified otherwise; all voltages are defined in relation to ground; positive currents flow into the IC.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Transceiver Timing for Higher Bit Rates, Pins CANH, CANL, TXD and RXD (see <a href="#">Figure 2-1</a> and <a href="#">Figure 2-3</a> ), External Capacitor on the RXD Pin, $C_{RXD} \leq 20\text{ pF}$						
Debouncing Time for Recessive Clamping State Detection	$t_{RC\_det}$	—	—	90	ns	$V_{(CANH-CANL)} > 900\text{ mV}$ , RXD = high ( <b>Note 3</b> )
Recessive Bit Time on RXD	$t_{Bit(RXD)}$	400	—	550	ns	Normal mode, $t_{Bit(TXD)} = 500\text{ ns}$ ( <b>Note 1</b> )
		120	—	220	ns	Normal mode, $t_{Bit(TXD)} = 200\text{ ns}$
Recessive Bit Time on the Bus	$t_{Bit(Bus)}$	435	—	530	ns	Normal mode, $t_{Bit(TXD)} = 500\text{ ns}$ ( <b>Note 1</b> )
		155	—	210	ns	Normal mode, $t_{Bit(TXD)} = 200\text{ ns}$
Receiver Timing Symmetry	$\Delta t_{Rec}$	-65	—	+40	ns	Normal mode, $t_{Bit(TXD)} = 500\text{ ns}$ , $\Delta t_{Rec} = t_{Bit(RXD)} - t_{Bit(Bus)}$ ( <b>Note 1</b> )
		-45	—	+15	ns	Normal mode, $t_{Bit(TXD)} = 200\text{ ns}$ , $\Delta t_{Rec} = t_{Bit(RXD)} - t_{Bit(Bus)}$

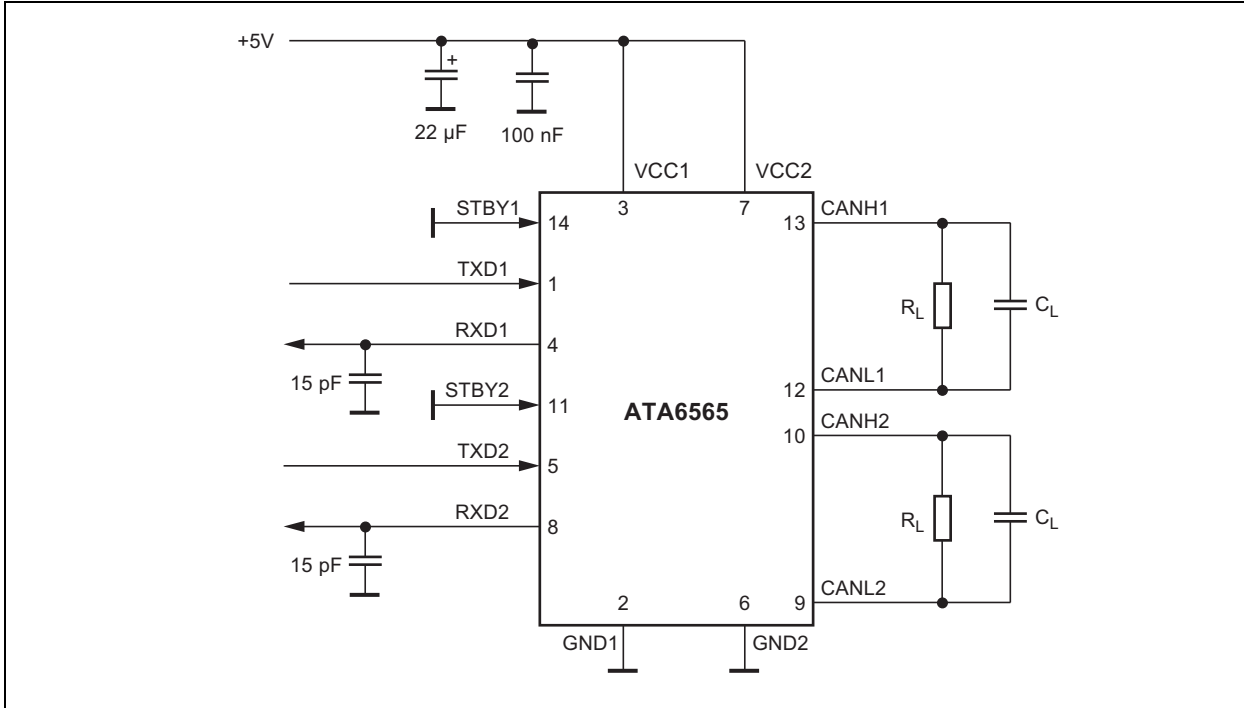
- Note 1:** 100% correlation tested.  
**Note 2:** Characterized on samples.  
**Note 3:** Design parameter.

**TABLE 2-2: TEMPERATURE SPECIFICATIONS**

Parameters	Sym.	Min.	Typ.	Max.	Units
<b>14-Lead SOIC</b>					
Thermal Shutdown of the Bus Drivers for ATA6565-GNQW1 (Grade 1)	$T_{Jsd}$	150	175	190	$^{\circ}\text{C}$
Thermal Shutdown of the Bus Drivers for ATA6565-GNQW0 (Grade 0)	$T_{Jsd}$	160	175	190	$^{\circ}\text{C}$
Thermal Resistance Virtual Junction to Ambient, where IC is soldered to PCB according to JEDEC	$R_{thvJA}$	—	110	—	K/W
<b>14-Lead VDFN</b>					
Thermal Shutdown of the Bus Drivers for ATA6565-GCQW1 (Grade 1)	$T_{Jsd}$	150	175	195	$^{\circ}\text{C}$
Thermal Shutdown of the Bus Drivers for ATA6565-GCQW0 (Grade 0)	$T_{Jsd}$	160	175	195	$^{\circ}\text{C}$
Thermal Resistance Virtual Junction to Heat Slug	$R_{thvJC}$	—	8	—	K/W
Thermal Resistance Virtual Junction to Ambient, where Heat Slug is Soldered to PCB according to JEDEC	$R_{thvJA}$	—	45	—	K/W

# ATA6565

**FIGURE 2-1: TIMING TEST CIRCUIT FOR THE ATA6565 CAN TRANSCEIVER**



**FIGURE 2-2: CAN TRANSCEIVER TIMING DIAGRAM 1**

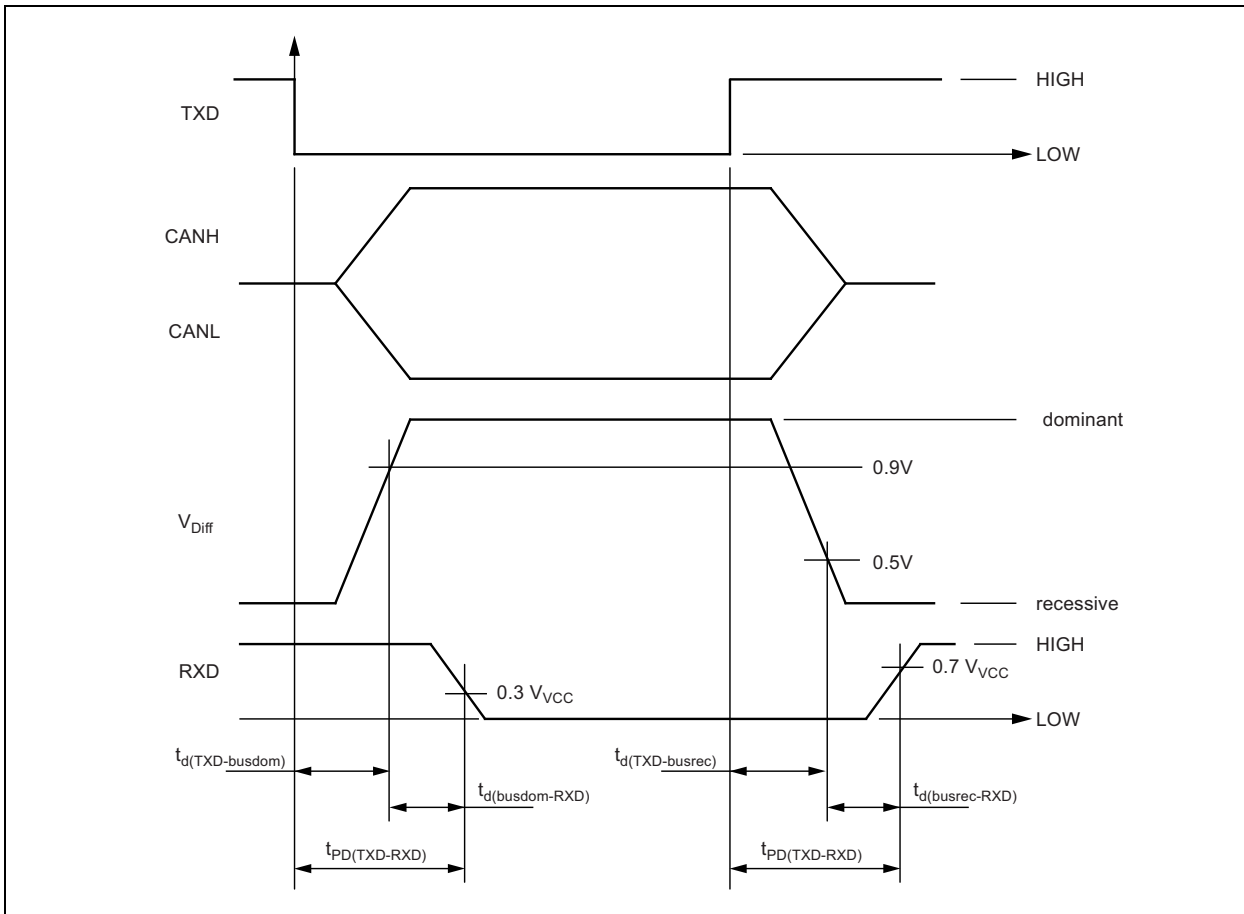
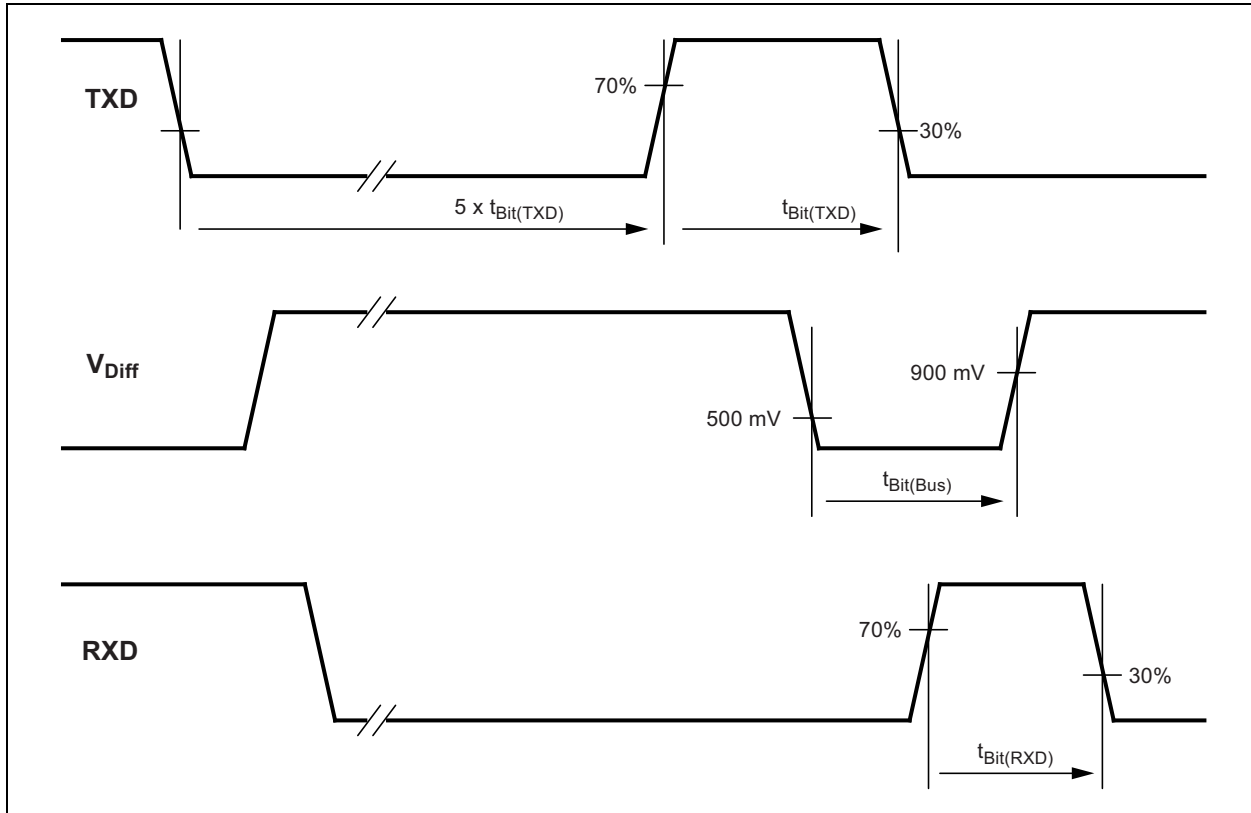




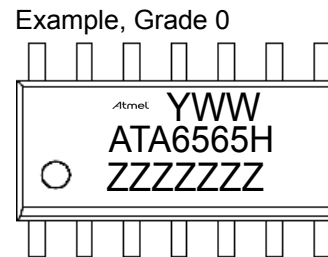
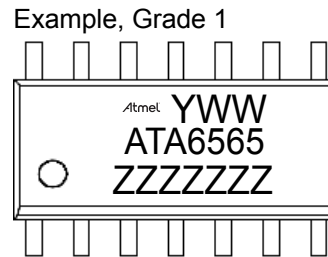
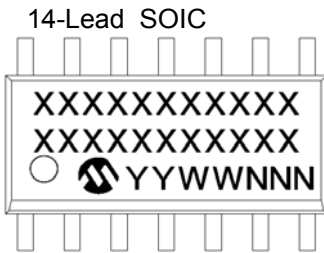
FIGURE 2-3: CAN TRANSCEIVER TIMING DIAGRAM 2



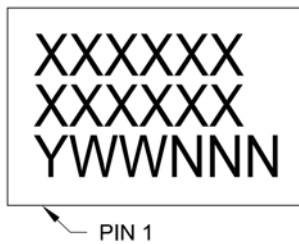
# ATA6565

## 3.0 PACKAGING INFORMATION

### 3.1 Package Marking Information



14-Lead 4.5 x 3 mm VDFN



Example, Grade 1



Example, Grade 0

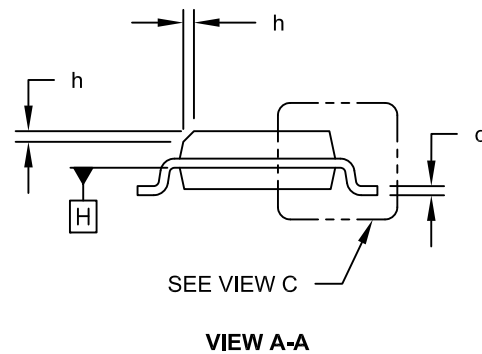
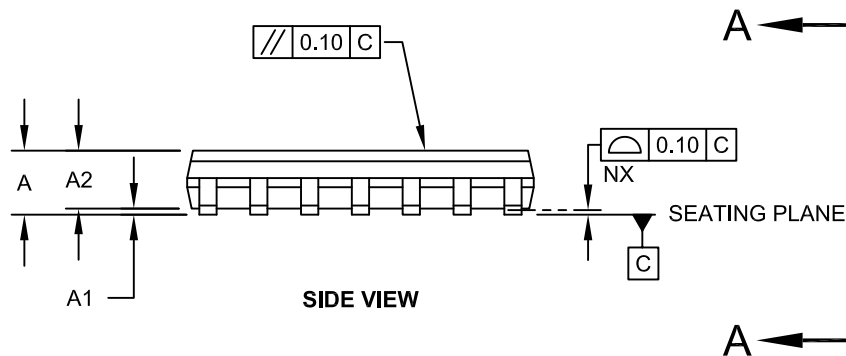
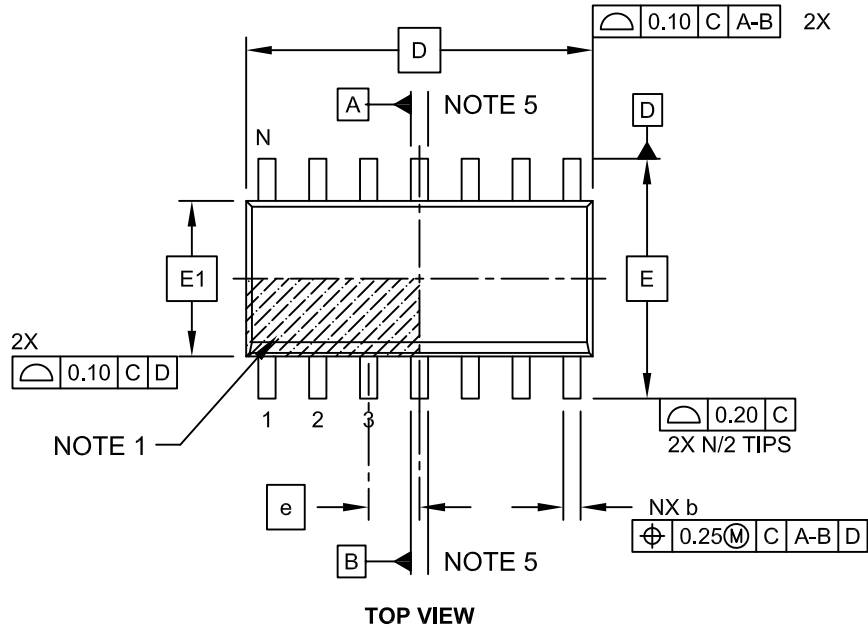


<b>Legend:</b>	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

## 14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

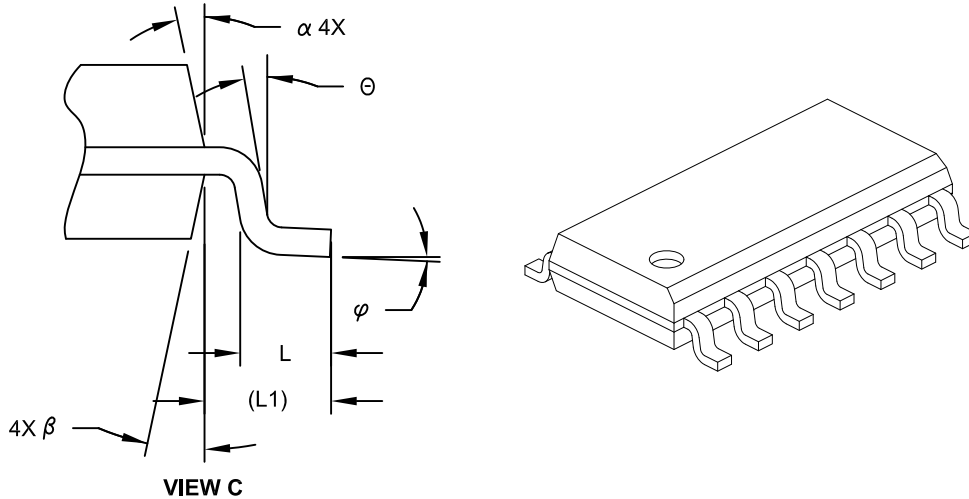


Microchip Technology Drawing No. C04-065C Sheet 1 of 2

# ATA6565

## 14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	14		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	8.65 BSC		
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1	1.04 REF		
Lead Angle	θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.10	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

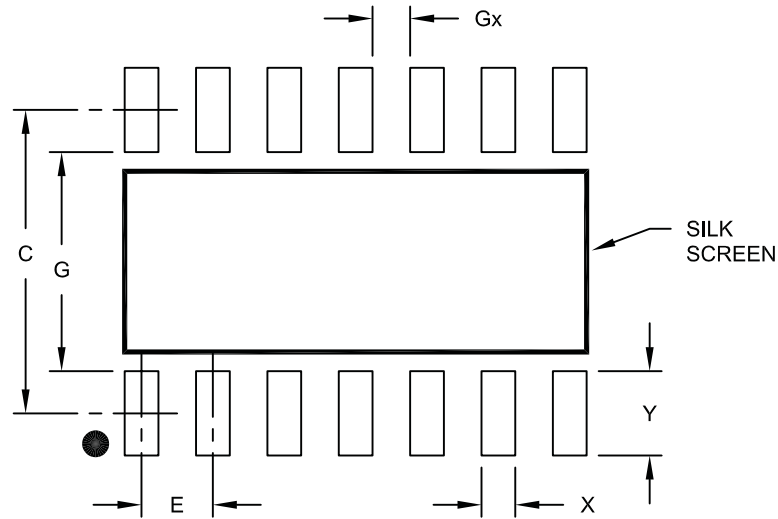
**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic
- Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M  
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.  
 REF: Reference Dimension, usually without tolerance, for information purposes only.
- Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-065C Sheet 2 of 2

## 14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



### RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width	X			0.60
Contact Pad Length	Y			1.50
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	3.90		

**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M

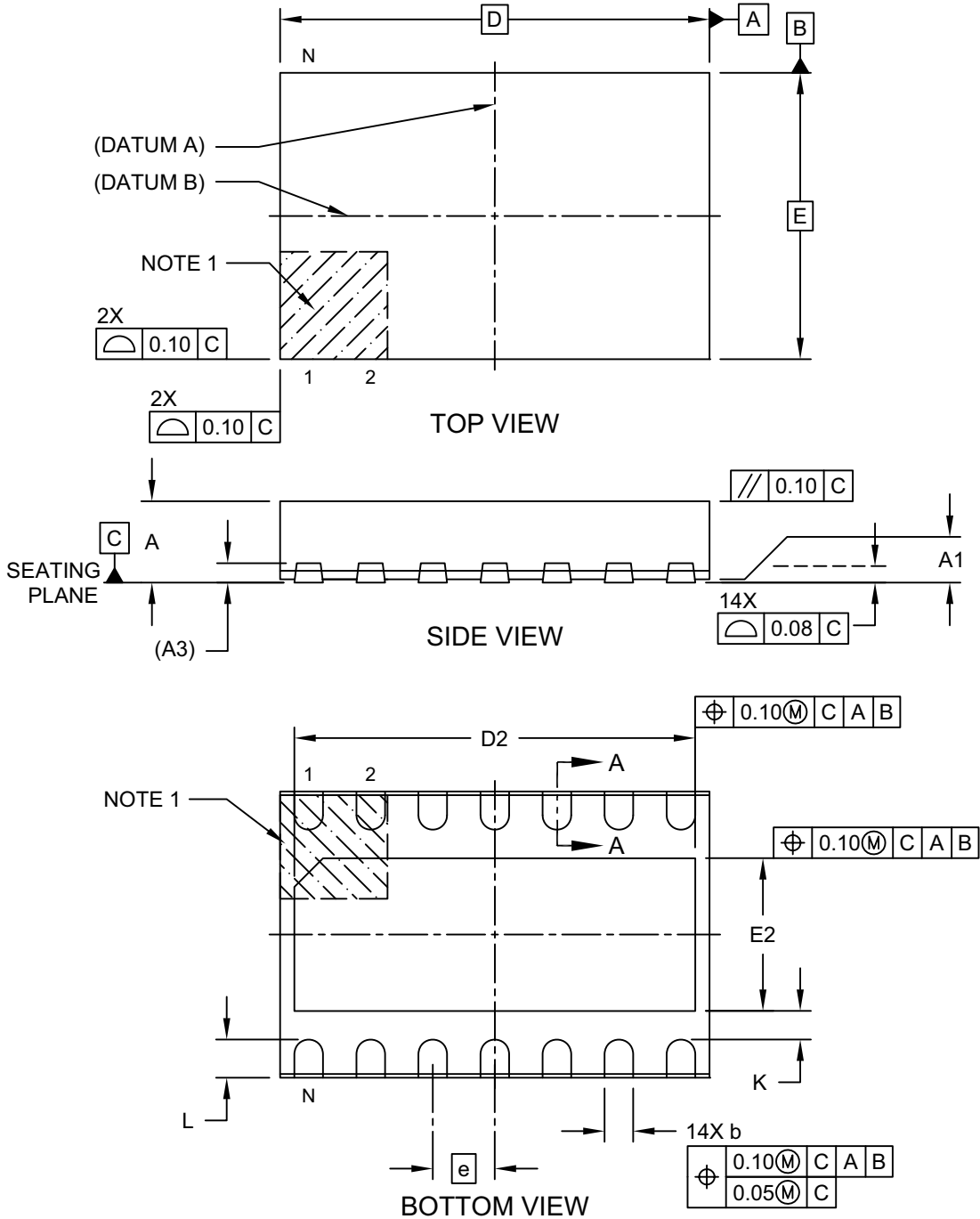
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065A

# ATA6565

## 14-Lead Very Thin Plastic Dual Flat, No Lead Package (QBB) - 4.5x3 mm Body [VDFN] With 1.6x4.2 mm Exposed Pad and Stepped Wettable Flanks

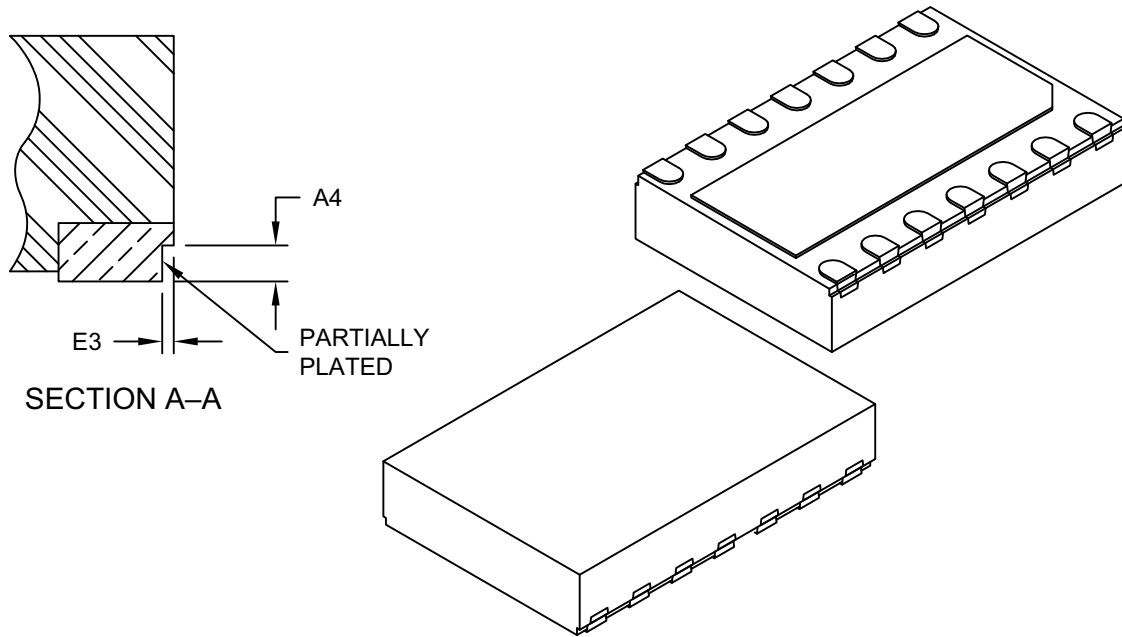
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-21361 Rev A Sheet 1 of 2

## 14-Lead Very Thin Plastic Dual Flat, No Lead Package (QBB) - 4.5x3 mm Body [VDFN] With 1.6x4.2 mm Exposed Pad and Stepped Wettable Flanks

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Terminals	N		14		
Pitch	e		0.65 BSC		
Overall Height	A		0.80	0.85	0.90
Standoff	A1		0.00	0.03	0.05
Terminal Thickness	A3		0.203 REF		
Overall Length	D		4.50 BSC		
Exposed Pad Length	D2		4.15	4.20	4.25
Overall Width	E		3.00 BSC		
Exposed Pad Width	E2		1.55	1.60	1.65
Terminal Width	b		0.27	0.32	0.37
Terminal Length	L		0.35	0.40	0.45
Terminal-to-Exposed-Pad	K		0.20	-	-
Wettable Flank Step Cut Depth	A4		0.10	0.13	0.15
Wettable Flank Step Cut Width	E3		-	-	0.04

**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated
- Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

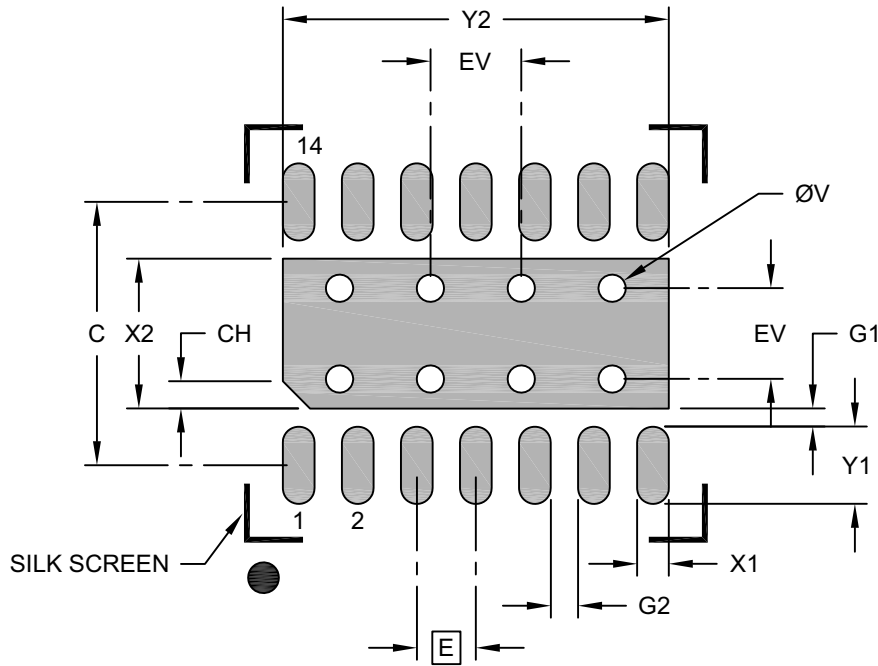
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21361 Rev A Sheet 2 of 2

# ATA6565

## 14-Lead Very Thin Plastic Dual Flat, No Lead Package (QBB) - 4.5x3 mm Body [VDFN] With 1.6x4.2 mm Exposed Pad and Stepped Wettable Flanks

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



### RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	X2			1.65
Optional Center Pad Length	Y2			4.25
Contact Pad Spacing	C	2.90		
Contact Pad Width (X14)	X1			0.35
Contact Pad Length (X14)	Y1			0.85
Pin 1 Index Chamfer	CH	0.30		
Contact Pad to Center Pad (X14)	G1	0.20		
Contact Pad to Center Pad (X12)	G2	0.20		
Thermal Via Diameter	V	0.30		
Thermal Via Pitch	EV	1.00		

**Notes:**

- Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-23361 Rev A



## APPENDIX A: REVISION HISTORY

### Revision B (September 2017)

The following is the list of modifications:

- Added the new devices ATA6565-GNQW0 and ATA6565- GNQW1 and updated the related information across the document.
- Updated [Package Types](#) section.
- Updated [ATA6565 Family Members](#) section.
- Modified [Figure 1-3](#).
- Updated [Section 1.3, Pin Description](#).
- Updated [Temperature Specifications](#).
- Updated [Section 3.0, Packaging Information](#).
- Updated the [Product Identification System](#).
- Fixed minor typographical errors.

### Revision A (June 2017)

- Original Release of this Document.
- This document replaces Atmel - 9364G-11/16.

# ATA6565

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NOTES:

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>XX</u>	<u>IXI<sup>(1)</sup></u>	<u>X</u>	<u>X</u>
Device	Package	Tape and Reel Option	Package Directives Classification	Temperature Range
<b>Device:</b>	ATA6565: Dual High-Speed CAN Transceiver with Standby Mode			
<b>Package:</b>	GC = 14-Lead VDFN GN = 14-Lead SOIC			
<b>Tape and Reel Option:</b>	Q = 330 mm diameter Tape and Reel			
<b>Package Directives Classification:</b>	W = Package according to RoHS <sup>(2)</sup>			
<b>Temperature Range:</b>	0 = Temperature Grade 0 (-40°C to +150°C) 1 = Temperature Grade 1 (-40°C to +125°C)			

<b>Examples:</b>	
a) ATA6565-GCQW0:	ATA6565, 14-Lead VDFN, Tape and Reel, Package according to RoHS, Temperature Grade 0
b) ATA6565-GCQW1:	ATA6565, 14-Lead VDFN, Tape and Reel, Package according to RoHS, Temperature Grade 1
c) ATA6565-GNQW1:	ATA6565, 14-Lead SOIC, Tape and Reel, Package according to RoHS, Temperature Grade 1
b) ATA6565-GNQW0:	ATA6565, 14-Lead SOIC, Tape and Reel, Package according to RoHS, Temperature Grade 0

<b>Note 1:</b>	Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
<b>2:</b>	RoHS compliant, maximum concentration value of 0.09% (900 ppm) for Bromine (Br) and Chlorine (Cl), and less than 0.15% (1500 ppm) total Bromine (Br) and Chlorine (Cl) in any homogeneous material. Maximum concentration value of 0.09% (900 ppm) for Antimony (Sb) in any homogeneous material.

# ATA6565

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NOTES:

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**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

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