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Kind regards,

Team Nexperia



# BUK7240-100A

## N-channel TrenchMOS standard level FET

Rev. 2 — 23 February 2011

Product data sheet

## 1. Product profile

### 1.1 General description

Standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

### 1.2 Features and benefits

- AEC Q101 compliant
- Low conduction losses due to low on-state resistance
- Suitable for standard level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

### 1.3 Applications

- 12 V and 24 V loads
- Automotive and general purpose power switching
- Motors, lamps and solenoids

### 1.4 Quick reference data

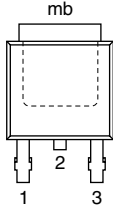
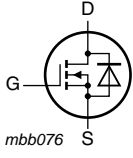
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	-	100	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a>	-	-	34	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	-	114	W
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 175\text{ °C}$ ; see <a href="#">Figure 12</a> ; see <a href="#">Figure 13</a>	-	-	100	m $\Omega$
		$V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 12</a> ; see <a href="#">Figure 13</a>	-	34	40	m $\Omega$
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 35\text{ A}$ ; $V_{sup} \leq 100\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; unclamped	-	-	122.5	mJ



## 2. Pinning information

**Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p style="text-align: center;"><b>SOT428 (DPAK)</b></p>	 <p style="text-align: center;"><i>mbb076</i></p>
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

## 3. Ordering information

**Table 3. Ordering information**

Type number	Package		Version
	Name	Description	
BUK7240-100A	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

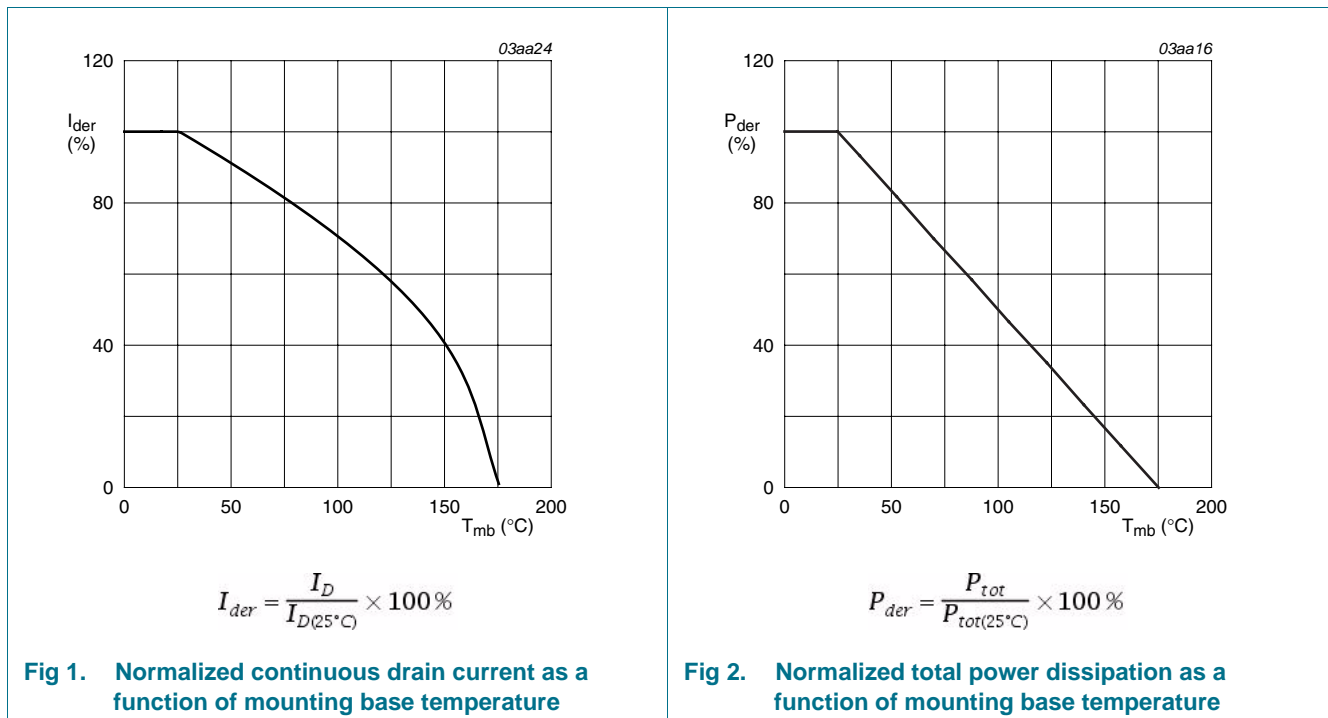
## 4. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C	-	100	V
V <sub>DGR</sub>	drain-gate voltage	R <sub>GS</sub> = 20 kΩ	-	100	V
V <sub>GS</sub>	gate-source voltage		-20	20	V
I <sub>D</sub>	drain current	T <sub>mb</sub> = 100 °C; V <sub>GS</sub> = 10 V; see <a href="#">Figure 1</a> T <sub>mb</sub> = 25 °C; V <sub>GS</sub> = 10 V; see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a>	-	24 34	A
I <sub>DM</sub>	peak drain current	T <sub>mb</sub> = 25 °C; pulsed; t <sub>p</sub> ≤ 10 μs; see <a href="#">Figure 3</a> [1]	-	136	A
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <a href="#">Figure 2</a>	-	114	W
T <sub>stg</sub>	storage temperature		-55	175	°C
T <sub>j</sub>	junction temperature		-55	175	°C
<b>Source-drain diode</b>					
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	-	34	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C	-	136	A
<b>Avalanche ruggedness</b>					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	I <sub>D</sub> = 35 A; V <sub>sup</sub> ≤ 100 V; R <sub>GS</sub> = 50 Ω; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; unclamped	-	122.5	mJ

[1] Peak drain current is limited by chip, not package.



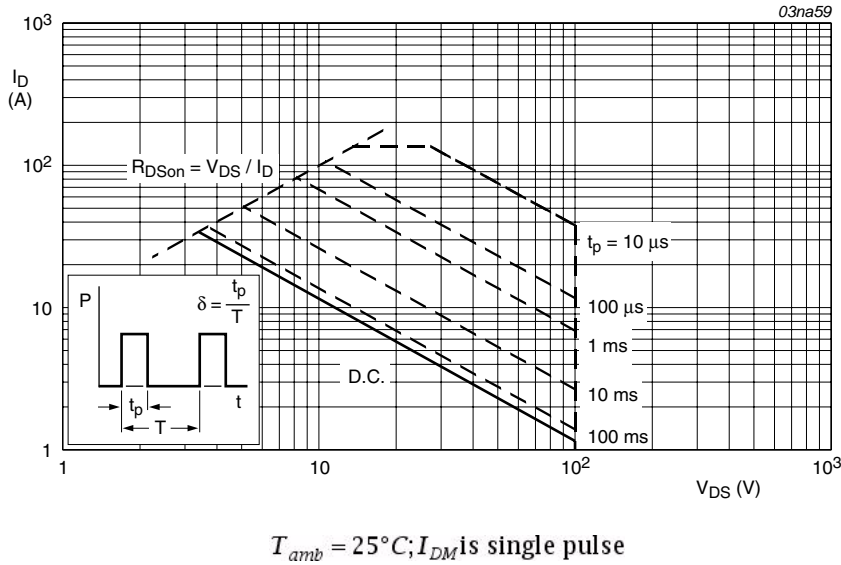


Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

## 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	-	1.3	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		-	71.4	-	K/W

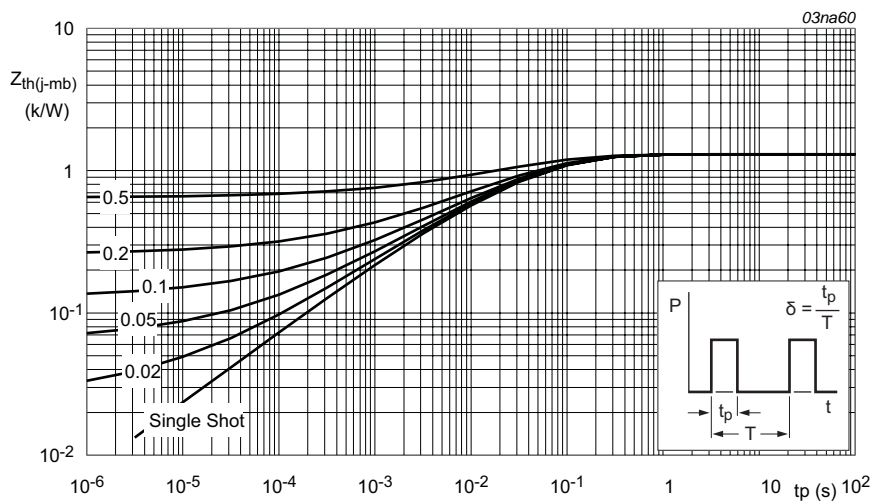
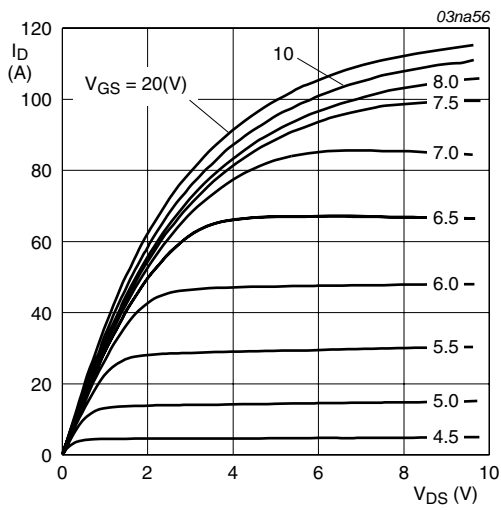


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 6. Characteristics

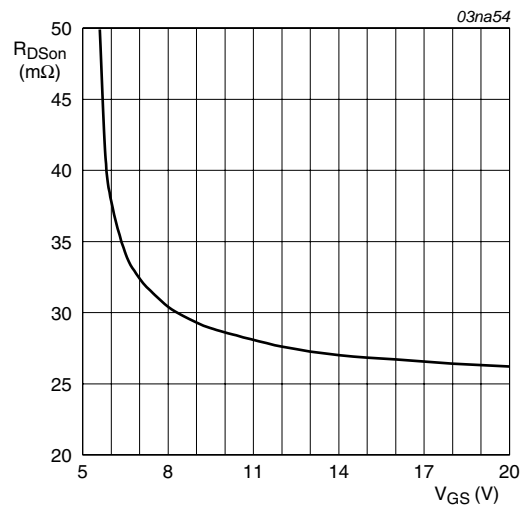
**Table 6. Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ °C}$	100	-	-	V
		$I_D = 0.25\text{ A}; V_{GS} = 0\text{ V}; T_j = -55\text{ °C}$	89	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}; V_{DS} = V_{GS}; T_j = 175\text{ °C};$ see <a href="#">Figure 11</a>	1	-	-	V
		$I_D = 1\text{ mA}; V_{DS} = V_{GS}; T_j = 25\text{ °C};$ see <a href="#">Figure 11</a>	2	3	4	V
		$I_D = 1\text{ mA}; V_{DS} = V_{GS}; T_j = -55\text{ °C};$ see <a href="#">Figure 11</a>	-	-	4.4	V
$I_{DSS}$	drain leakage current	$V_{DS} = 100\text{ V}; V_{GS} = 0\text{ V}; T_j = 25\text{ °C}$	-	0.05	10	$\mu\text{A}$
		$V_{DS} = 100\text{ V}; V_{GS} = 0\text{ V}; T_j = 175\text{ °C}$	-	-	500	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 20\text{ V}; V_{DS} = 0\text{ V}; T_j = 25\text{ °C}$	-	2	100	nA
		$V_{GS} = -20\text{ V}; V_{DS} = 0\text{ V}; T_j = 25\text{ °C}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 175\text{ °C};$ see <a href="#">Figure 12</a> ; see <a href="#">Figure 13</a>	-	-	100	$\text{m}\Omega$
		$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C};$ see <a href="#">Figure 12</a> ; see <a href="#">Figure 13</a>	-	34	40	$\text{m}\Omega$
<b>Dynamic characteristics</b>						
$C_{iss}$	input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz};$ $T_j = 25\text{ °C};$ see <a href="#">Figure 14</a>	-	1720	2293	pF
$C_{oss}$	output capacitance		-	216	259	pF
$C_{rss}$	reverse transfer capacitance		-	133	182	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 50\text{ V}; R_L = 1.5\ \Omega; V_{GS} = 10\text{ V};$ $R_{G(ext)} = 5.6\ \Omega; T_j = 25\text{ °C}$	-	12	-	ns
$t_r$	rise time		-	55	-	ns
$t_{d(off)}$	turn-off delay time		-	48	-	ns
$t_f$	fall time		-	30	-	ns
$L_D$	internal drain inductance	measured from drain lead from package to centre of die; $T_j = 25\text{ °C}$	-	2.5	-	nH
$L_S$	internal source inductance	measured from source lead from package to source bond pad; $T_j = 25\text{ °C}$	-	7.5	-	nH
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ °C};$ see <a href="#">Figure 15</a>	-	0.85	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 17\text{ A}; dI_S/dt = -100\text{ A}/\mu\text{s};$ $V_{GS} = -10\text{ V}; V_{DS} = 25\text{ V}; T_j = 25\text{ °C}$	-	70	-	ns
$Q_r$	recovered charge		-	240	-	nC



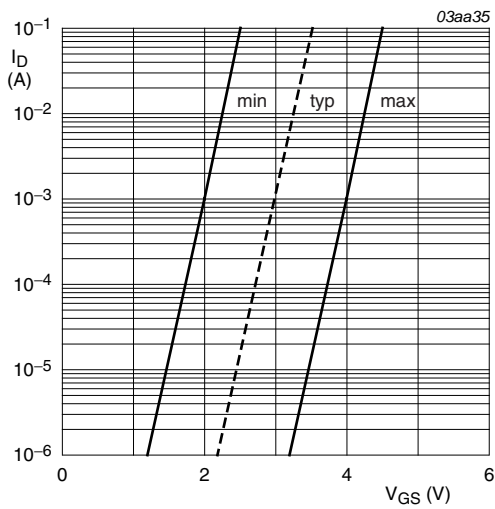
$T_j = 25^\circ\text{C}$

**Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values**



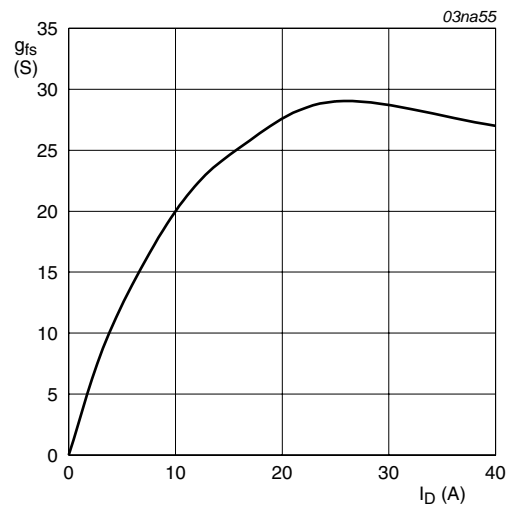
$T_j = 25^\circ\text{C}; I_D = 25\text{A}$

**Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values**



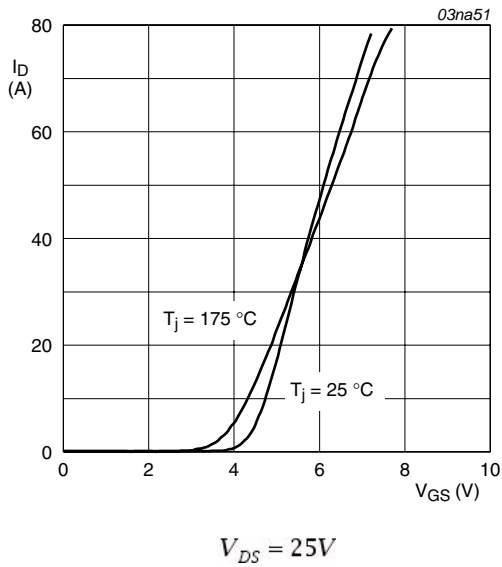
$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$

**Fig 7. Sub-threshold drain current as a function of gate-source voltage**

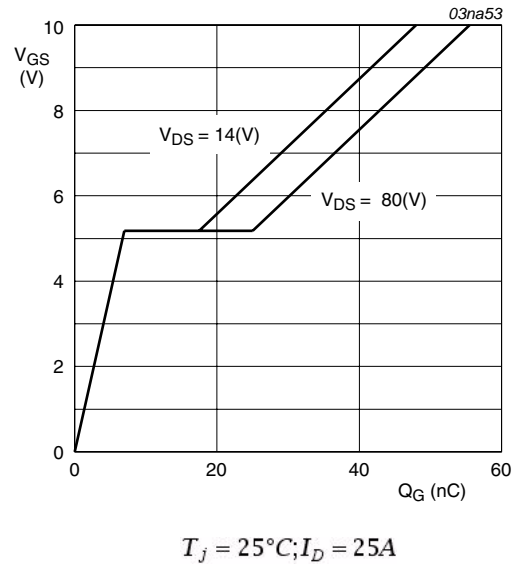


$T_j = 25^\circ\text{C}; V_{DS} = 25\text{V}$

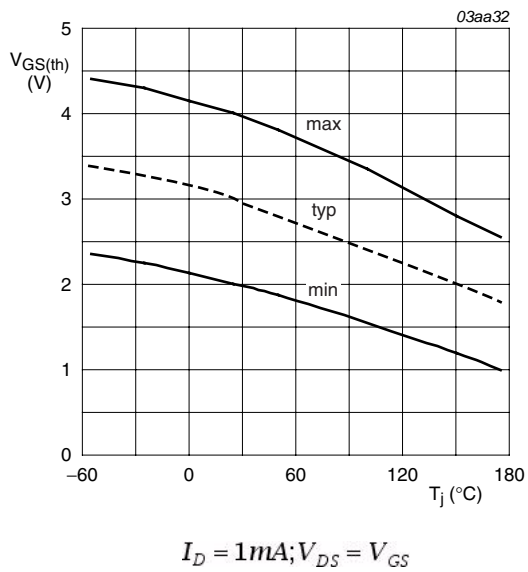
**Fig 8. Forward transconductance as a function of drain current; typical values**



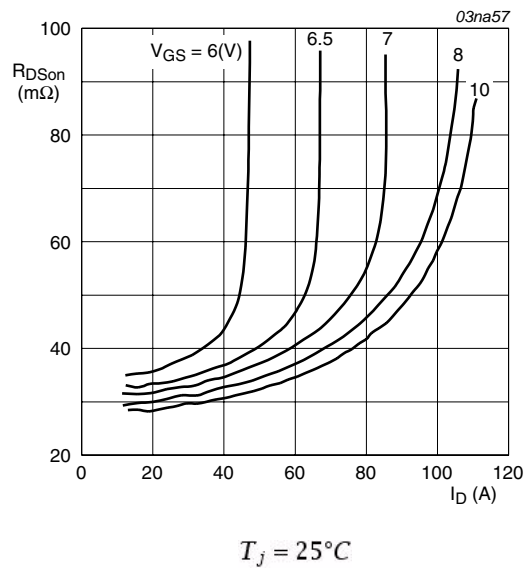
**Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



**Fig 10. Gate-source voltage as a function of turn-on gate charge; typical values**

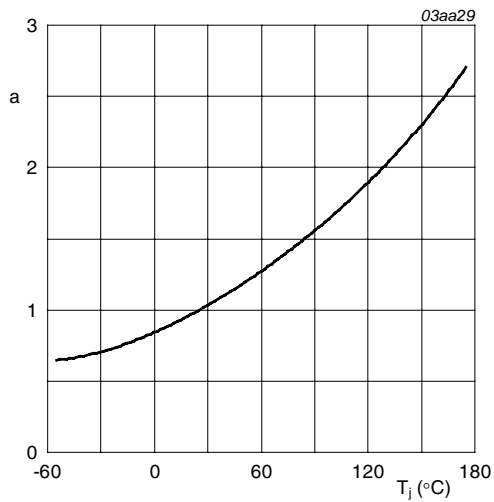


**Fig 11. Gate-source threshold voltage as a function of junction temperature**



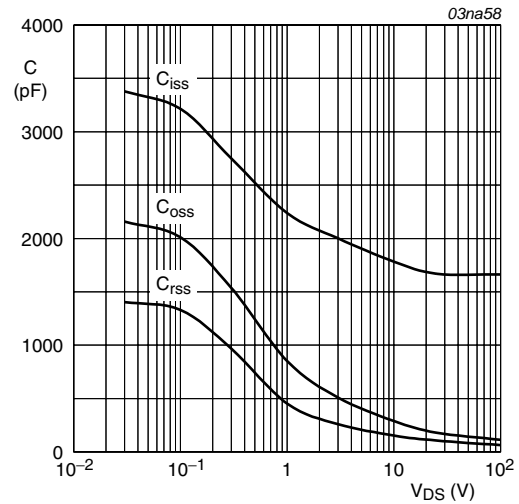
**Fig 12. Drain-source on-state resistance as a function of drain current; typical values**





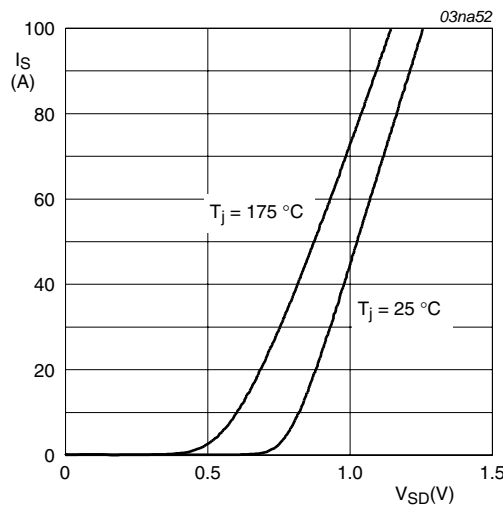
$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

**Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature**



$$V_{GS} = 0V; f = 1MHz$$

**Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



$$V_{DS} = 0V$$

**Fig 15. Reverse diode current; typical values**

**7. Package outline**

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)

SOT428

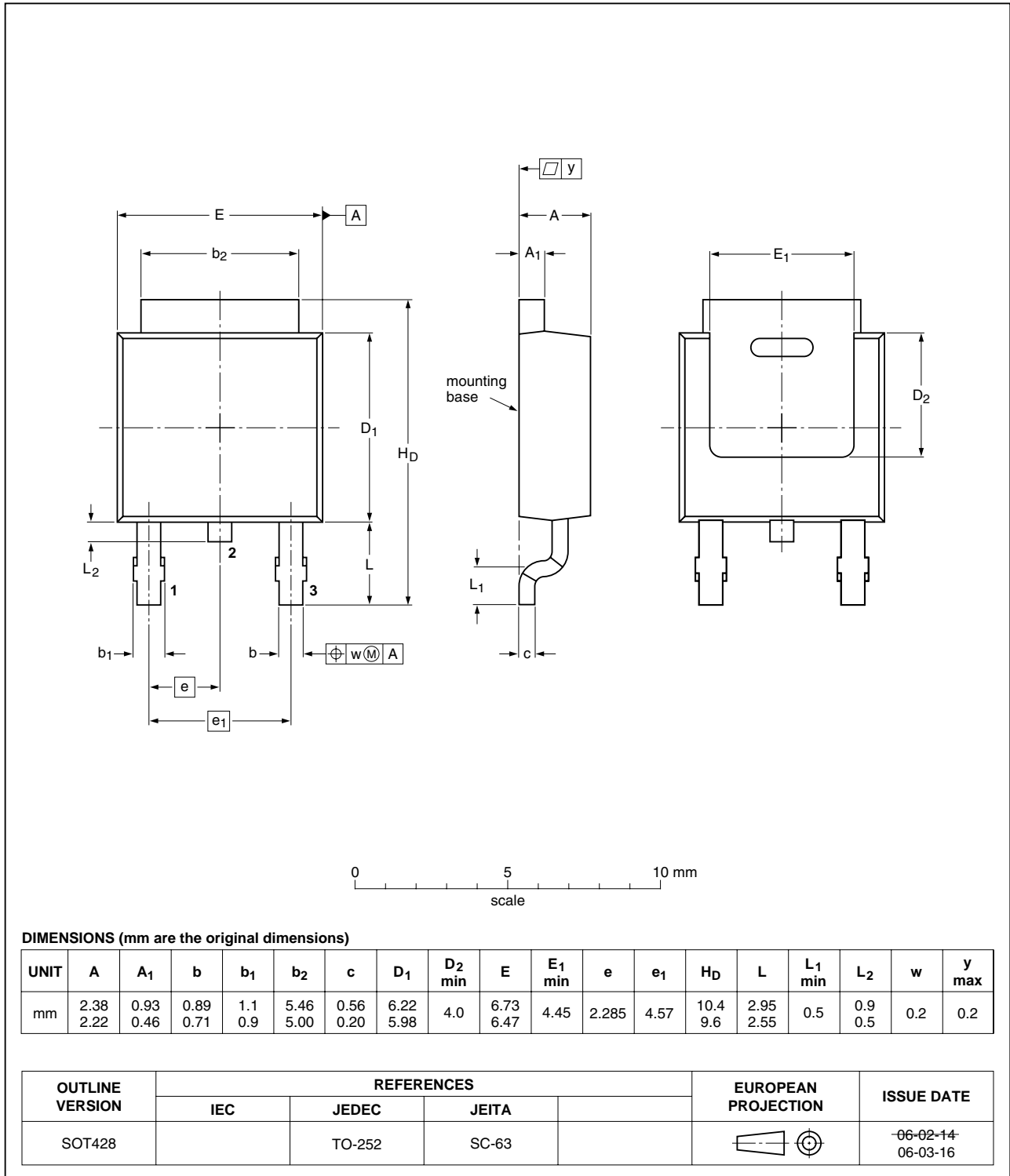


Fig 16. Package outline SOT428 (DPAK)

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK7240-100A v.2	20110223	Product data sheet	-	BUK7240_100A-01
Modifications:	<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>• Legal texts have been adapted to the new company name where appropriate.</li></ul>			
BUK7240_100A-01	20001003	Product specification	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1]</sup> <sup>[2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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## 11. Contents

<b>1</b>	<b>Product profile</b> . . . . .	<b>1</b>
1.1	General description . . . . .	1
1.2	Features and benefits . . . . .	1
1.3	Applications . . . . .	1
1.4	Quick reference data . . . . .	1
<b>2</b>	<b>Pinning information</b> . . . . .	<b>2</b>
<b>3</b>	<b>Ordering information</b> . . . . .	<b>2</b>
<b>4</b>	<b>Limiting values</b> . . . . .	<b>3</b>
<b>5</b>	<b>Thermal characteristics</b> . . . . .	<b>4</b>
<b>6</b>	<b>Characteristics</b> . . . . .	<b>5</b>
<b>7</b>	<b>Package outline</b> . . . . .	<b>9</b>
<b>8</b>	<b>Revision history</b> . . . . .	<b>10</b>
<b>9</b>	<b>Legal information</b> . . . . .	<b>11</b>
9.1	Data sheet status . . . . .	11
9.2	Definitions . . . . .	11
9.3	Disclaimers . . . . .	11
9.4	Trademarks . . . . .	12
<b>10</b>	<b>Contact information</b> . . . . .	<b>12</b>

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